

ABSTRACT OF THE DISCLOSURE

SHIFT REGISTER FOR PULSE-CUT CLOCK SIGNAL

When a voltage level of a pulse-cut first clock signal inputted to a first clock terminal is reversed in the state where a first transistor is turned on and a second transistor is turned off, an anti-reversal circuit including a seventh transistor and an eighth transistor supplies a high voltage VDD to a node n2. In this way, a floating state of the node n2 is avoided, and the voltage level of the node n2 is prevented from being reversed. Accordingly, the second transistor will not be turned on in the interval, whereby electric potential of an output signal is stably maintained.

(Figure 4)



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