

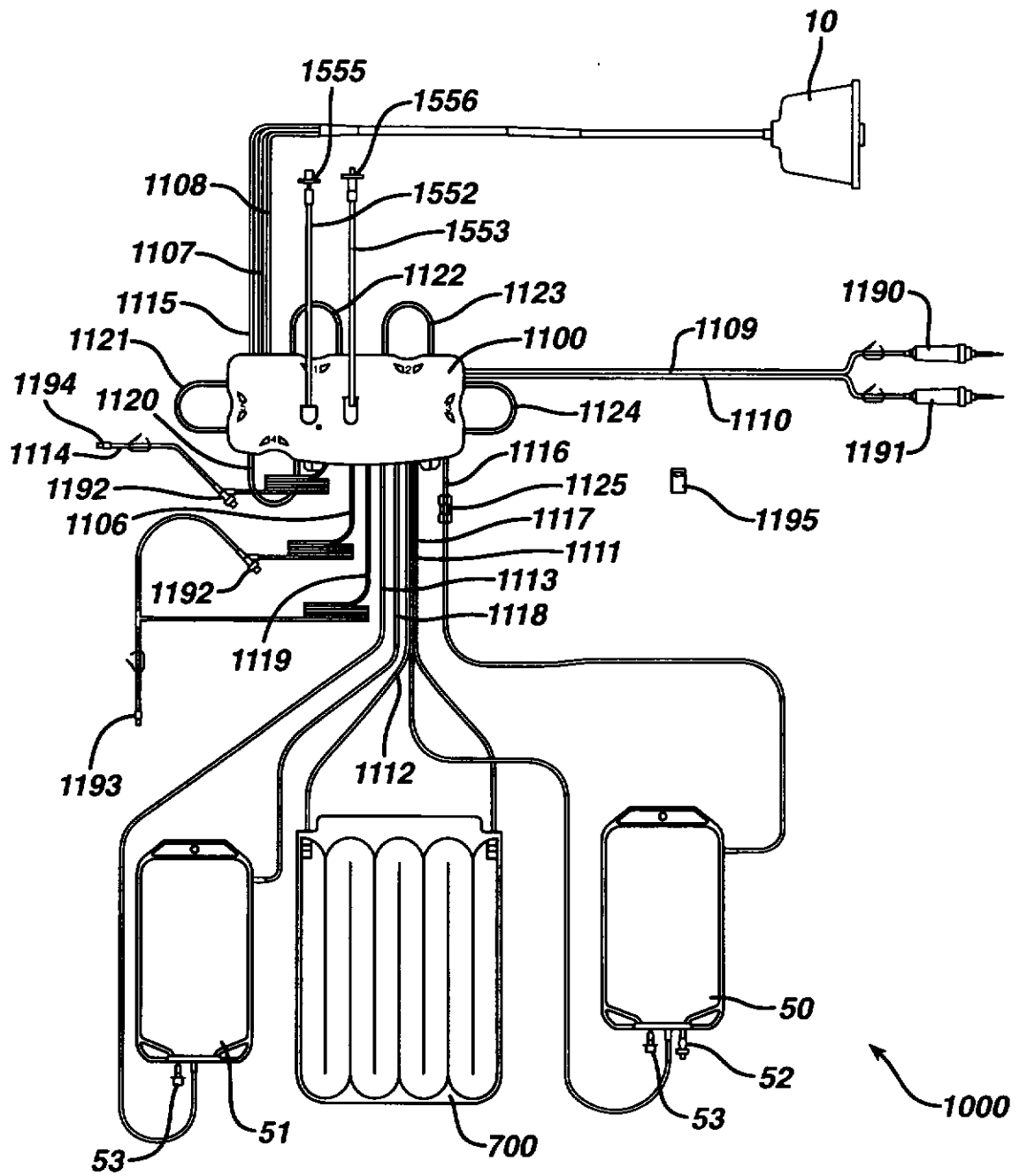
FIG. 1

FIG. 2

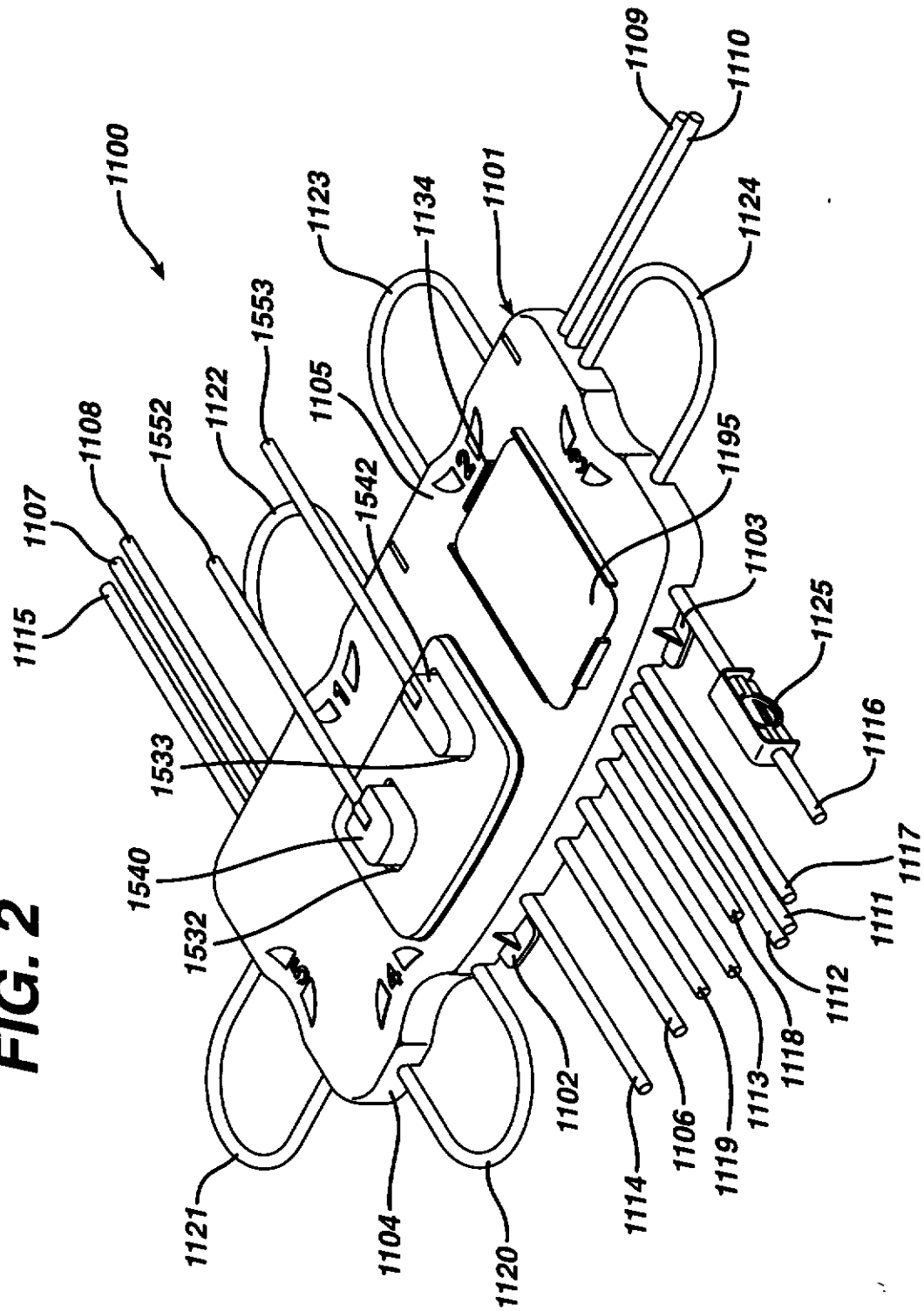


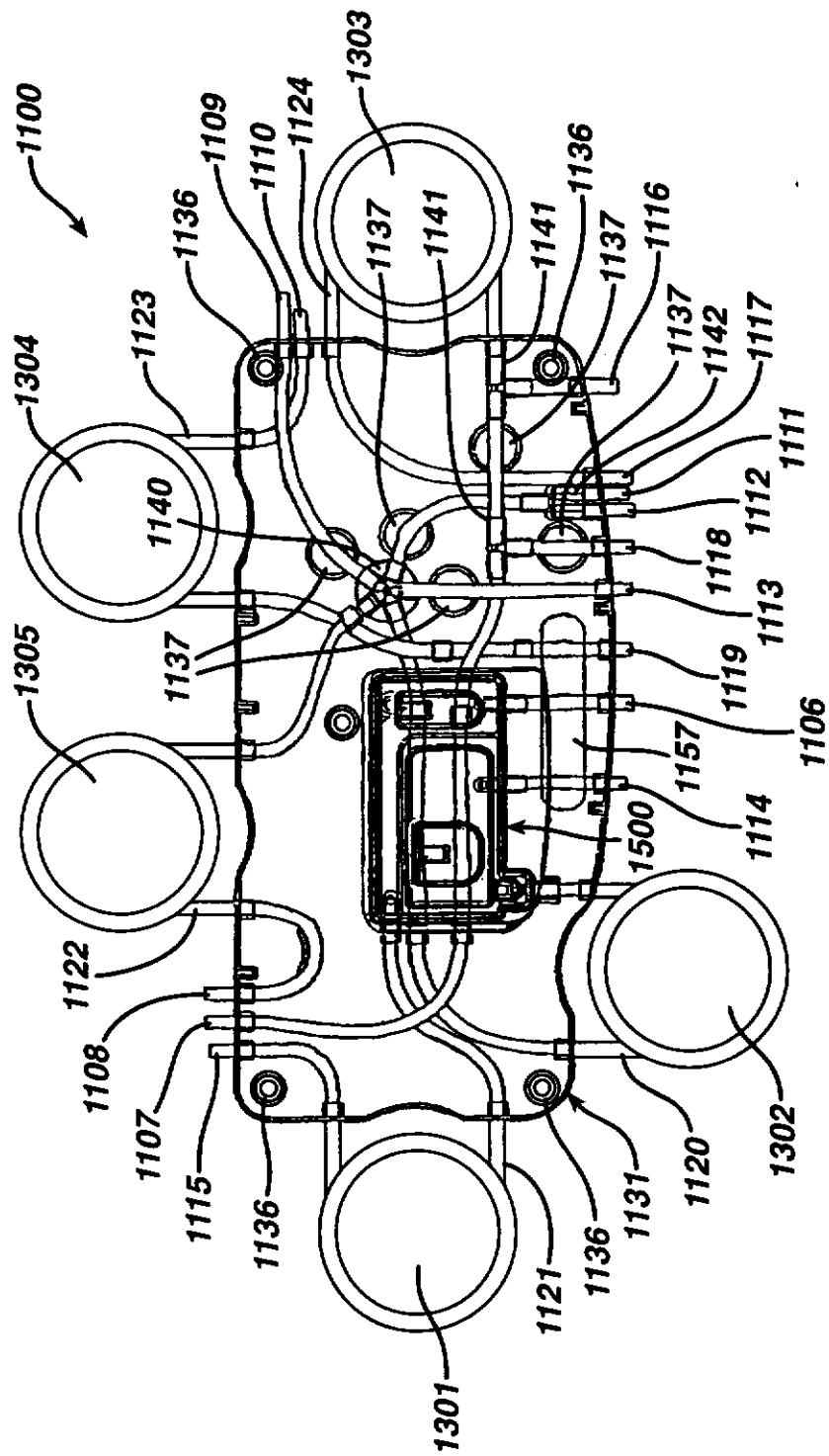
FIG. 4

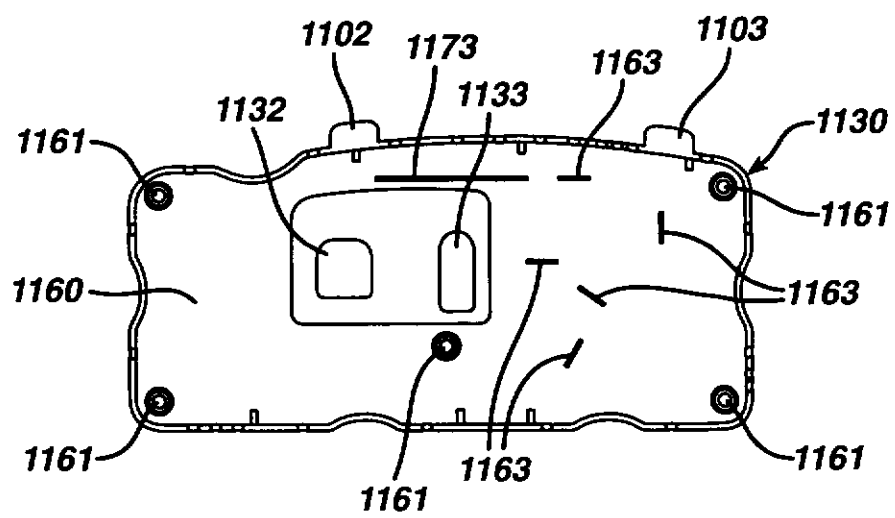
FIG. 5

FIG. 6

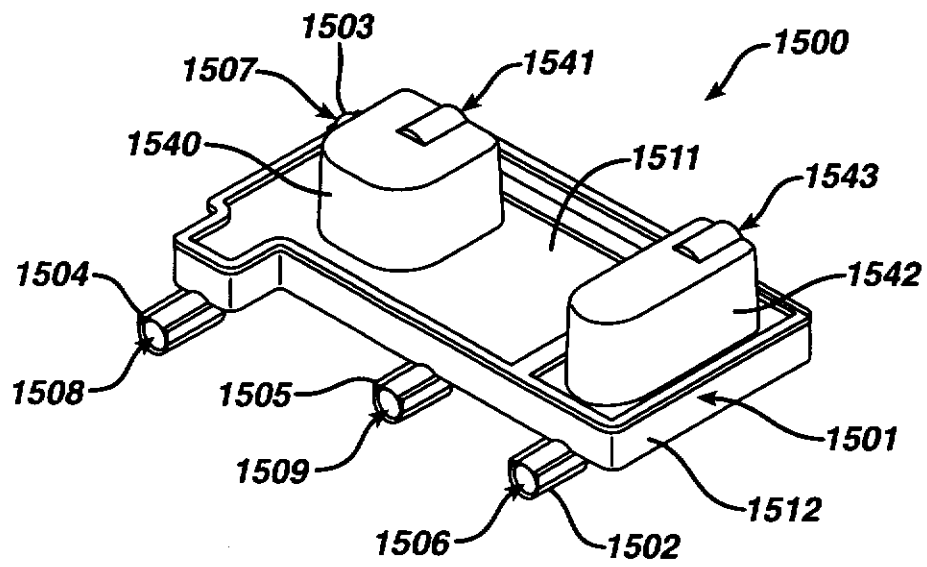


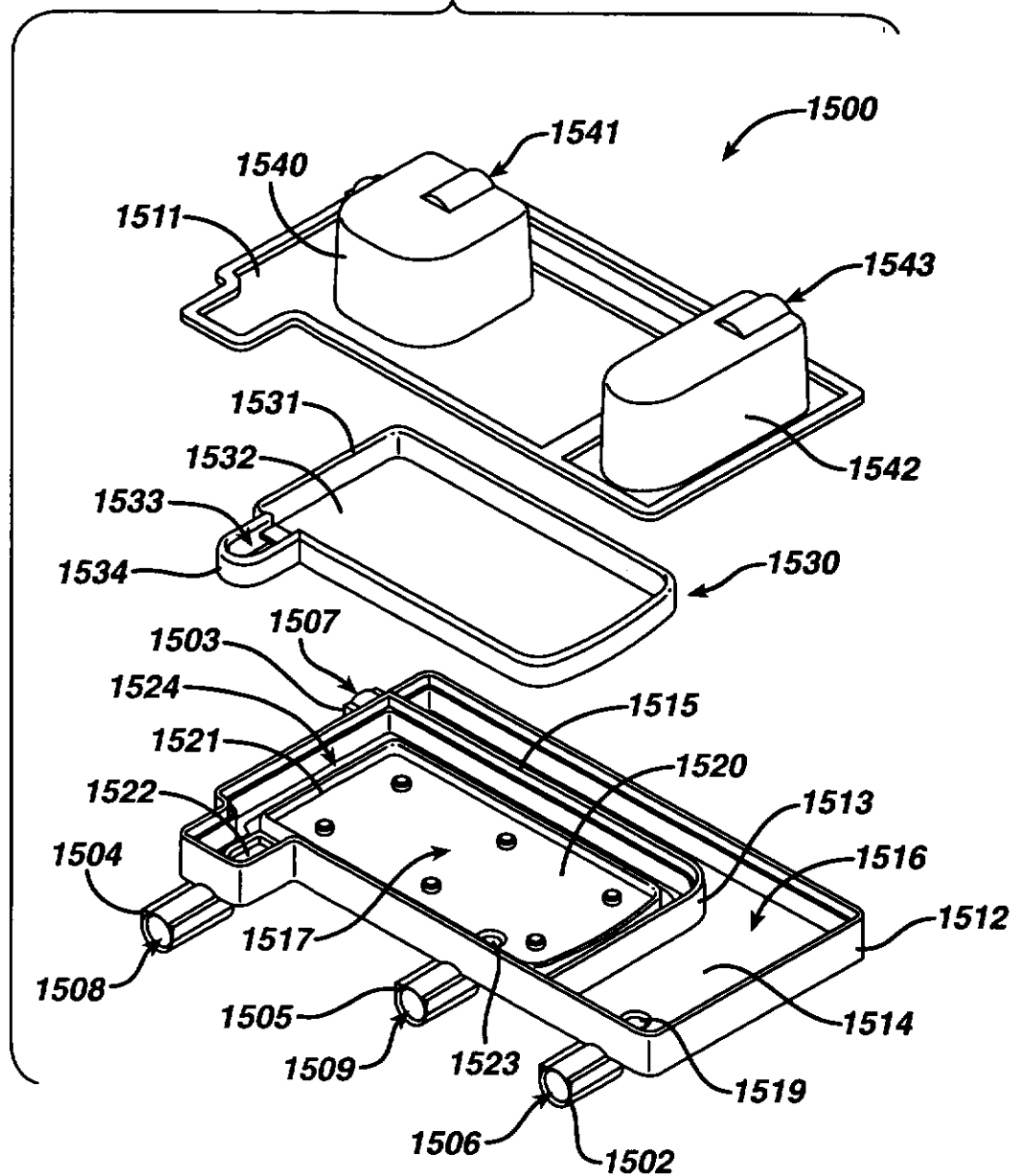
FIG. 8

FIG. 9

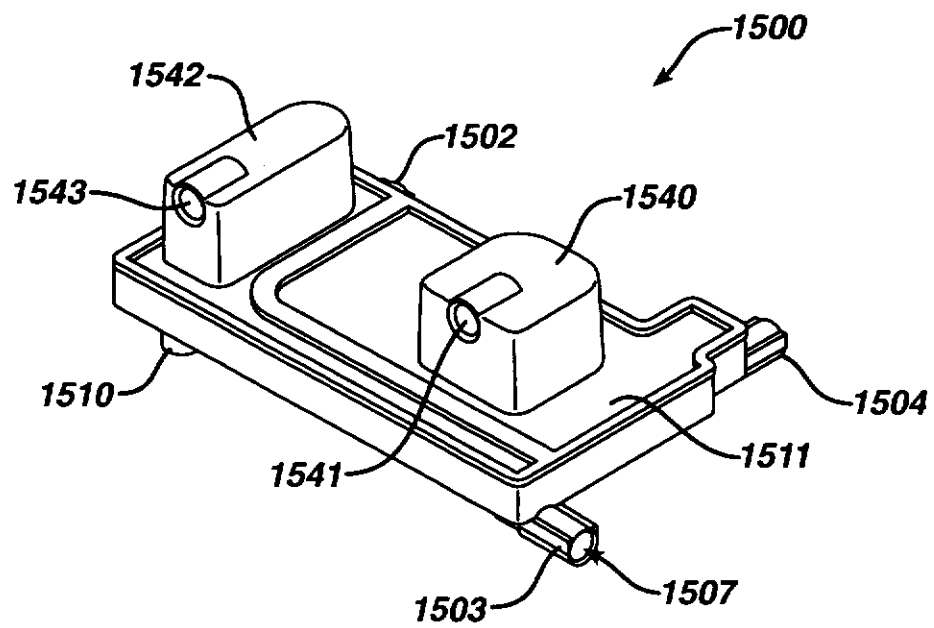


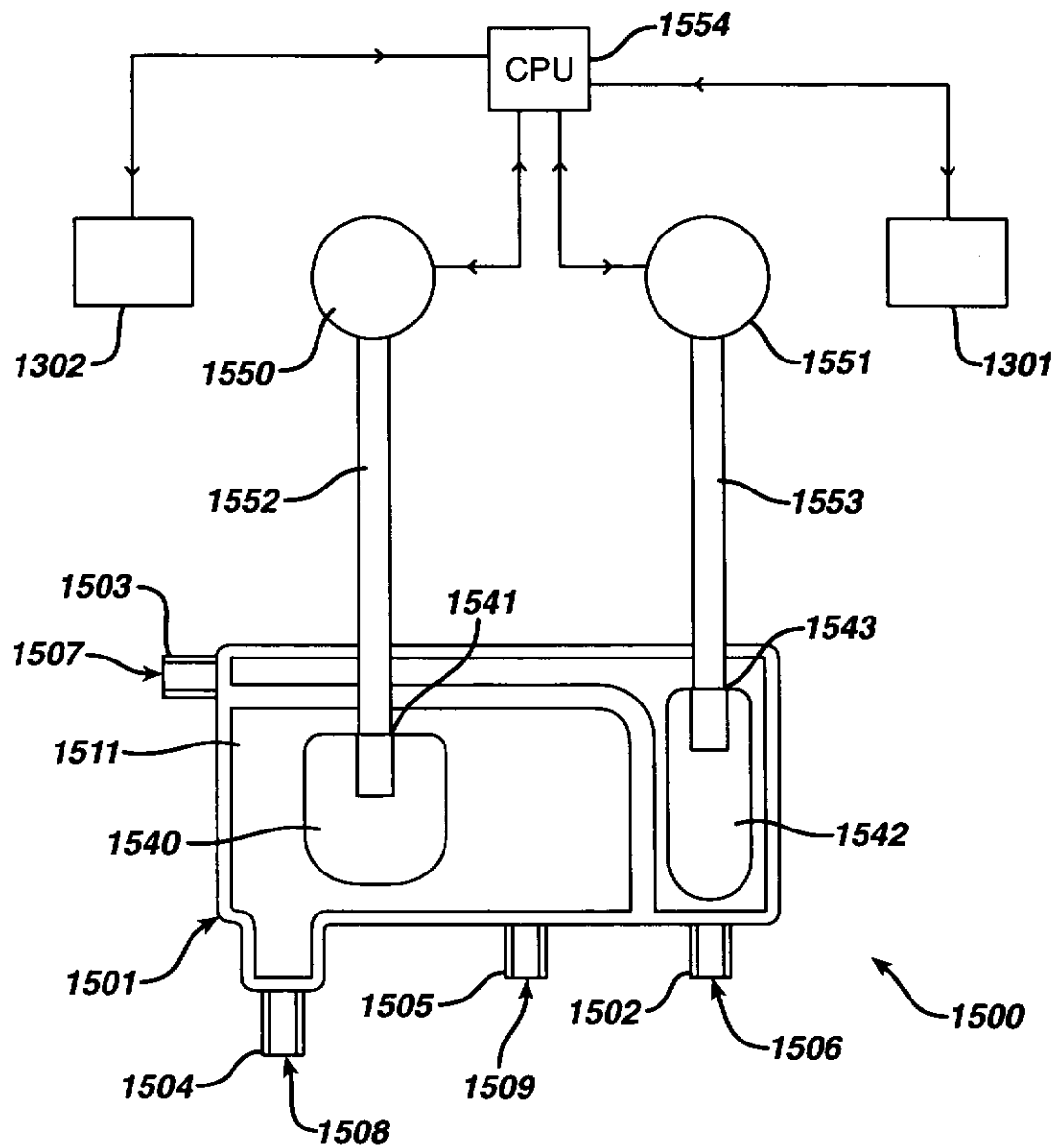
FIG. 10

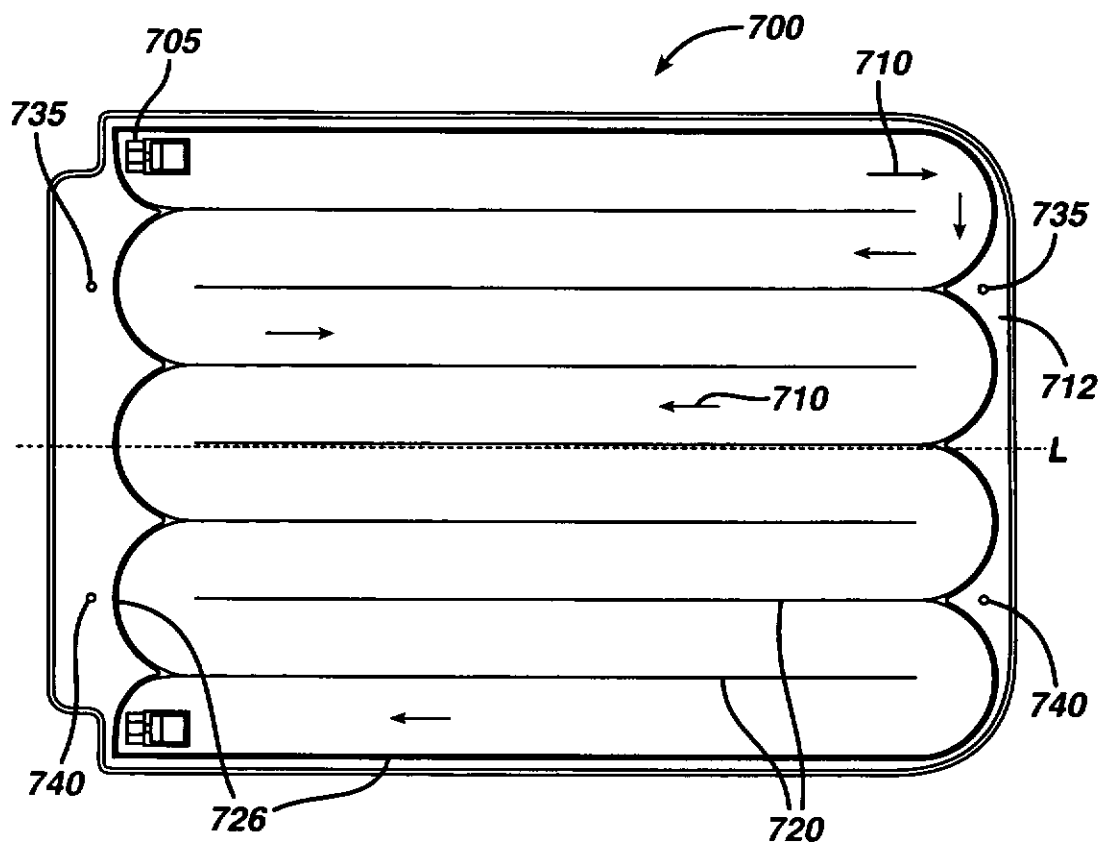
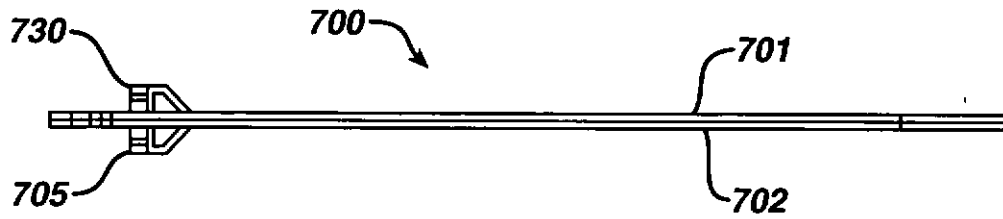
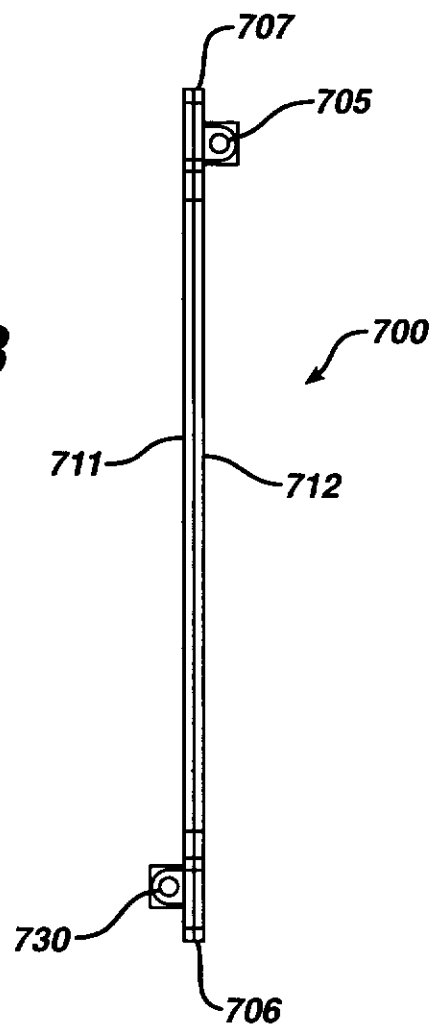
FIG. 11

FIG. 12**FIG. 13**

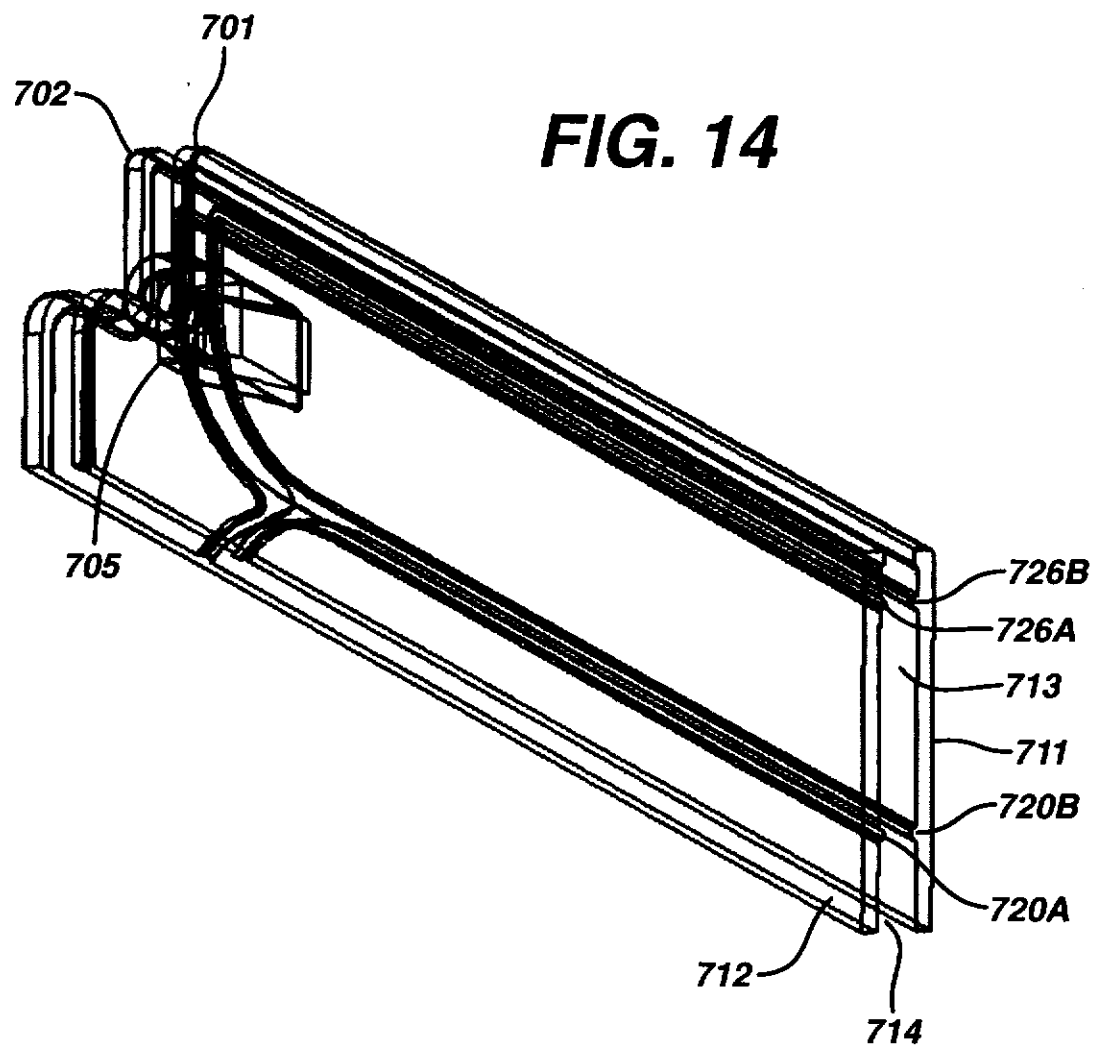


FIG. 15

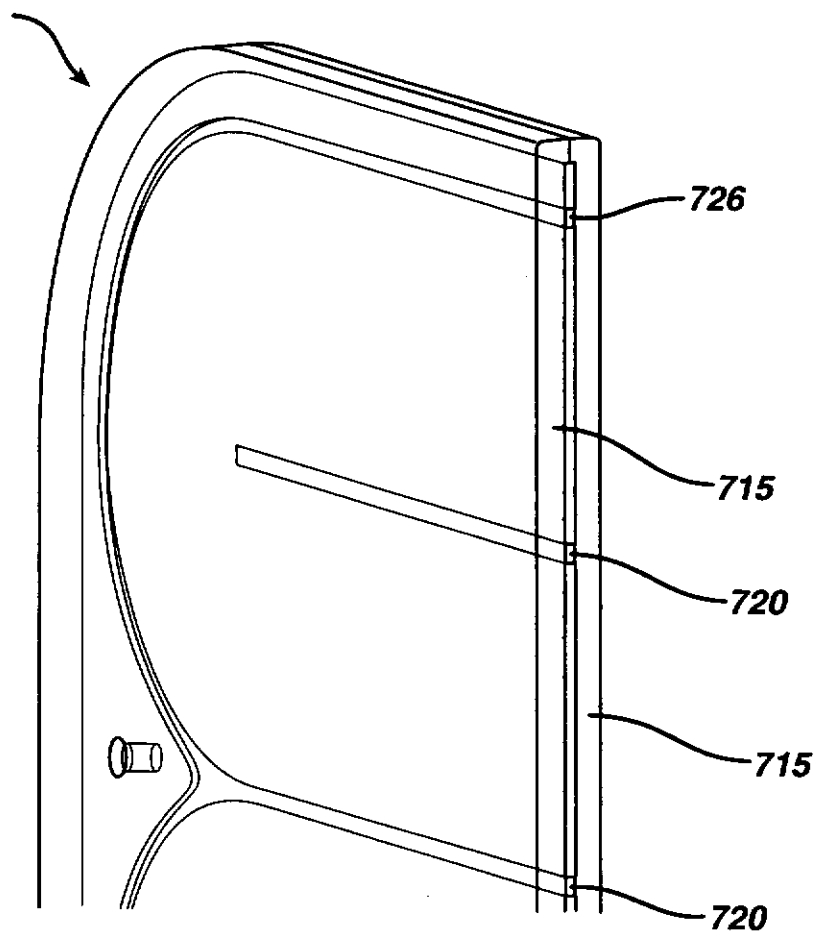
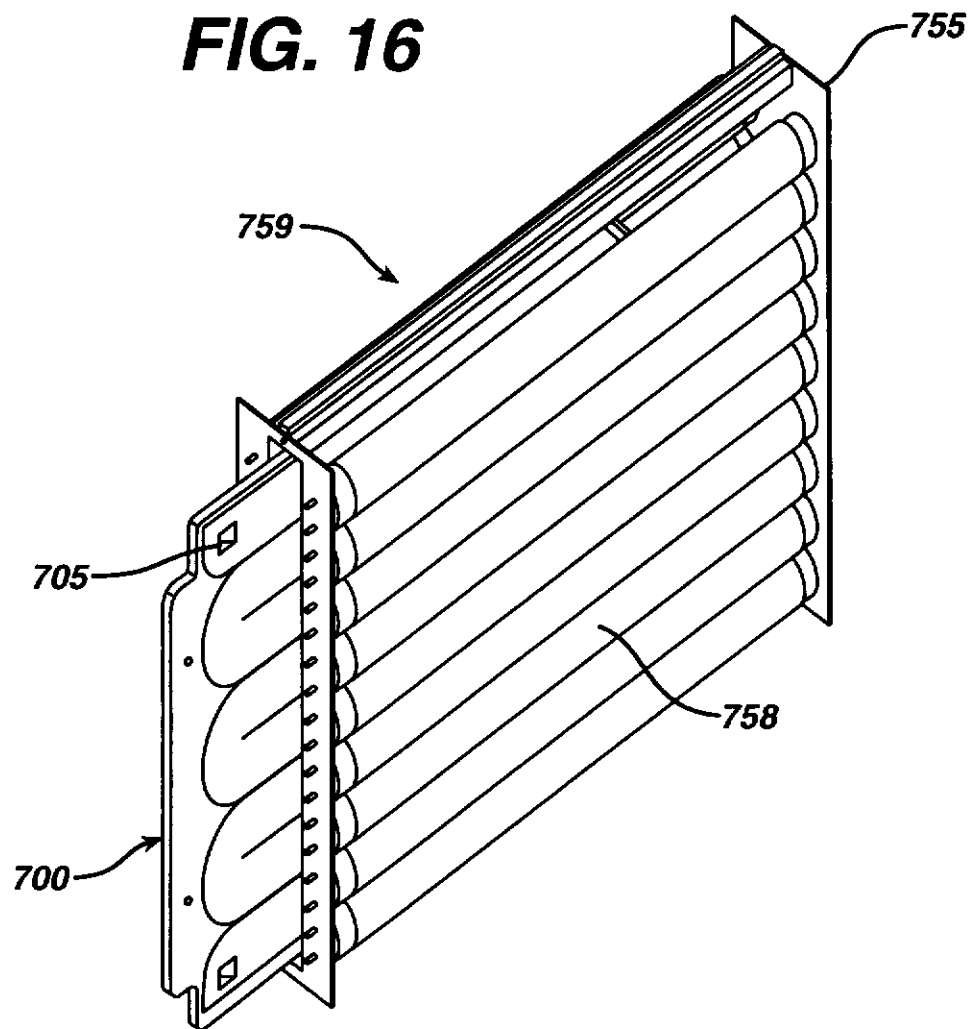


FIG. 16

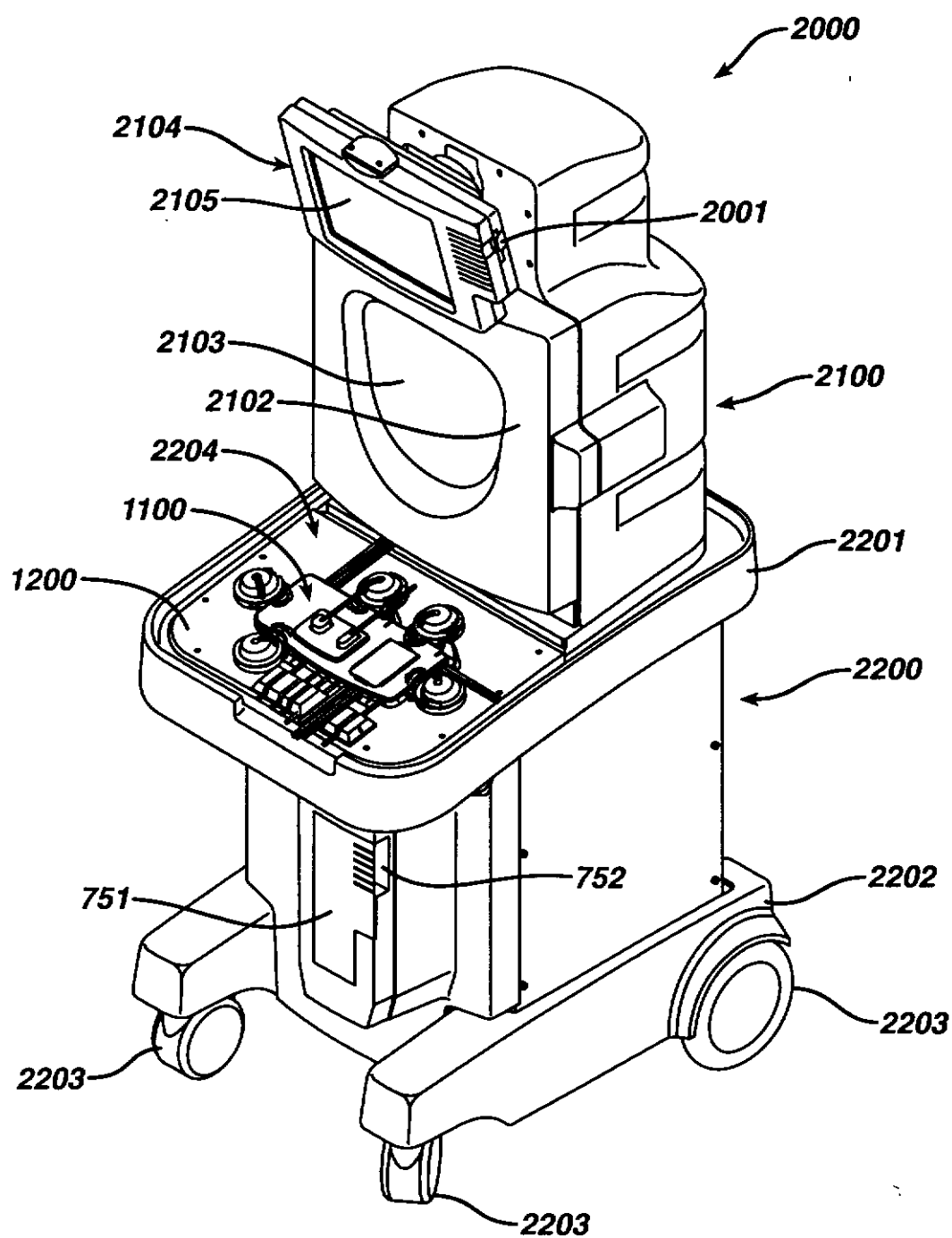


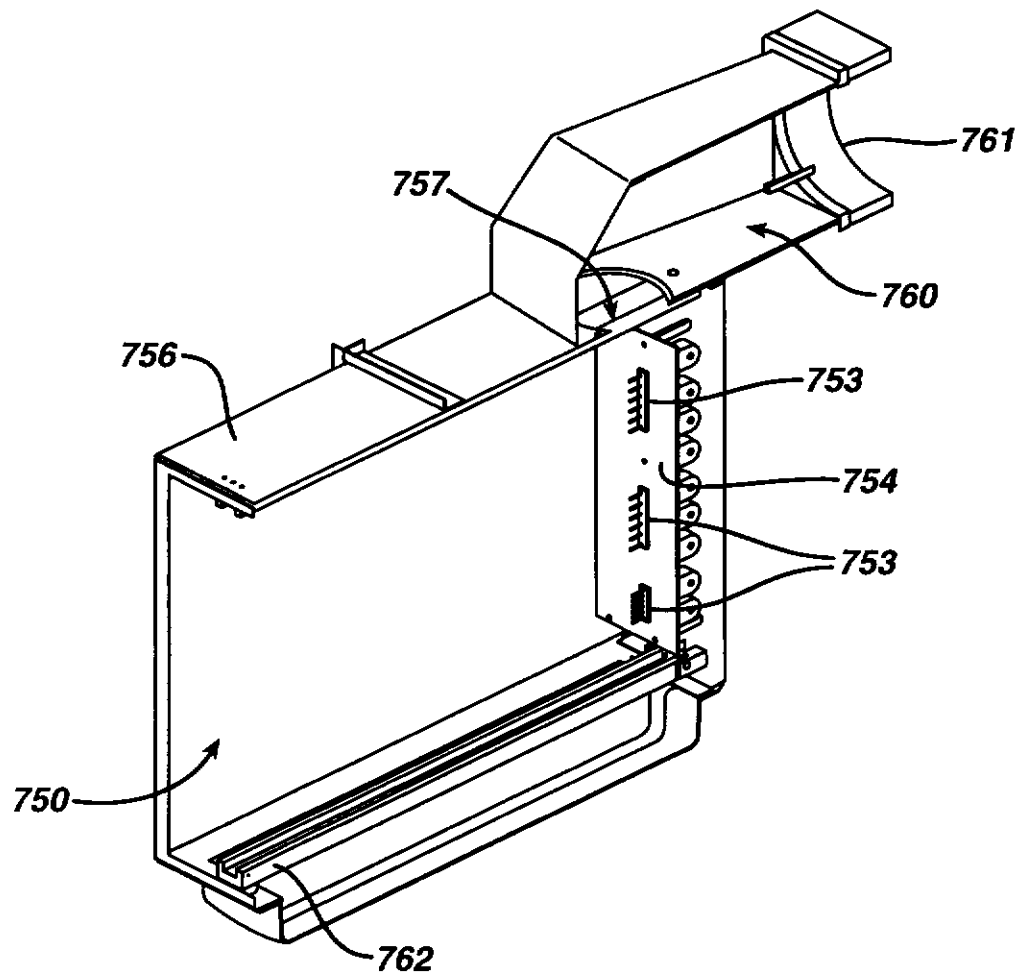
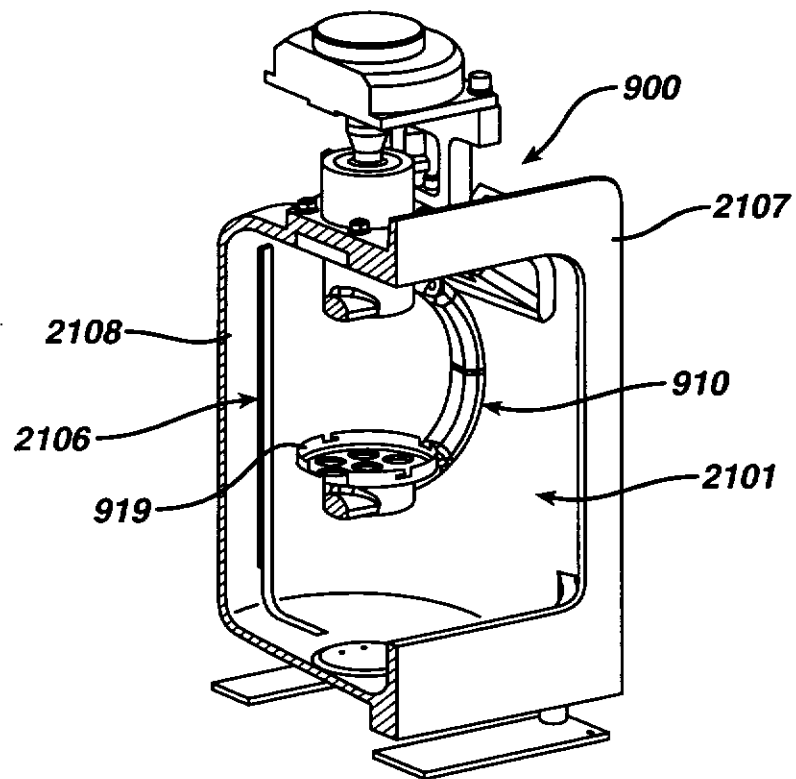
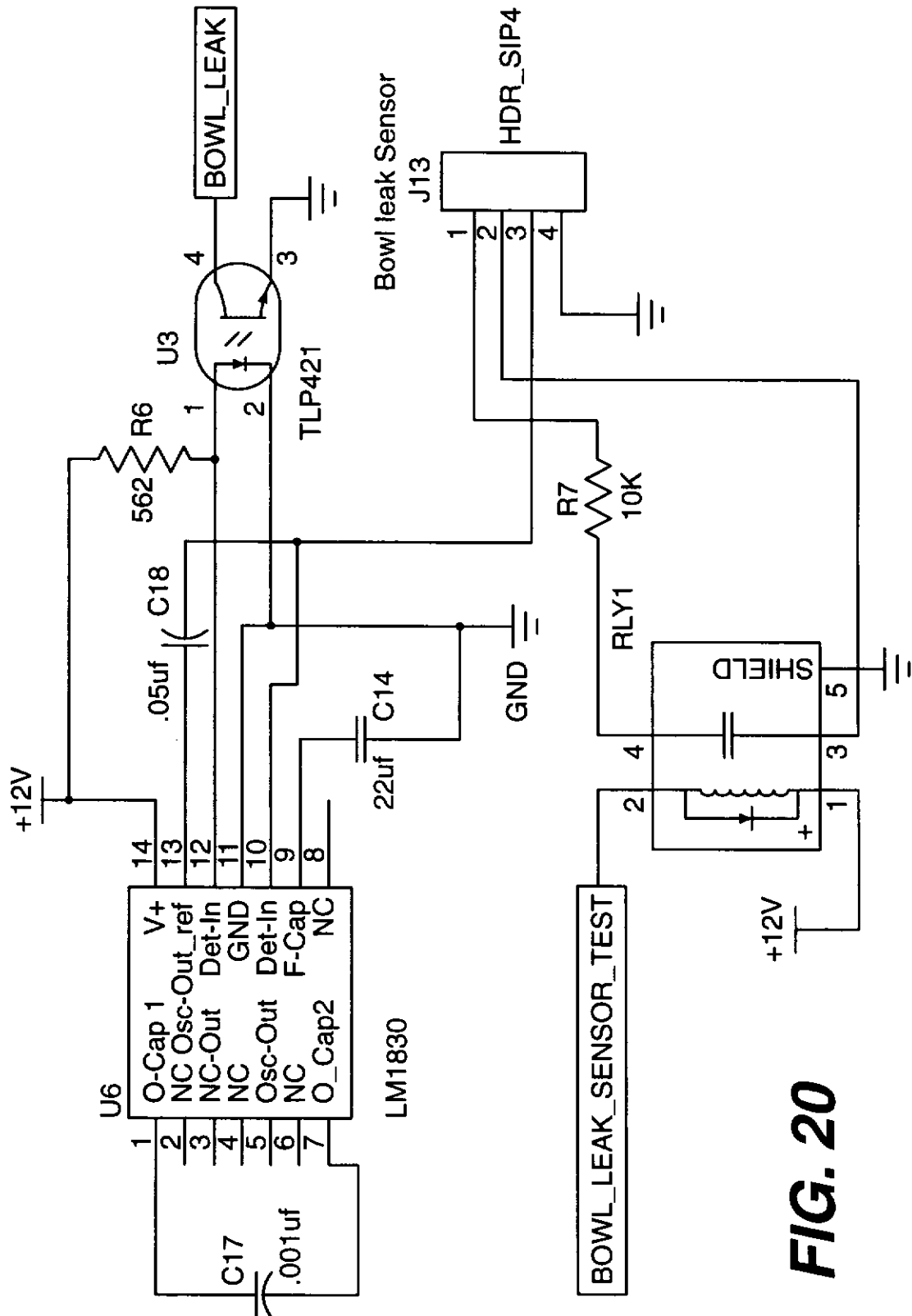
FIG. 18

FIG. 19





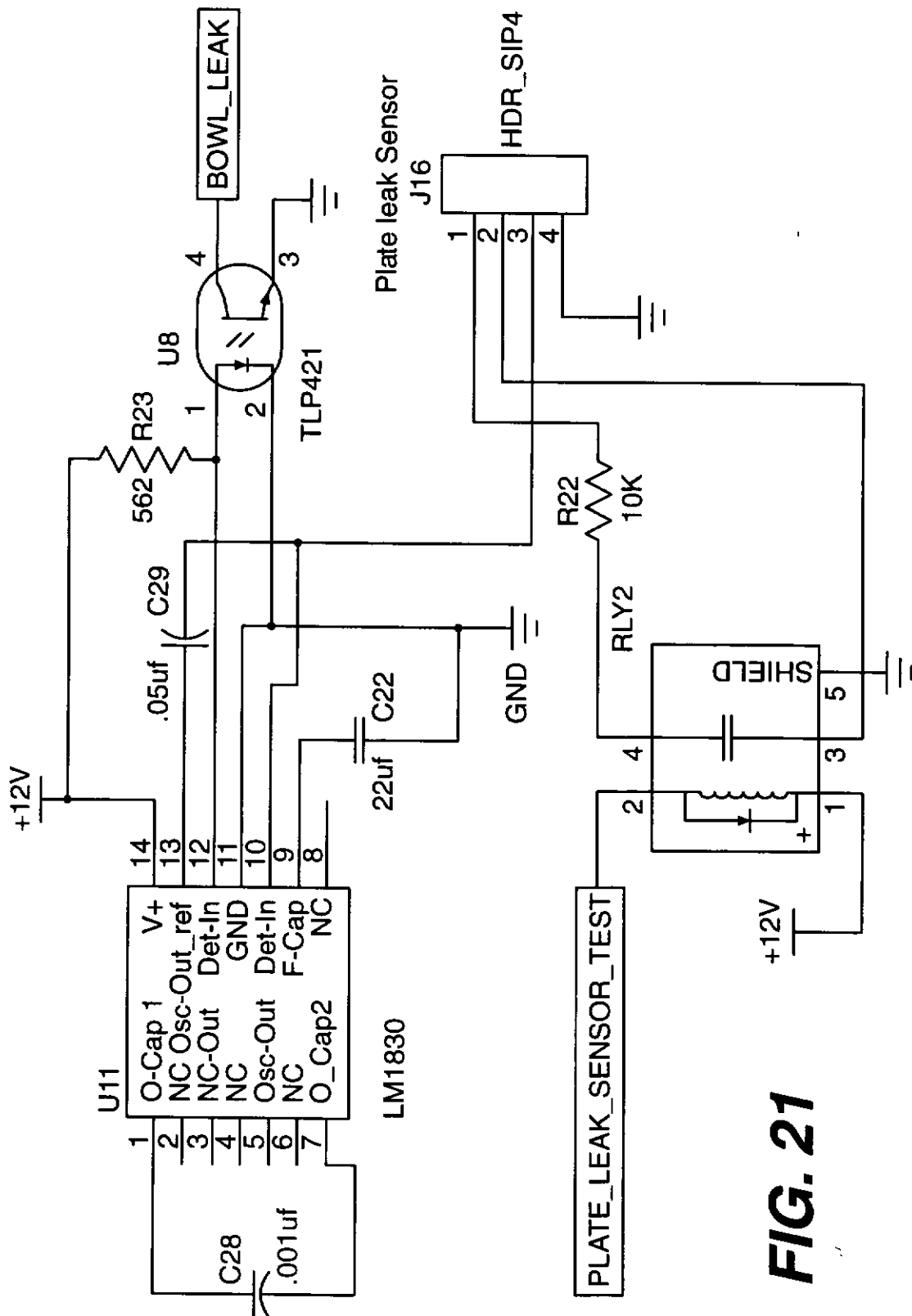


FIG. 21

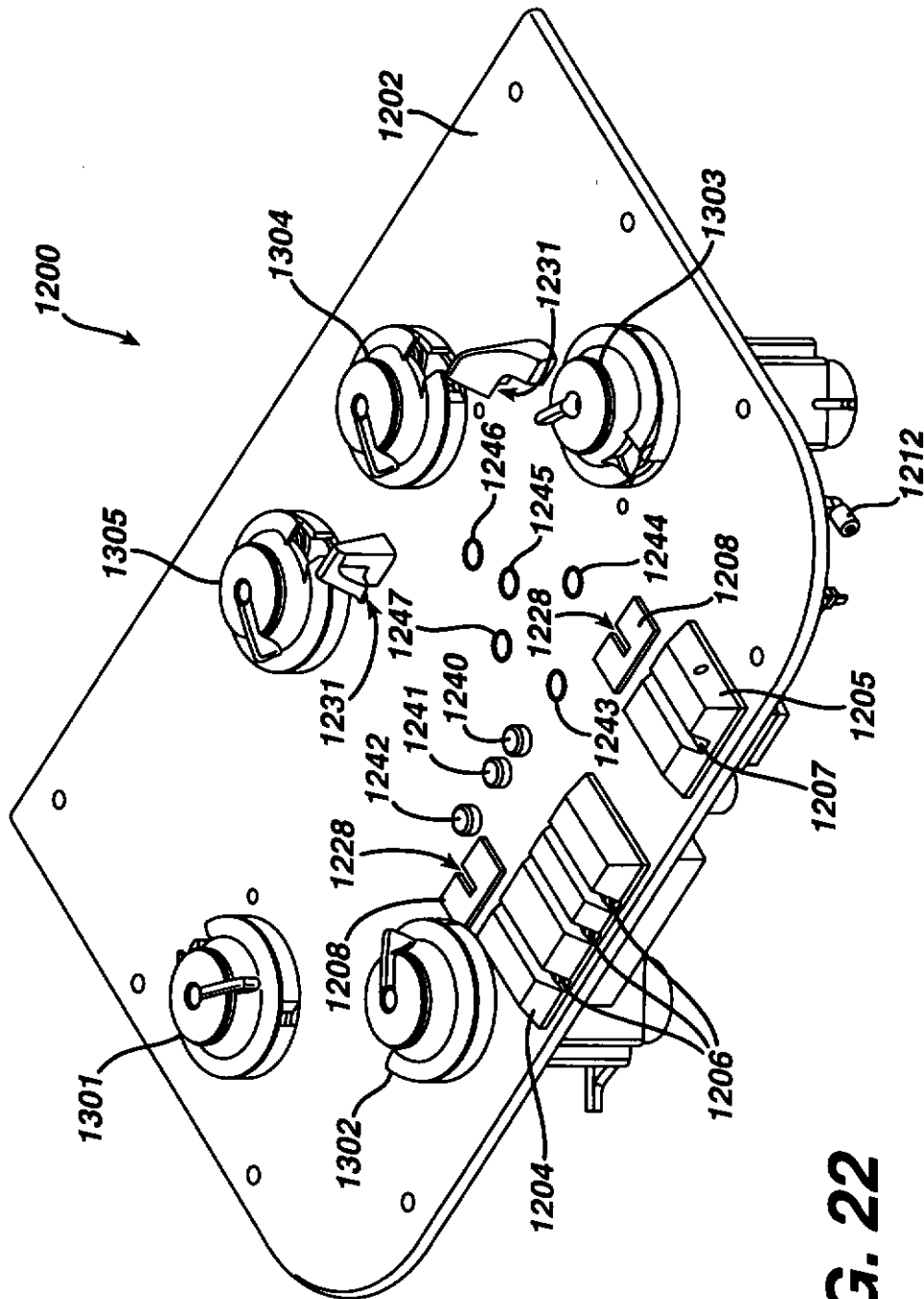


FIG. 22

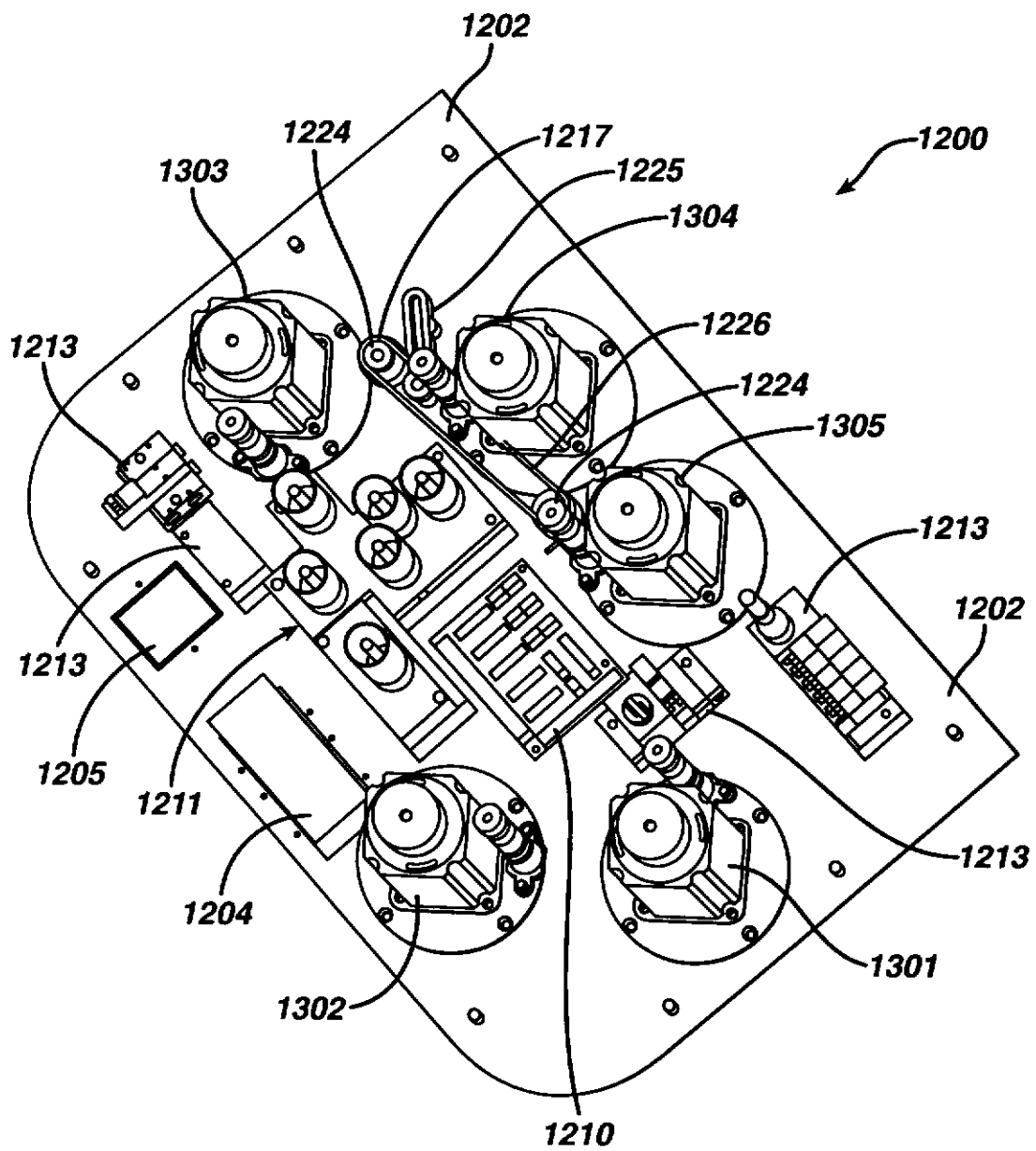
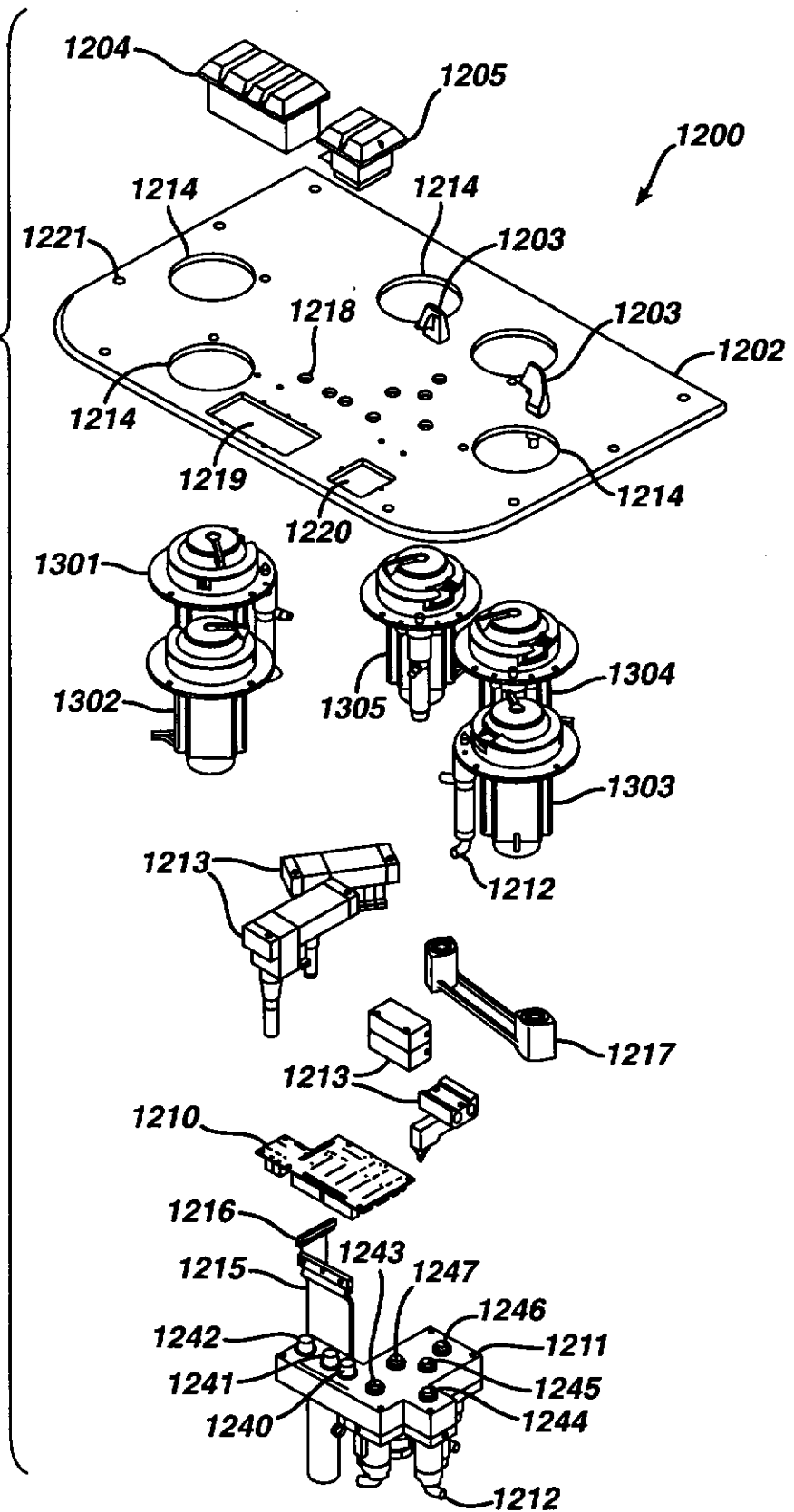
FIG. 23

FIG. 24

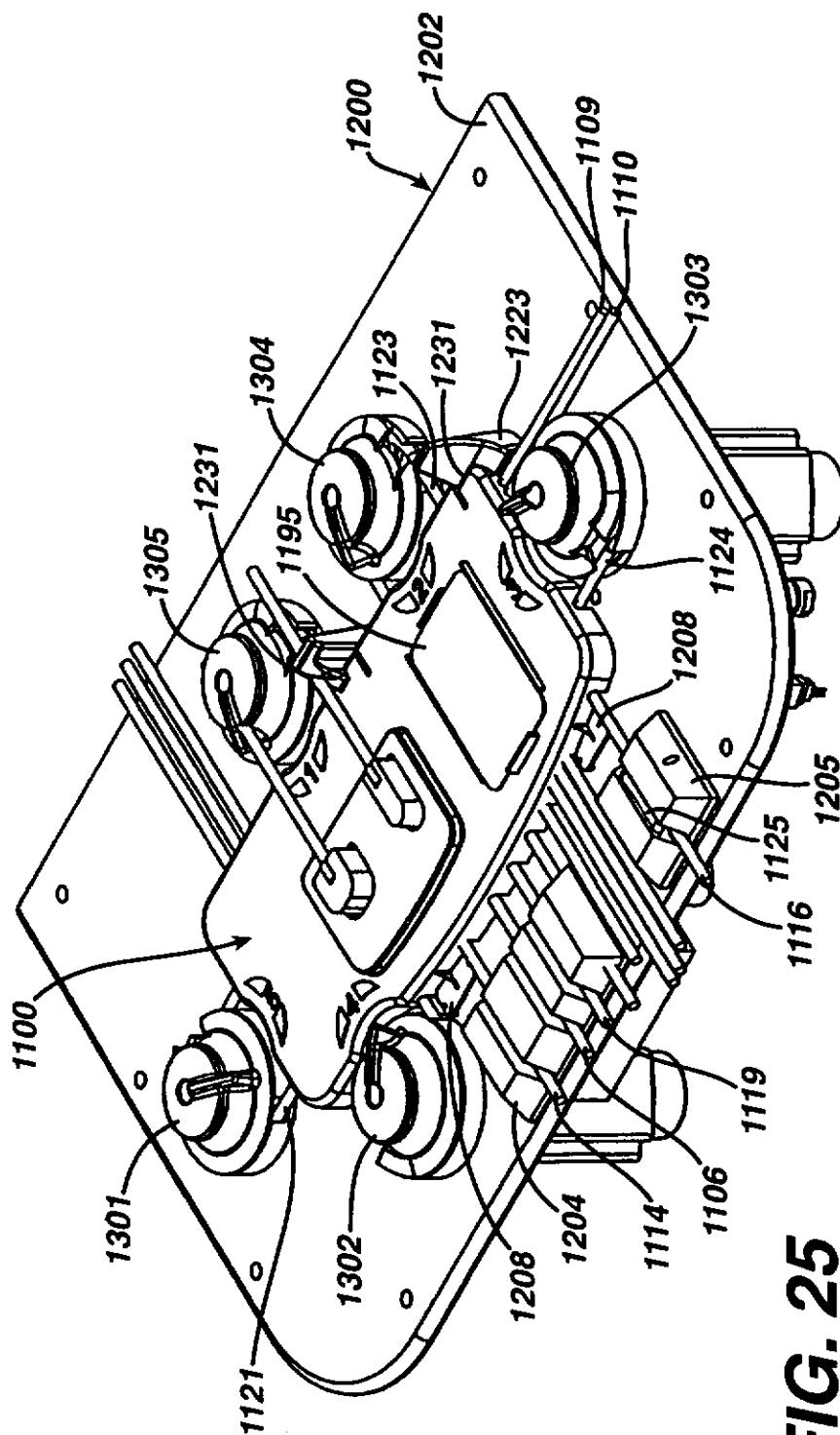
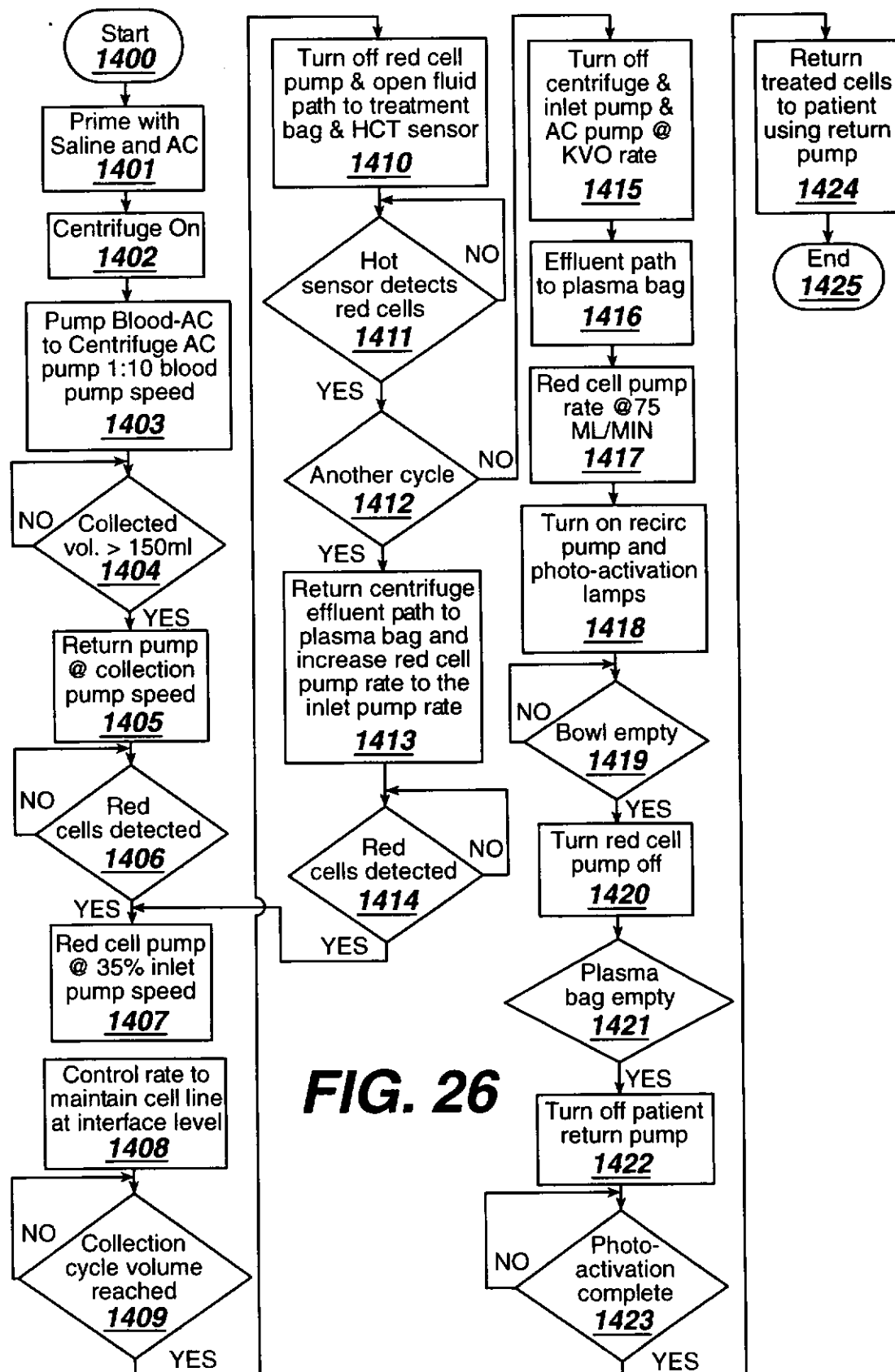


FIG. 25



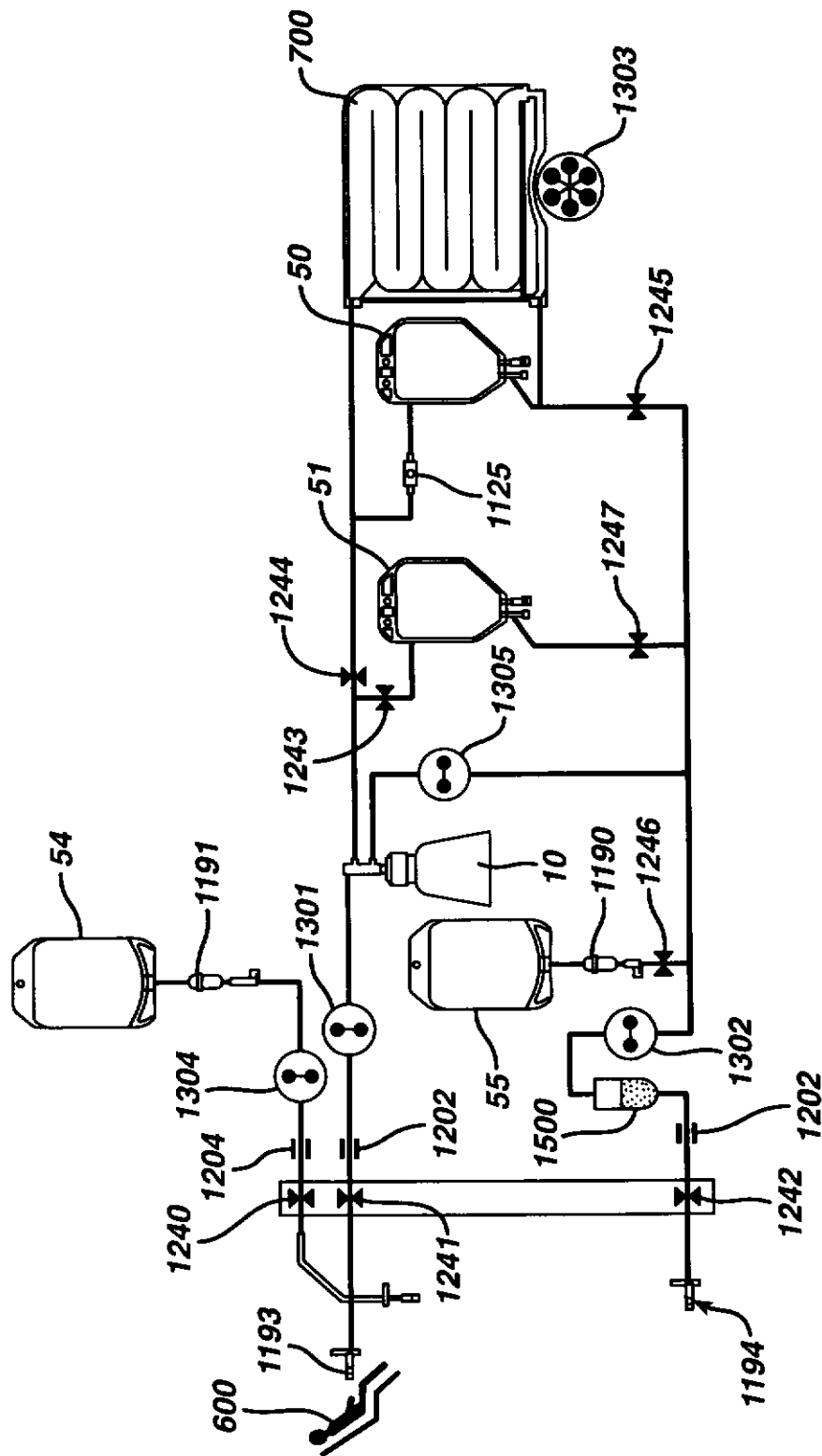


FIG. 27

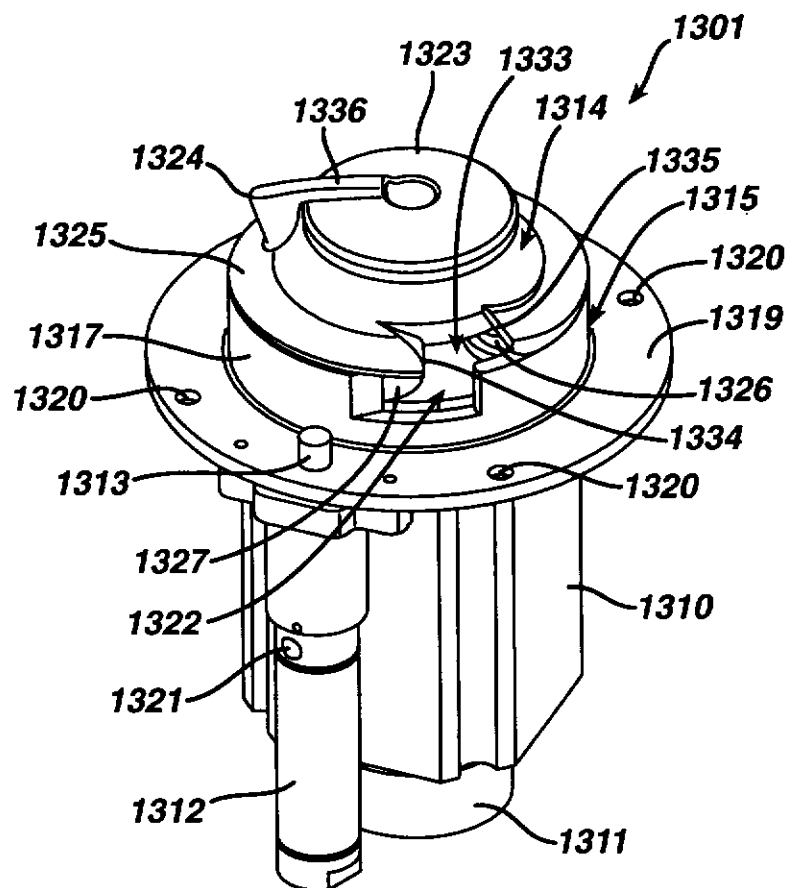
FIG. 28

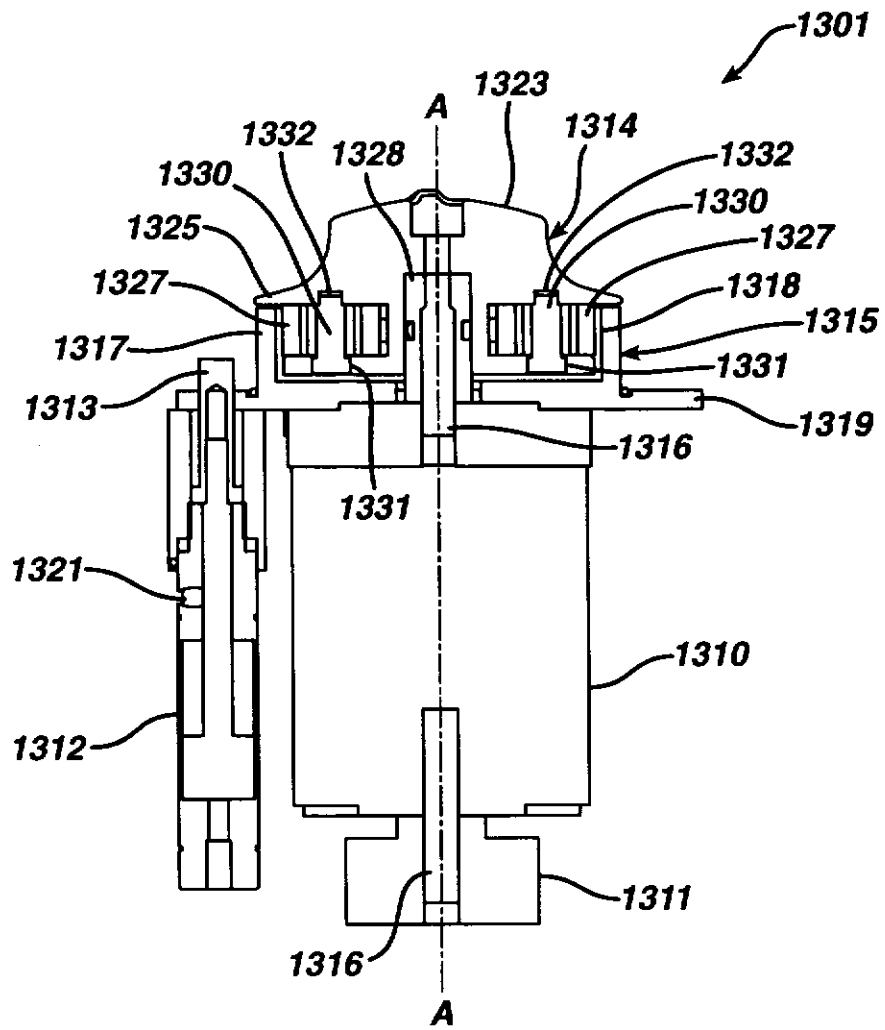
FIG. 29

FIG. 30

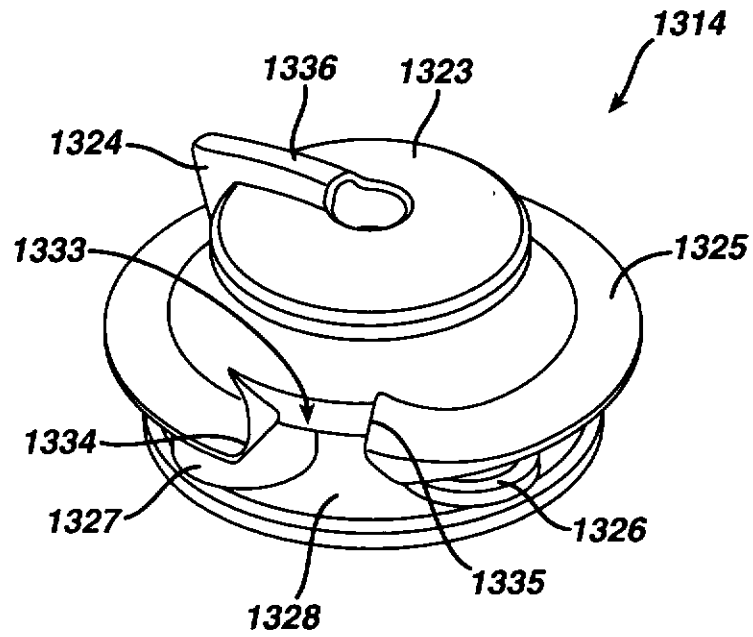


FIG. 31

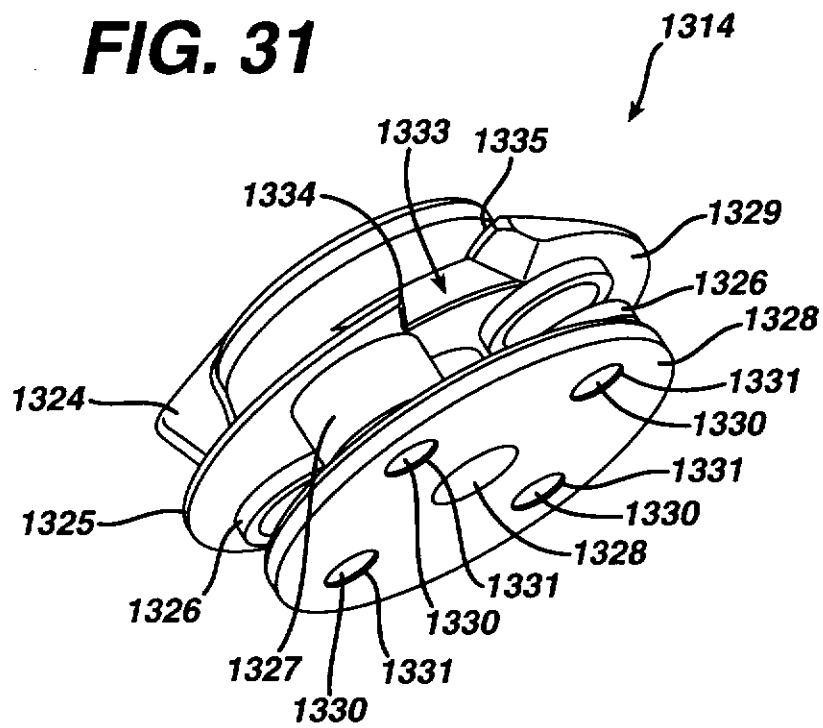


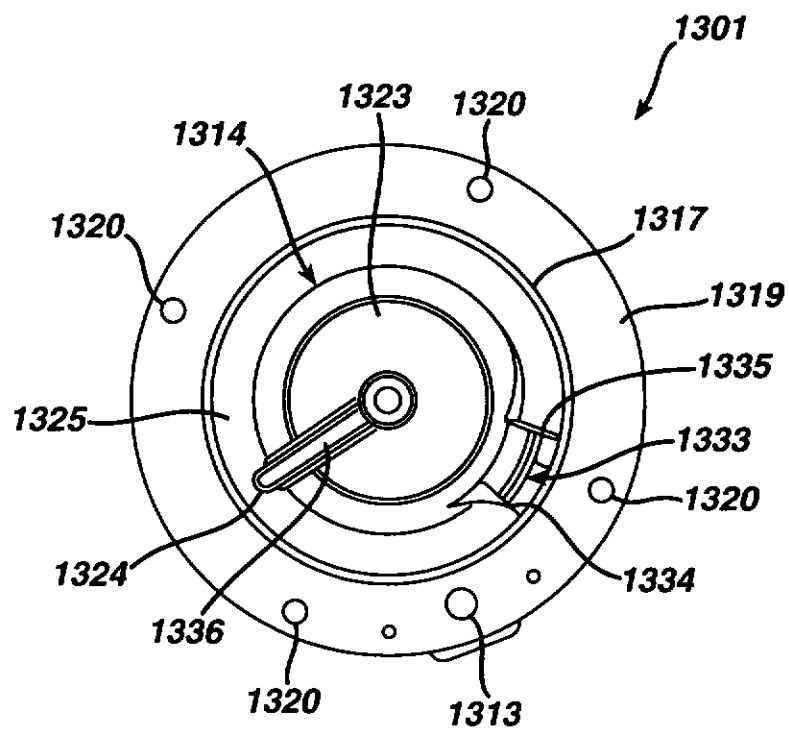
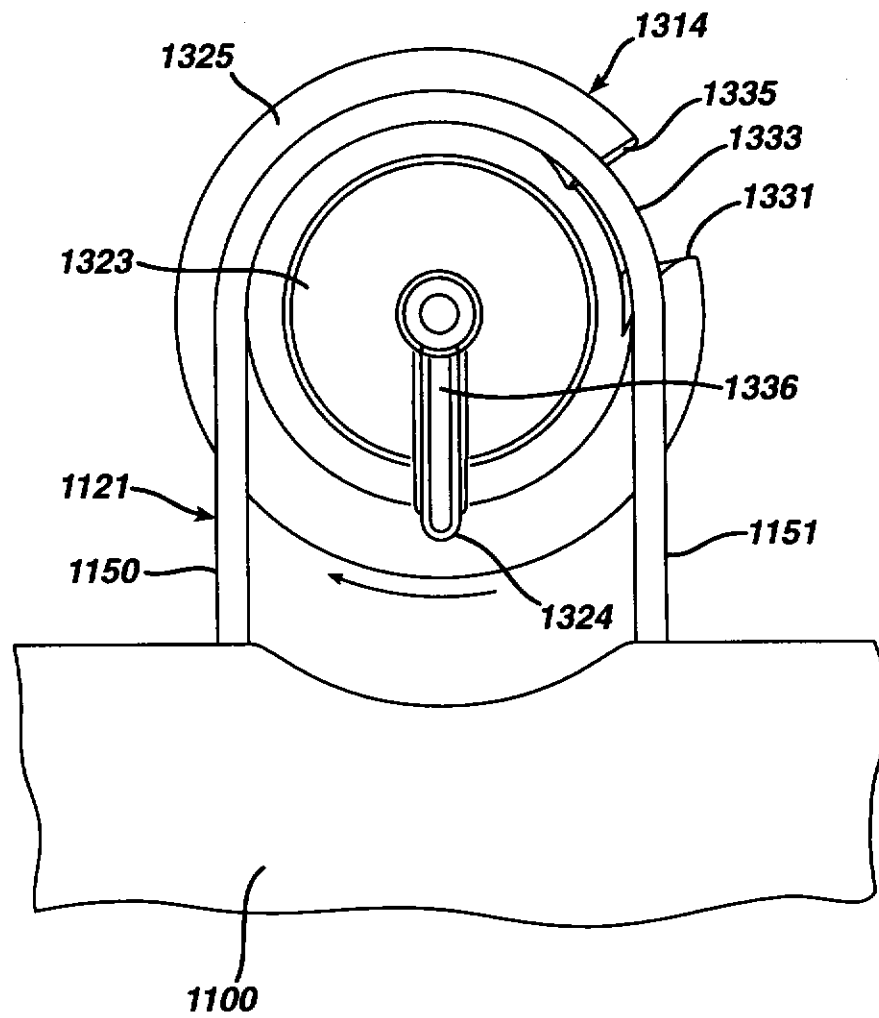
FIG. 32

FIG. 33

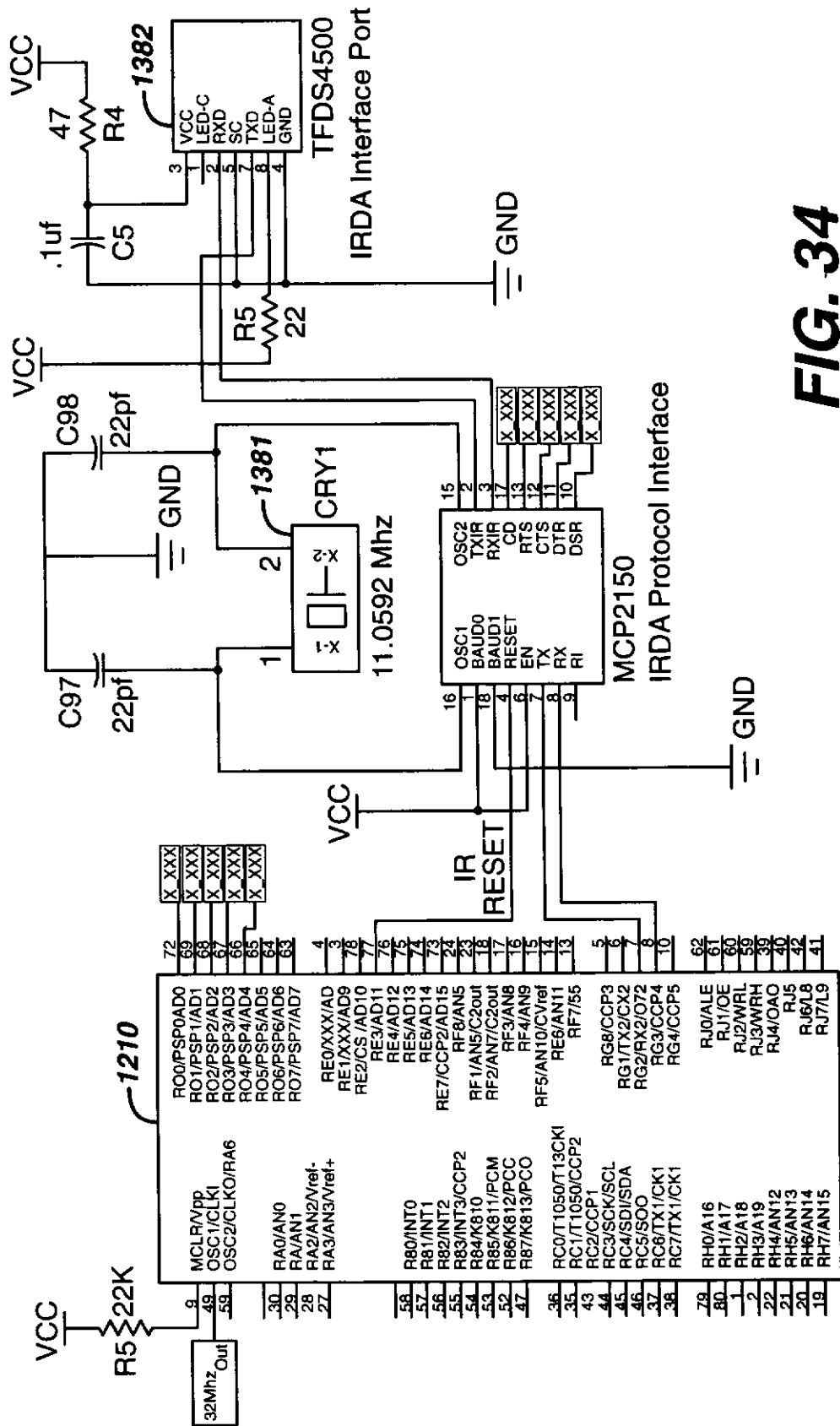


FIG. 34

System CPU

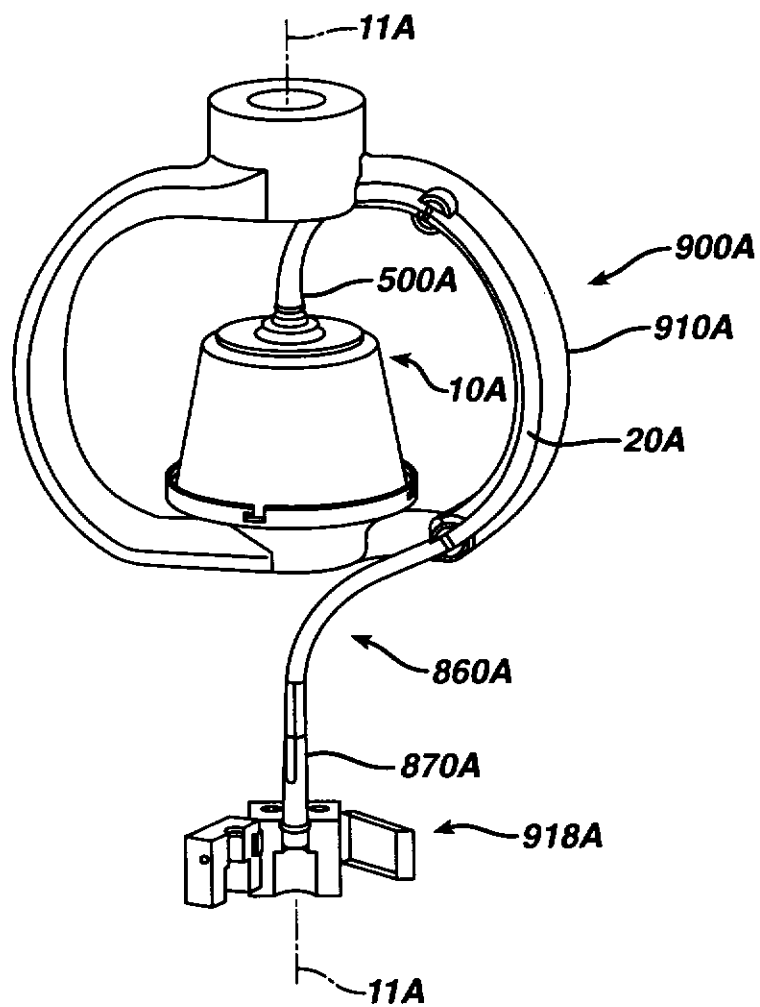
FIG. 35

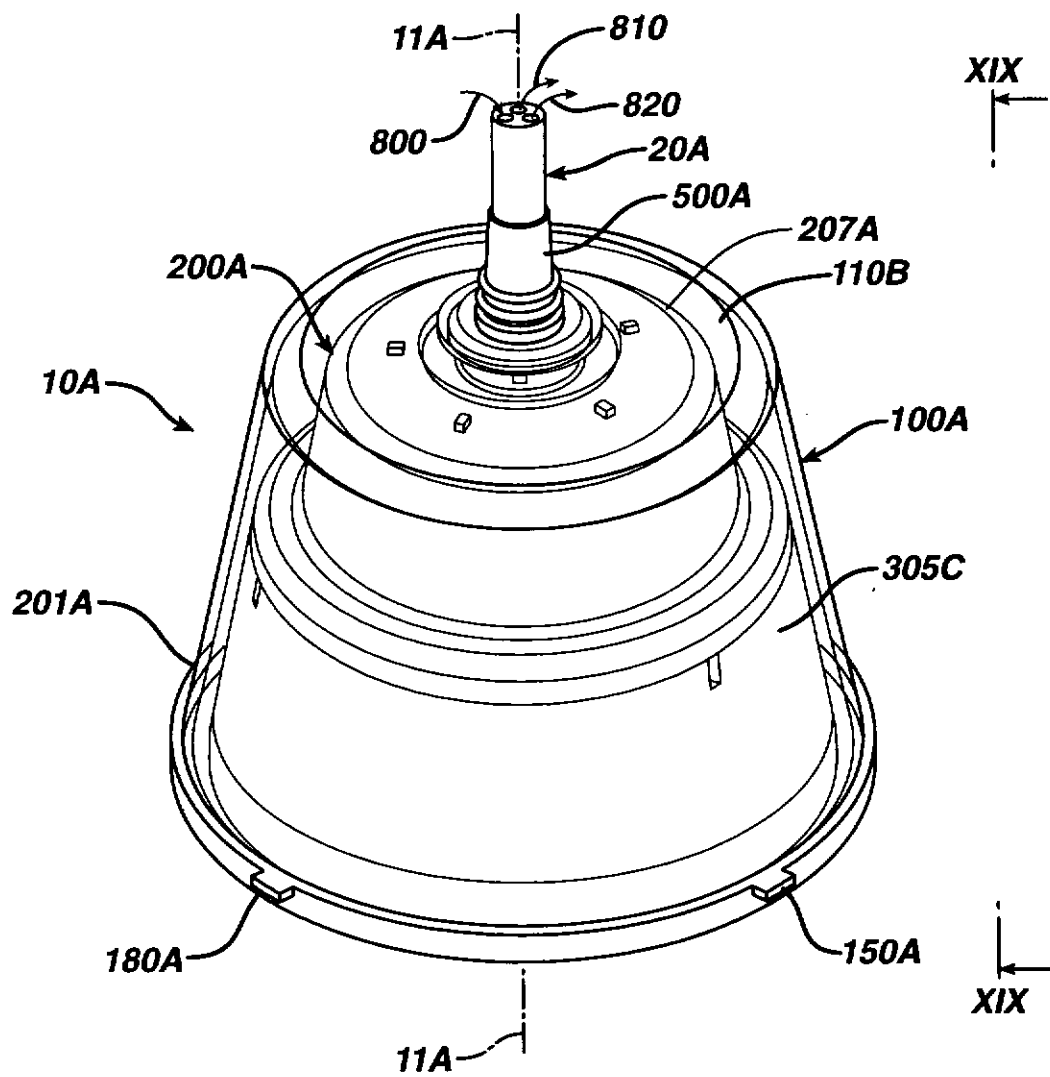
FIG. 36

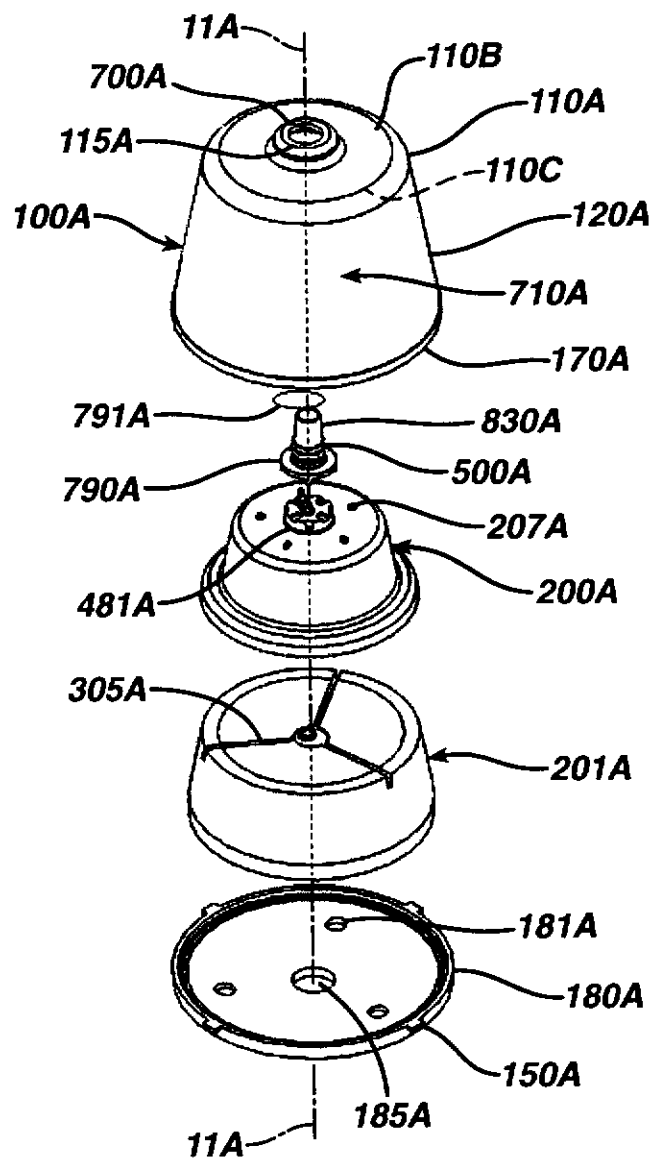
FIG. 37

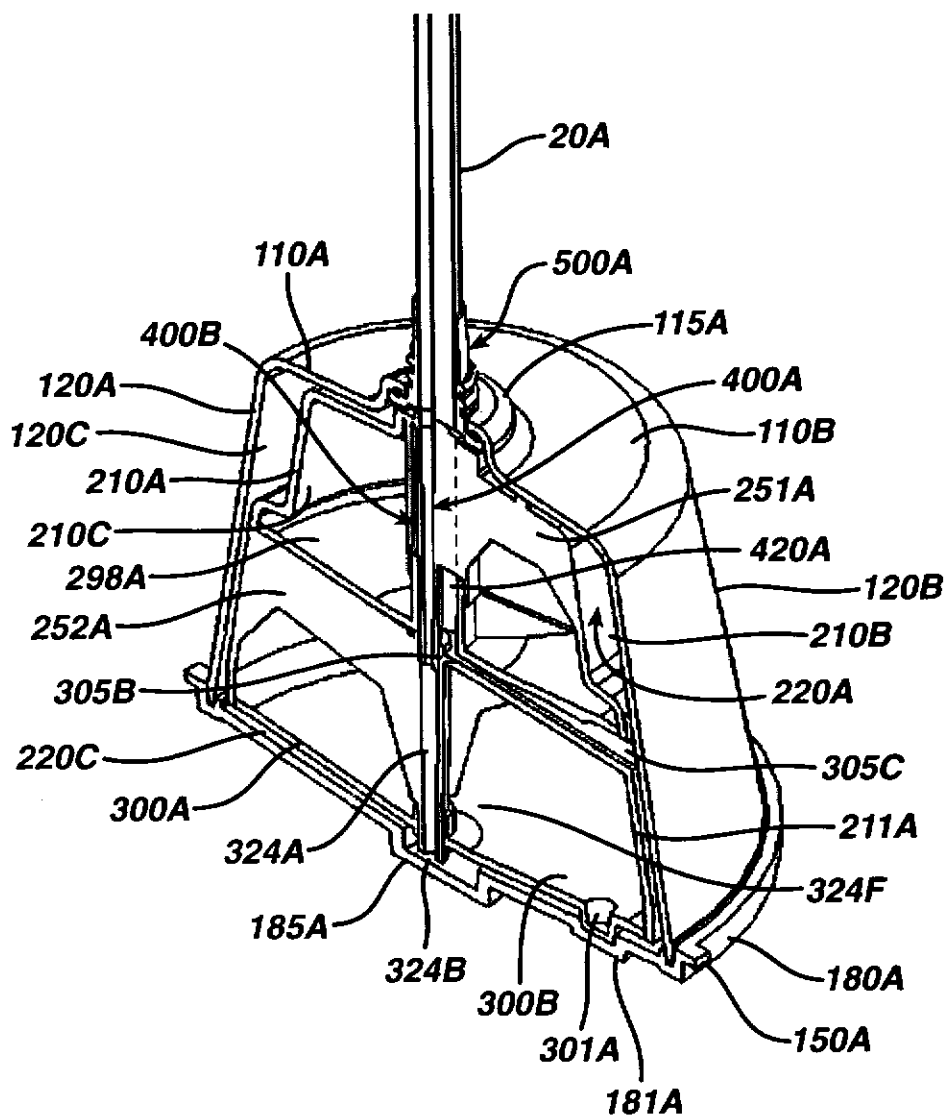
FIG. 38

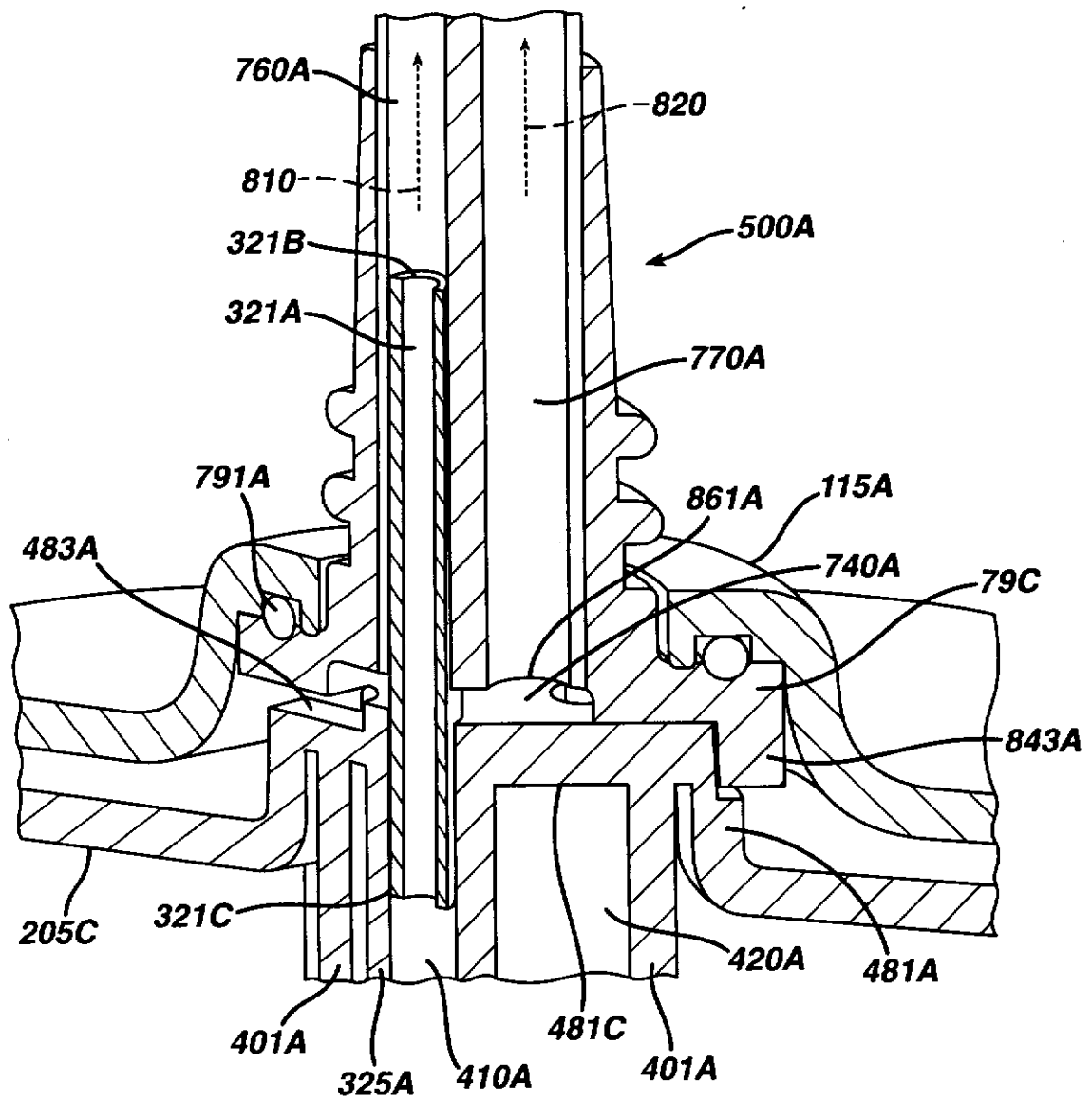
FIG. 39A

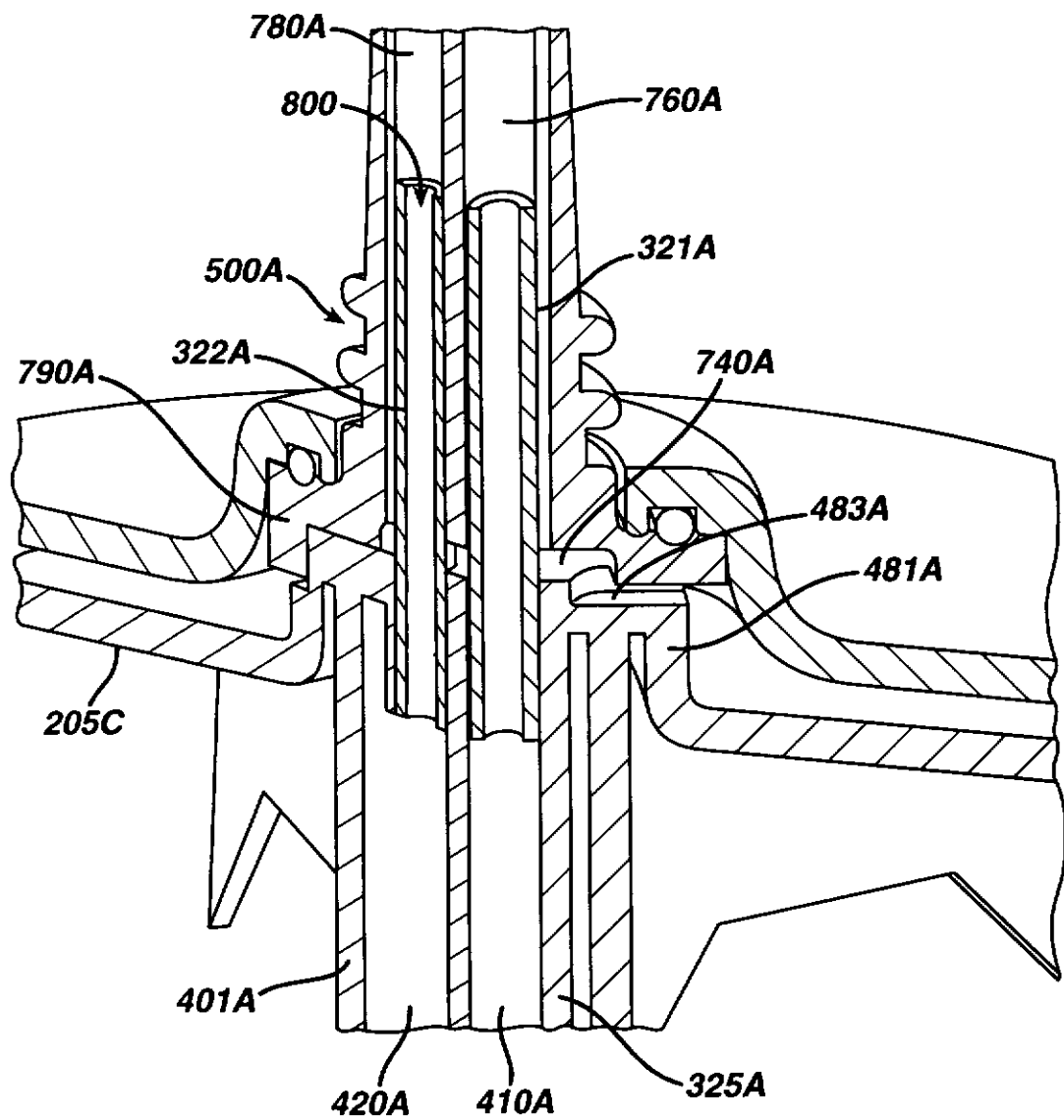
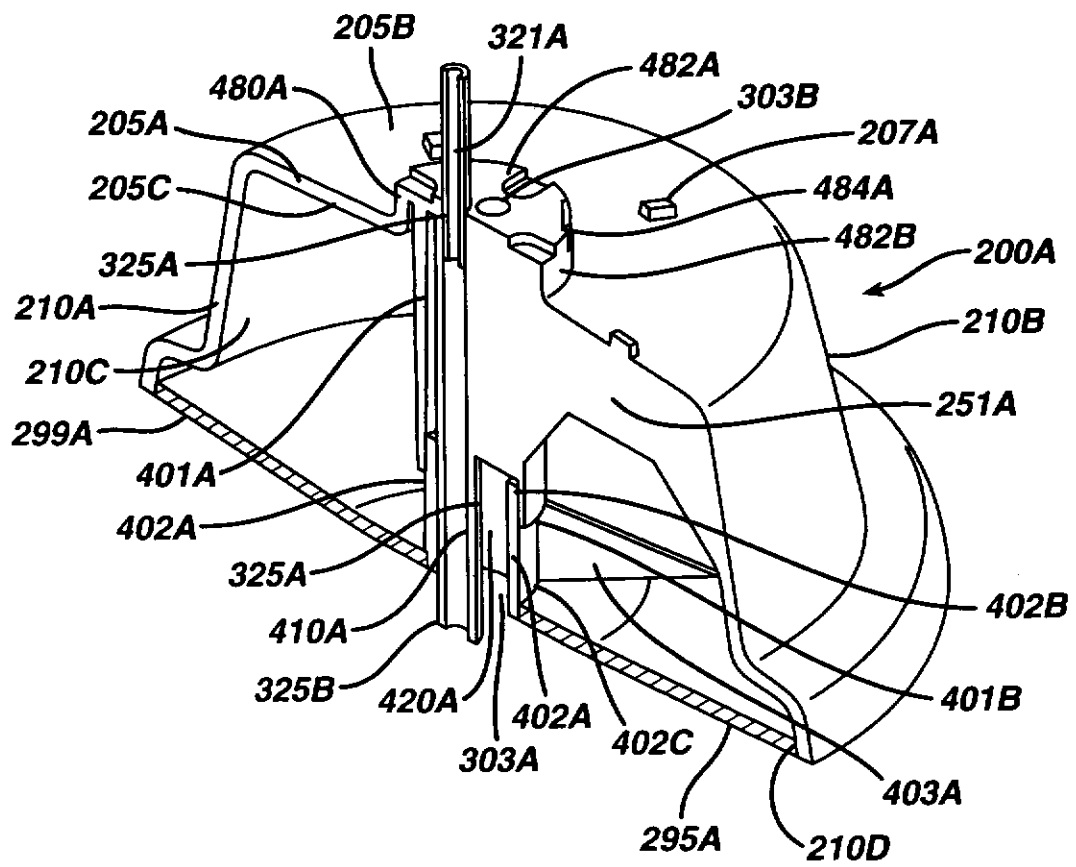
FIG. 39B

FIG. 40

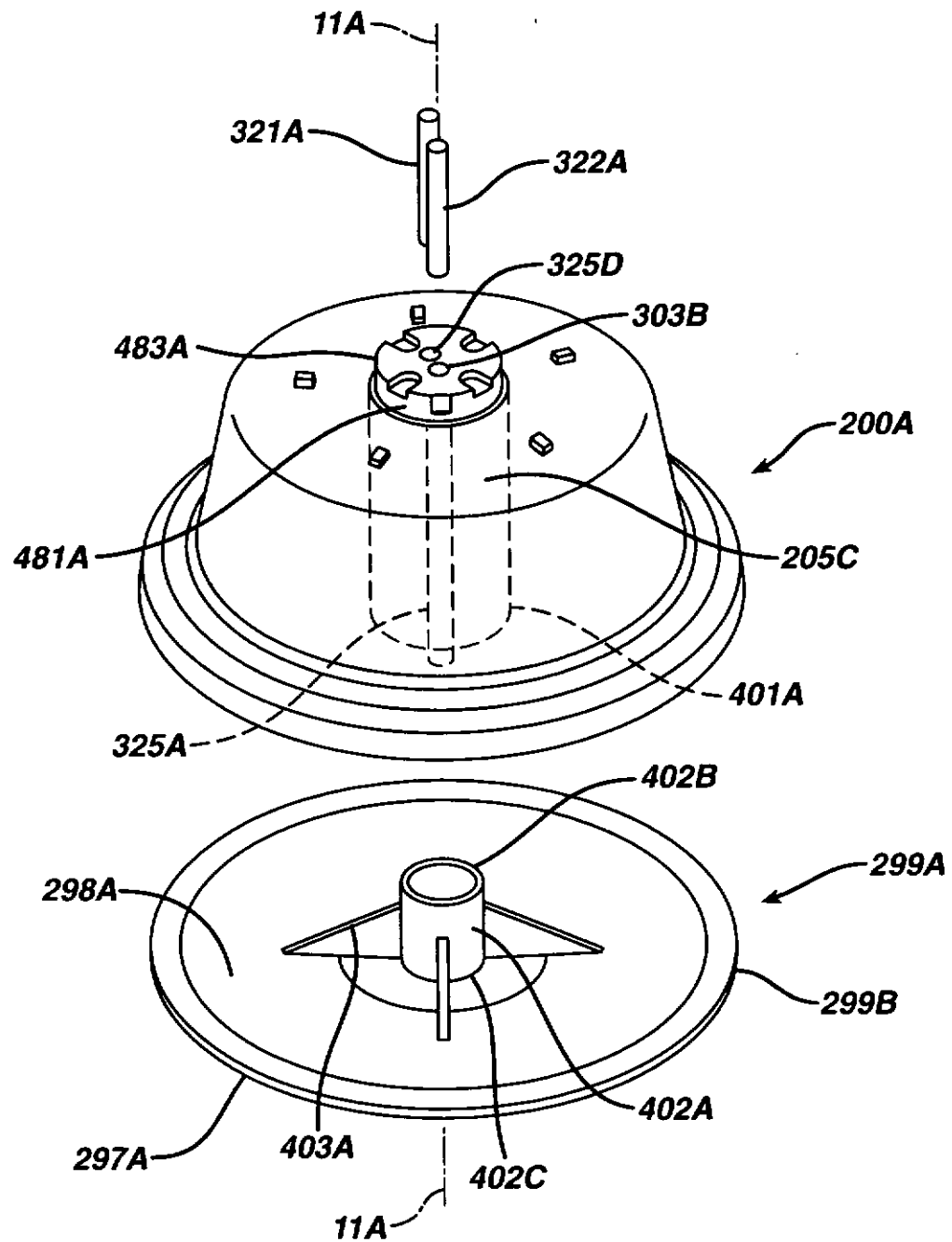


FIG. 42

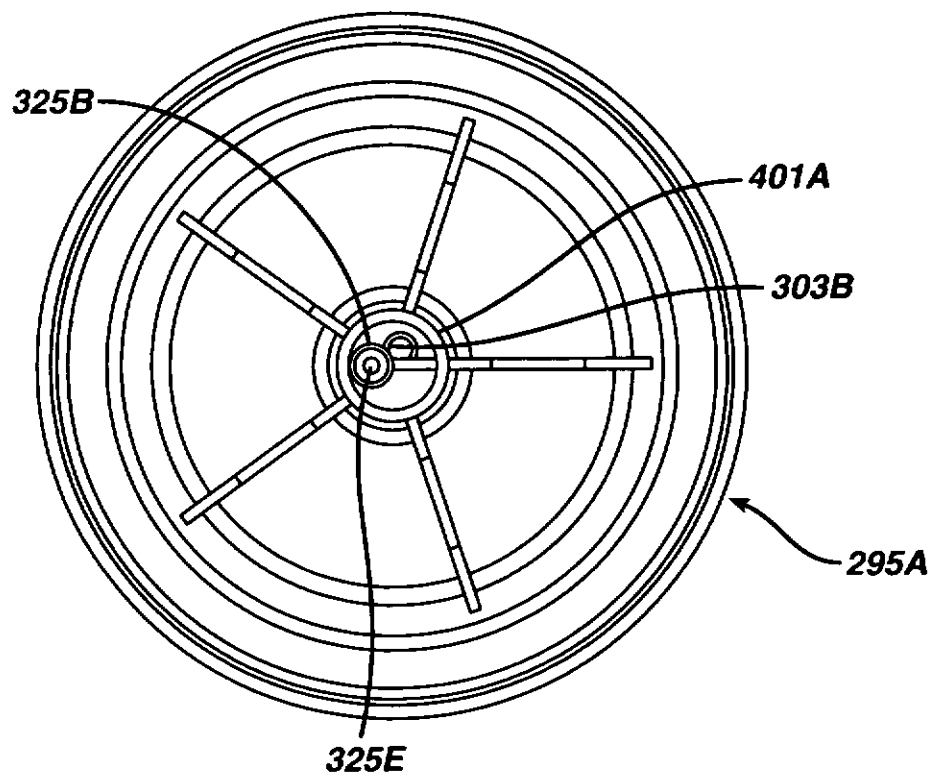
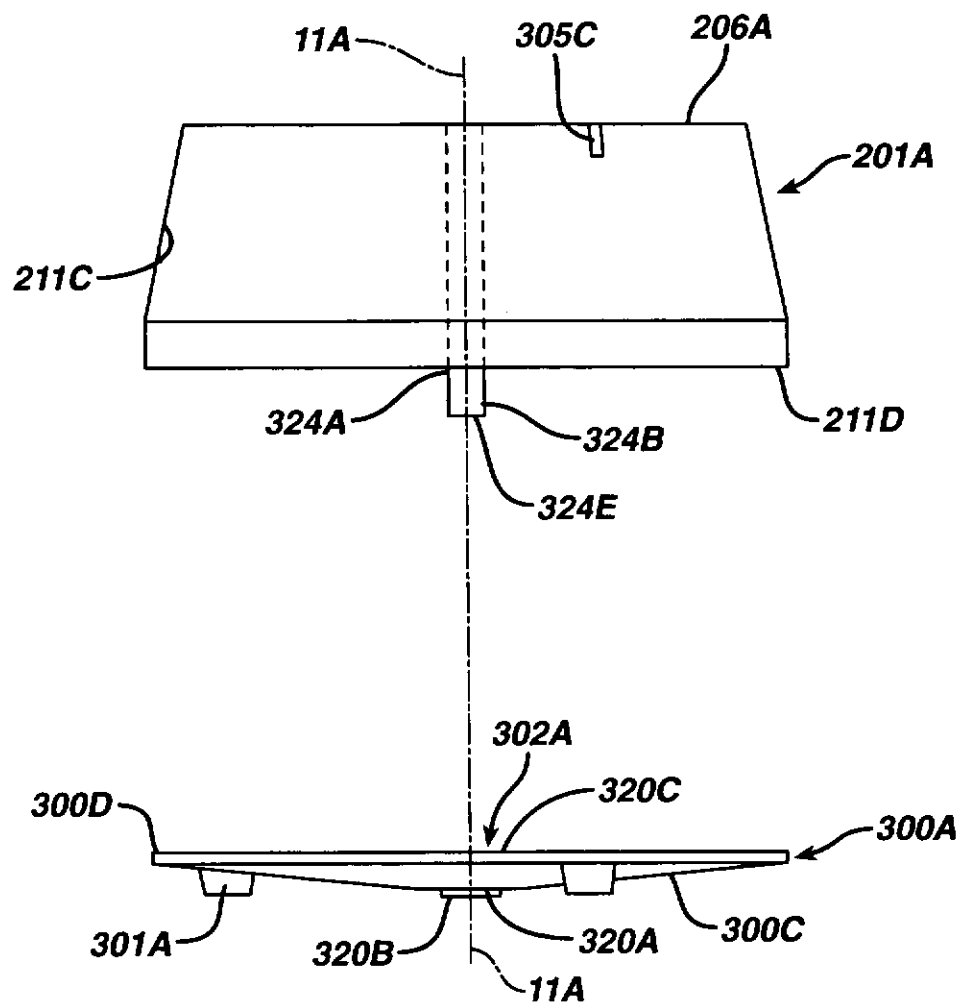


FIG. 44

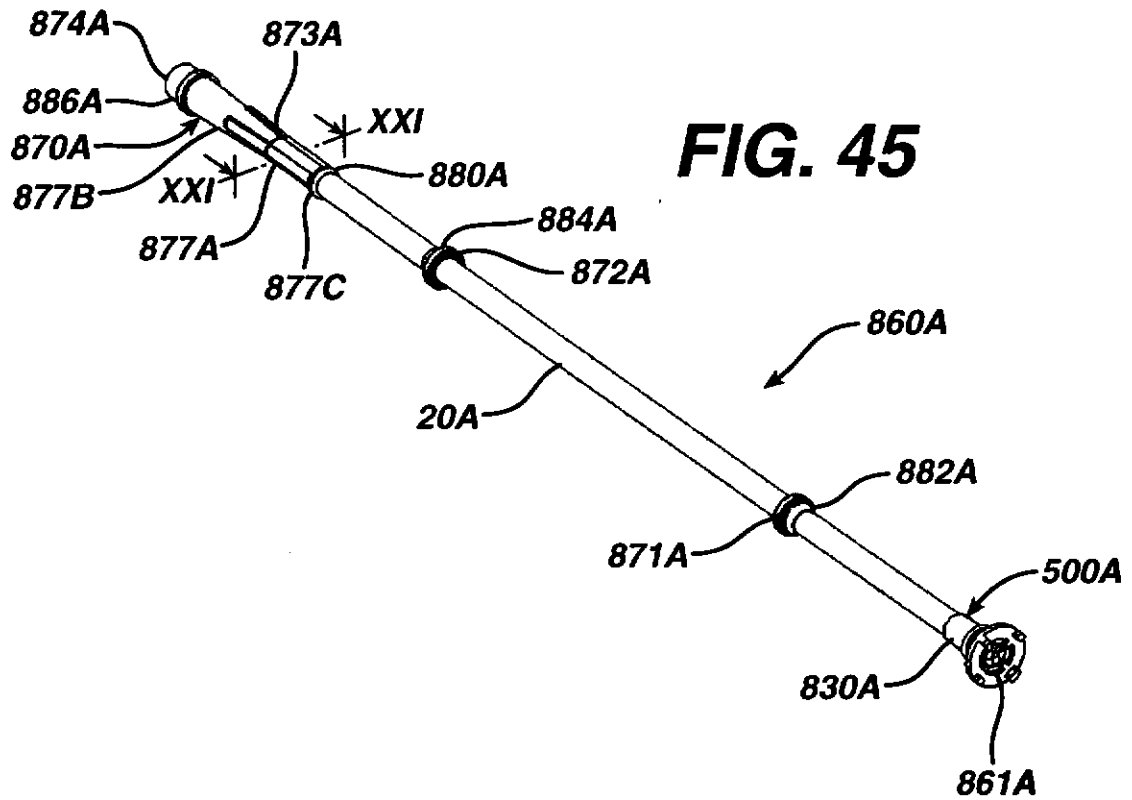


FIG. 46

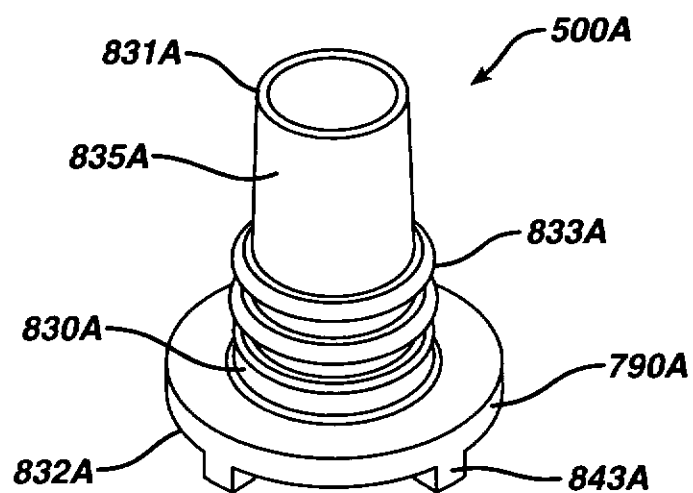


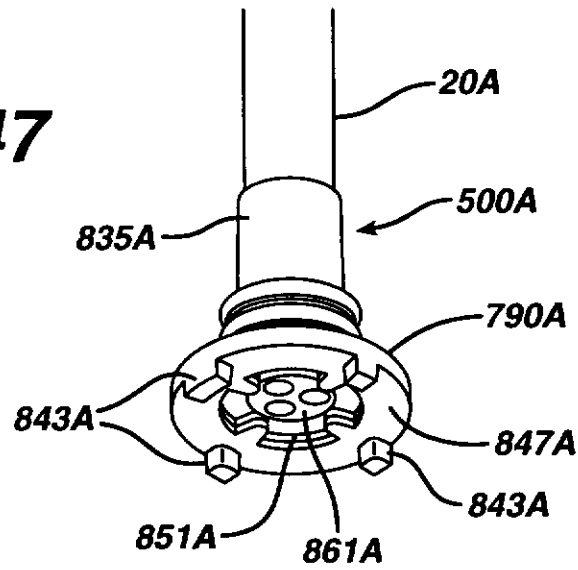
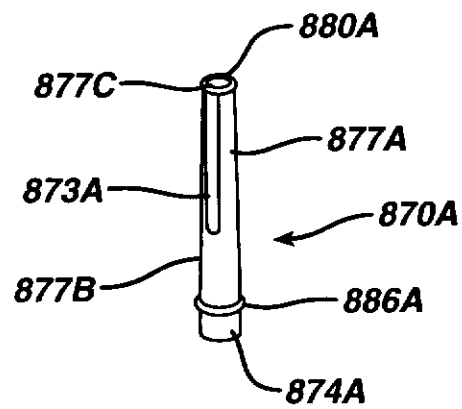
FIG. 47**FIG. 48**

FIG. 49

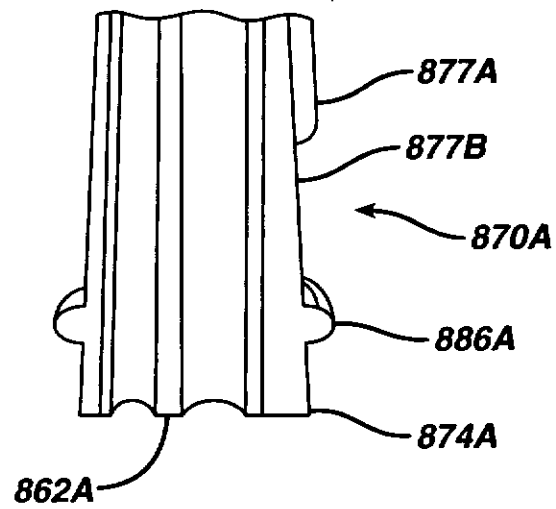


FIG. 50

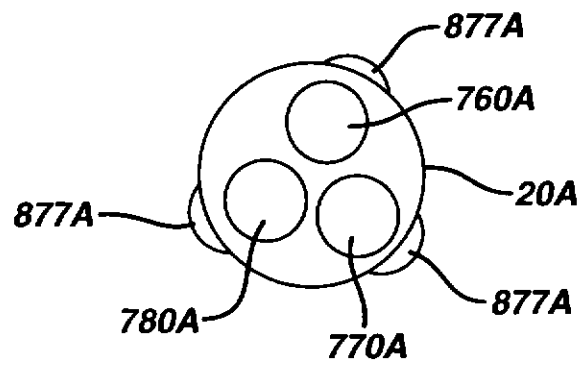


FIG. 51

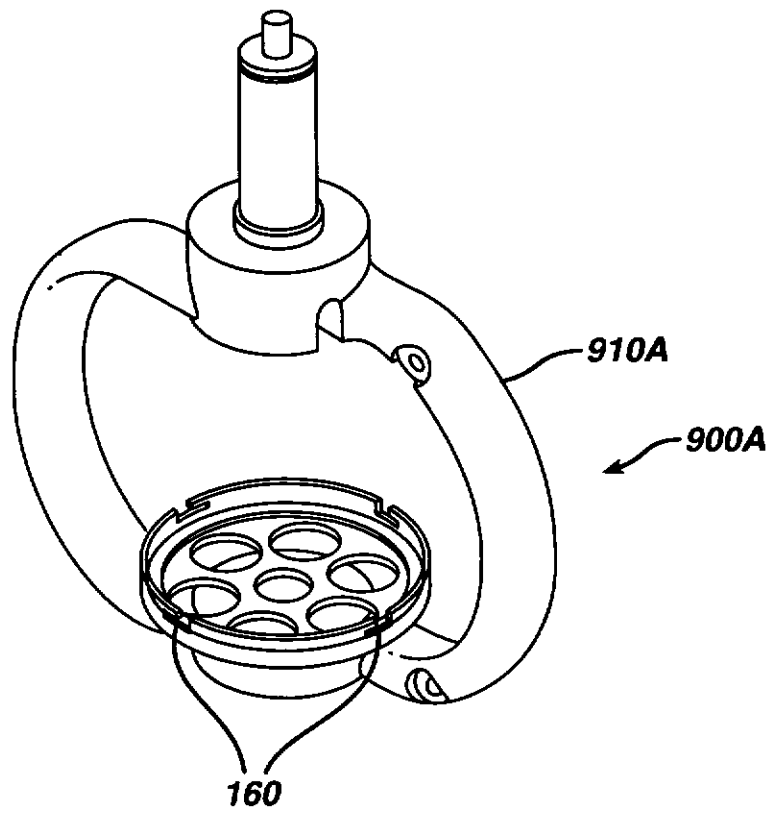


FIG. 52

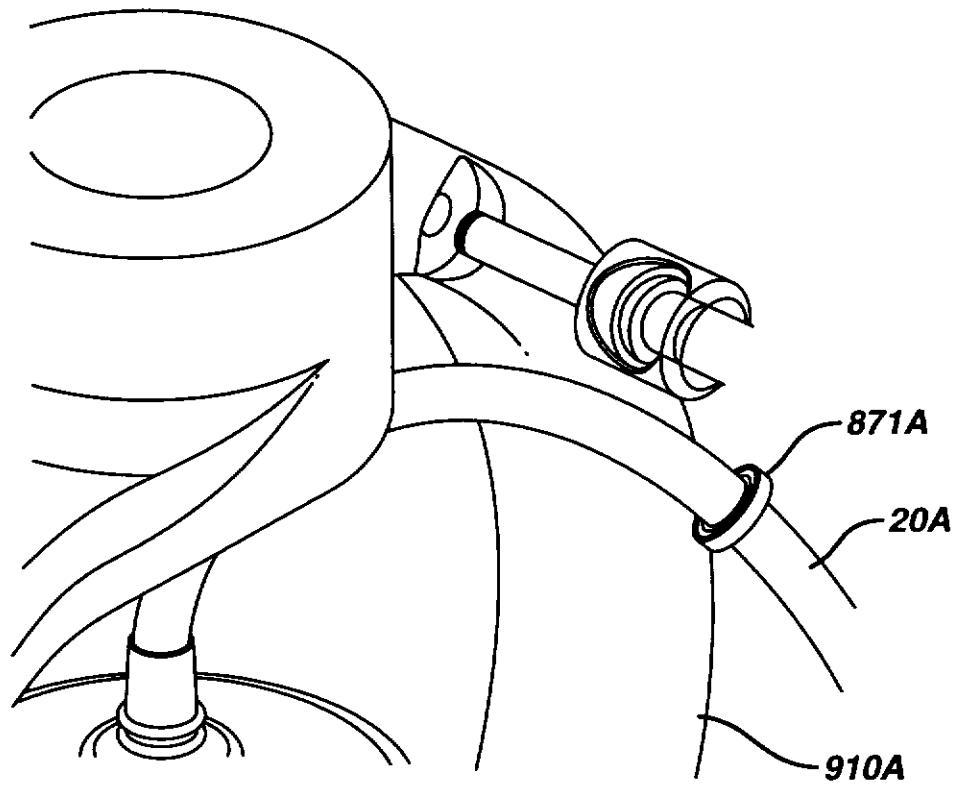


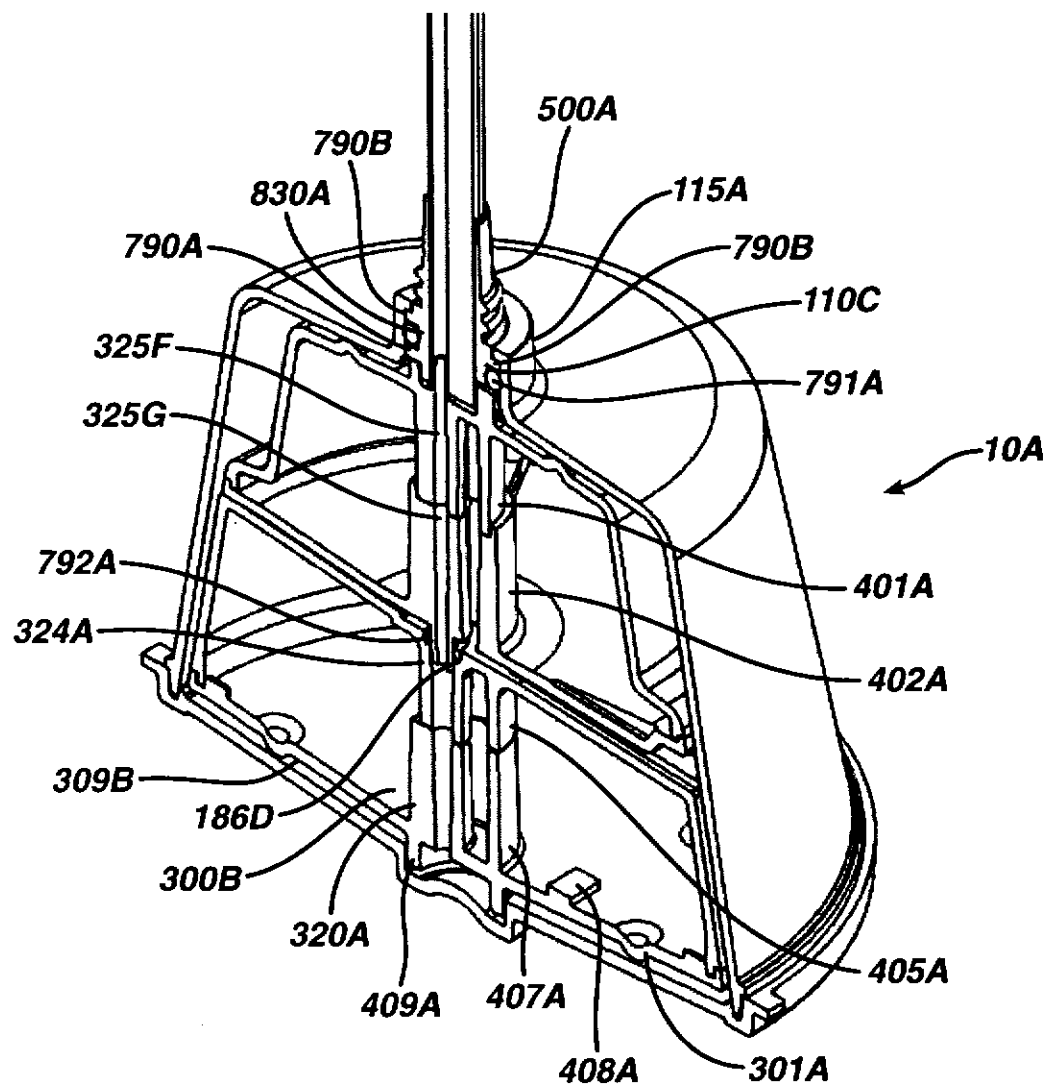
FIG. 53

FIG. 54

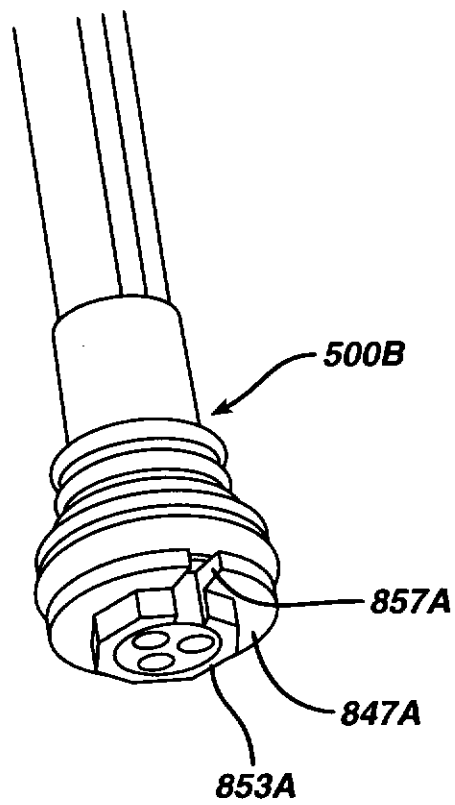


FIG. 55