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Electrical Inverter with a Silicon Controlled Rectifier Full-Bridge Circuit

FIELD OF THE INVENTION

- 5 The present invention relates to an inverter circuit for converting a DC voltage into an AC voltage.

BACKGROUND OF THE INVENTION

- 10 Conventional inverter circuits typically employ push-pull circuitry to alternately drive the two primary windings of a transformer and generate an alternating positive/negative or AC signal at the secondary windings of the transformer. This type of inverter is widely used in small and medium uninterruptible power supply (UPS) systems (i.e. below 1 kilo-voltamperes), as well as in other equipment which converts DC
- 15 voltage to AC voltage. Although such invertors are simple and reliable, many require low frequency (10-100 Hz) iron core transformers which are large, heavy, and expensive. As a result, these invertors are unsuitable for use in personal computers, fax machines and small UPS systems, and there is therefore a need for a novel inverter circuit which operates in a
- 20 reliable and stable manner but does not require an iron core transformer.

SUMMARY OF THE INVENTION

- In one of its specific embodiments, the present invention is an inverter circuit (10) for converting a DC voltage between a first DC input
- 25 (14) and a second DC input (16) into an AC voltage across a first output terminal (O1) and a second output terminal (O2), characterized in that the inverter circuit comprises: a bridge circuit (3) comprising a plurality of switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit being coupled between said first DC input (14) and a first node (15),
- 30 said bridge circuit further being coupled to said first output terminal (O1) and said second output terminal (O2); a power switch circuit (5) responsive to an intermittent cycle pulse signal (I3) for connecting said first node (15)

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to said second DC input (16); a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3); a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal for controlling said first pulse control circuit (1), a second pulse signal for controlling said second pulse control circuit (2), said first pulse signal and said second pulse signal being in phase opposition, and an intermittent cycle pulse signal for turning said power switch circuit (5) off during periods between a pulse of said first pulse signal and a pulse of said second pulse signal.

15 **BRIEF DESCRIPTION OF THE DRAWINGS**

In the accompanying drawings which illustrate preferred embodiments of the invention:

Fig. 1 shows the inverter circuit in accordance with a preferred embodiment of the present invention.

20 Fig. 2 shows one of the Pulse Control Circuits of Fig. 1.

Fig. 3 shows the other of the Pulse Control Circuits of Fig. 1.

Fig. 4 shows a possible Time Sequencing Circuit for the inverter of Fig. 1.

Fig. 5 is a timing diagram for the circuit of Fig. 4.

25 Fig. 6 illustrates an alternate embodiment of the inverter of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows an inverter 10 in accordance with a preferred embodiment of the present invention. Inverter 10 comprises a full-bridge circuit 3 having a plurality (i.e. four) silicon controlled rectifier switches, or SCRs, S1, S2, S3, and S4, two pulse control circuits labelled 1 and 2



respectively, a time sequencing circuit 4, and a power switch circuit 5. The full bridge circuit 3 is connected directly to a positive DC input terminal 14 and is coupled through the power switch circuit 5 to a negative DC input terminal 16. Referring to Fig. 1, rectifiers S1 and S4 are positively
5 connected in series between the DC input 14 and node 15, so that the anode of S1 is coupled to the positive DC input 14 and the cathode of S4 is connected to node 15 and is thereby coupled, through power switch circuit 5, to the negative DC input 16. As shown in Fig. 1, rectifiers S2 and S3 are similarly connected and are in parallel with the series connection of S1
10 and S4. The AC output voltage of the inverter is generated between terminals O1 and O2. As shown in Fig. 1, an AC load 6 is coupled between the terminals O1 and O2. Output terminal O1 is coupled to the cathode of S1 and the anode of S4, and output terminal O2 is coupled to the cathode of S2 and the anode of S3. Diode D1 is connected in parallel with S1 so that
15 the cathode of D1 is connected to the anode of S1 and the anode of D1 is connected to the cathode of S1. Diodes D2, D3, and D4 are similarly connected in parallel across rectifiers S2, S3, and S4 respectively, as shown in Fig. 1.

The gate and cathode of SCRs S1 and S3 are connected to differential
20 control voltage signals U1 and U3 which are generated by Pulse Control Circuit 1. Similarly, the gate and cathode of SCRs S2 and S4 are connected to differential control voltage signals U2 and U4 which are generated by Pulse Control Circuit 2.

Time Sequencing Circuit 4 outputs three time-sequencing pulse
25 signals: I1, a first half-cycle time sequencing pulse which is the input to Pulse Control Circuit 1; I2, a second half-cycle time sequencing pulse which is the input to Pulse Control Circuit 2; and I3, an intermittent break-off time sequencing pulse which pulses low between the first and second half-cycles and is the input to power switch circuit 5. (See also Fig. 5 which will
30 be described shortly and which shows the waveforms for the signals I1, I2, and I3.)

Preferred embodiments of the Pulse Control Circuits 1 and 2 are

shown in Figs. 2 and 3 respectively. Pulse Control Circuit 1 has two pairs of mutually isolated terminals to output the control pulse signals U1 and U3, and Pulse Control Circuit 2 has two pairs of mutually isolated terminals to output the control pulse signals U2 and U4.

- 5 Referring to Fig. 2, pulse transformer T1 has one primary winding and two secondary windings, with the polarity marked terminal of the primary winding connected to a reference voltage +Vf and the other terminal of the primary winding connected to the collector of transistor Q1. Note that transformer T1 need not comprise an iron core transformer.
- 10 The emitter of transistor Q1 is connected to ground as is one terminal of resistor R5. The base of Q1 is connected to the other terminal of resistor R5 and to one terminal of capacitor C5. The other terminal of capacitor C5 is coupled to the input timing sequence pulse signal I1. Diode D5 is connected in series with the first secondary winding of transformer t1, and
- 15 capacitor C1 and resistor R1 are each connected across the first secondary winding of transformer T1 in the manner shown in Fig. 2. Diode D6, capacitor C3, and resistor R3 are similarly connected to the second secondary winding of transformer T1. Control pulse signal U1 is output across the terminals of C1 and R1, and control pulse signal U3 is output
- 20 across the terminals of C3 and R3.

The description of the configuration of Pulse Control Circuit 2 is the same as the above description for Pulse Control Circuit 1, with components C5, R5, Q1, T1, D5, C1, R1, D6, C3, and R3 correspondingly replaced by C6, R6, Q2, T2, D7, C2, R2, D8, C4, and R4 respectively.

- 25 As shown in Fig. 1, power switch circuit 5 may comprise one power field effect transistor S5, wherein the grid or gate of S5 receives the time sequencing pulse signal I3 and thereby controls whether the channel between the source and the drain of S5, i.e. the control path, is conducting.

- Fig. 4 illustrates a possible embodiment for the Time Sequencing
- 30 Circuit 4 and how time sequencing pulses I1, I2, and I3 may be generated from the signal I0 which acts as an input to the Time Sequencing Circuit 4. In an alternative embodiment, the signals I1, I2, and I3 may be generated

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by a programmable microprocessor or a pulse current supply (not shown) as will be clear to those skilled in the art. Referring to Fig. 4, Circuit 20 generates complementary high/low signals 28 and 30 which are inverted (by conventional means not shown) every half cycle of I0. Circuit 20 may
5 comprise a flip flop triggered by I0, or alternatively signals 28 and 30 may be generated by a programmable microprocessor. One of the signals, signal 28, from circuit 20 and the signal I0 are inputs to NOR gate 22 which outputs I1, and the other signal 30 from circuit 20 and the signal I0 are inputs to NOR gate 24 which outputs I2. As a result, signal I1 pulses high
10 during the first half cycle of I0, i.e the time period of $t_1 + t_0$, and signal I2 pulse high during the second half cycle of I0, i.e the time period of $t_2 + t_0$ (note that $t_2 = t_1$), so that signal I1 and signal I2 are in phase opposition (i.e. they are 180 degrees out of phase with each other) as shown in the timing diagram of Fig. 5. Referring to Fig. 4, NOR gate 26 acts as a digital inverter
15 which inverts the input I0 to produce pulse signal I3.

In operation, during the onset of the first half cycle of I0 power transistor S5 is turned on by the rising edge of I3, and transistor Q1 is turned on by the rising edge of I1 and conducts until the voltage at the base of Q1 discharges, at a rate determined by R5 and C5, below the base-emitter
20 threshold voltage. During the short time that Q1 is conducting, pulses are produced on each of the secondary windings of transformer T1 which charge C1 and C3 respectively through D5 and D6 respectively to a certain voltage. When U1 and U3 reach the trigger voltage necessary to turn S1 and S3 on, the output voltage across O1 and O2 becomes positive as shown
25 for VO1O2 in Fig. 5. At the end of period t_1 , power transistor S5 shuts off and effectively cuts off the entire circuit, while diodes D5 and D6 reversibly isolate the bridge circuit from any back swing of transformer T1. Once cut off, the current flowing through rectifiers S1 and S3 rapidly decreases to a value below the minimum current necessary to maintain the SCRs in a
30 conducting state, i.e. the holding current. Once S1 and S3 switch off, the output voltage across O1 and O2 goes to zero and remains at that value until the first half cycle of I0 ends. Note that to prevent S1 and S3 from

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possible damage, diodes D1 and D3 form a discharge loop in case an inductive load gives rise to an inductive current during cut off of the circuit.

5 The load 6 has a high impedance which maintains a stable current when either of the switching device pairs S1-S3 or S2-S4 are conducting. This current through the load is greater than the holding current, which is the minimum current required to maintain the conducting SCRs in a conducting state after they have been turned on.

10 During the second half cycle of I₀, power transistor S5 repeats the same turn on and cut off operation as just described for the first cycle, except in this case I₂, and not I₁, pulses high when I₃ goes high. Control pulses U₂ and U₄ eventually reach a level which turns on rectifiers S2 and S4 (while S1 and S3 remain cut off). This causes the output voltage across O1 and O2 to become negative as shown for VO₁O₂ in Fig. 5, before it
15 returns to zero when S2 and S4 turn off shortly after I₂ and I₃ go low. When I₃ goes high again, so does I₁, and the cycle repeats. As illustrated in Fig. 5, the output voltage, VO₁O₂, is a two step per half cycle AC voltage signal.

In one embodiment of the present invention which is illustrated in
20 Fig. 6, a filter capacitor C7 is connected between output terminals O1 and O2 so that it is effectively in parallel with the load 6. The output terminals O1 and O2 are additionally coupled to the series connected terminals of S1 and S4 and the series connected terminals of S2 and S3 through inductor L1 and inductor L2 respectively. Inductors L1 and L2 and capacitor C7
25 thereby comprise a filter circuit which increases the duration of the rise and fall times of the output signal, thereby inhibiting high frequency components during the rising and falling edges of the output signal and consequently reducing interference with the load. In addition, inductors L1 and L2 also serve to dampen the load current so that the circuitry can be
30 protected.

Also in Fig. 6, an alternate embodiment of the power switch circuit 5 is shown comprising the power field effect transistor S5, a second power

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field effect transistor S6, current limiting resistor R10, over current detecting resistor R9, gate or grid control resistor R7, gate or grid control transistor Q3, and resistor R8. Referring to Fig. 6, R10 is connected between the drain terminals of S5 and S6. The source of S6 is connected to a first terminal of R8 and a first terminal of R9, while the second terminal of R9 is connected to the negative DC voltage 16. The first terminal of R8 is also connected to the source of S5 (so that the source of S5 is connected to the source of S6) and the second terminal of R8 is connected to the base of Q3. The emitter of Q3 is connected to the negative DC voltage 16 and the collector of Q3 is connected to the gate of S5 and a first terminal of R7. The input I3 is coupled to the second terminal of R7 as well as directly to the gate of S6. In this manner, the combination of R10, S6, and R9 form a control loop or control path for the power switch circuit 5.

In operation, the rising edge of the input pulse signal I3 simultaneously turns on power transistors S5 and S6. Resistor R9 samples the magnitude of the load current, and when the load current reaches a certain threshold magnitude, the voltage drop across R9 turns transistor Q3 on, which lowers the gate potential of power transistor S5, and in turn quickly leads to S5 shutting off. With S5 cut off, the load current shifts to flow through power transistor S6, whereby it is limited by the value of resistor R10. The above described current limiting approach, which does not entirely cut off the current loop, ensures that maximum power can be outputted while still maintaining safe operation of the circuitry.

The above approach is particularly advantageous in the case of a large capacitive load (i.e. approximately 200-400 micro-Farads), such as with a rectifying circuit comprising a large capacitor and a rectifying diode. At the rising edge of the output signal, a large load capacitance effectively acts as a shorted load as it begins to charge. The current limiting function of the power switch circuitry protects the load while the load capacitor charges with the maximum output current that ensures safety and protection. Once the load capacitance has charged to the operating potential, the load current becomes too small to maintain the current

sampling voltage across R9 at a value great enough to keep Q3 on. As a result, power transistor S5 turns on. With S5 on, the power consumption or dissipation in the inverter circuit is principally due to the voltage drop across the conducting SCR pair (either S1- S3 or S2 - S4) and the voltage drop across S5, thus providing a high power efficiency. At the falling edge of I3, transistors S5 and S6 are cut off, and the inductive load current (from L1 and L2) continues to flow towards S5 so that the drain voltage of S5 rises. Diodes D1, D2, D3, and D4 provide a discharge loop for this current so that the SCR switches are protected, and energy is returned to positive DC voltage 14.

The inverter circuit according to the present invention does not comprise an iron core transformer and is capable of being designed so that its size and weight are compatible for use in small type UPS systems. In addition, the power switch circuit 5 acts to protect the entire system and enables safe and reliable inverter operation. While preferred embodiments of the present invention have been described, the embodiments disclosed are illustrative and not restrictive, and the scope of the invention is intended to be defined only by the appended claims.

I CLAIM:



1. An inverter circuit (10) for converting a DC voltage between a first DC input (14) and a second DC input (16) into an AC voltage across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), characterized in that the inverter circuit comprises:
- (a) a bridge circuit (3) comprising a plurality of switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit being coupled between said first DC input (14) and a first node (15), said bridge circuit further being coupled to said first output terminal (O1) and said second output terminal (O2);
 - (b) a power switch circuit (5) responsive to an intermittent cycle pulse signal (I3) for connecting said first node (15) to said second DC input (16);
 - (c) a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3);
 - (d) a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and
 - (e) a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal for controlling said first pulse control circuit (1), a second pulse signal for controlling said second pulse control circuit (2), said first pulse signal and said second pulse signal being in phase opposition, and an intermittent cycle pulse signal for turning said power switch circuit (5) off during periods between a pulse of said first pulse signal and a pulse of said second pulse signal.
2. An inverter according to claim 1 characterized in that said bridge





circuit (3) comprises first, second, third, and fourth switches (S1, S2, S3, S4), said first switch (S1) being coupled between said first DC input (14) and said first output terminal (O1), said second switch being coupled between said first DC input (14) and said second output terminal (O2), said third switch
5 being coupled between said first node (15) and said second output terminal (O2), and said fourth switch (S4) being coupled between said first node (15) and said first output terminal (O1).

3. An inverter according to claim 2 characterized in that said first
10 portion of said bridge circuit comprises said first switch (S1) and said third switch (S3), and said second portion of said bridge (3) comprises said second switch (S2) and said fourth switch (S4).

4. An inverter according to claim 3 characterized in that said first,
15 second, third, and fourth switches (S1, S2, S3, S4) are silicon controlled rectifier switches.

5. An inverter according to claim 4 characterized in that the anode of
said first silicon controlled rectifier switch (S1) and the anode of said
20 second silicon controlled rectifier switch are each connected to said first DC input (14), the anode of said third silicon controlled rectifier switch is connected to said second output terminal (O2), and the anode of said fourth silicon controlled rectifier switch is connected to said first output terminal (O1).

6. An inverter according to claim 4 or 5 characterized in that each of
said first, second, third, and fourth silicon controlled rectifier switches (S1, S2, S3, S4) is connected in parallel with a diode (D1, D2, D3, D4), such that
the anode of the diode is connected to the cathode of the silicon controlled
30 rectifier and the cathode of the diode is connected to the anode of the silicon controlled rectifier.





7. An inverter according to claim 3, characterized in that said first output terminal (O1) is coupled to said first switch (S1) and to said fourth switch (S4) through a first inductor (L1) and said second output terminal (O2) is coupled to said second switch (S2) and to said third switch (S3) through a second inductor (L2).

8. An inverter according to claim 8, characterized in that a capacitor (C7) is coupled between said first output terminal (O1) and said second output terminal (O2).

9. An inverter according to claim 3, characterized in that each of said first pulse control circuit (1) and said second pulse control circuit (2) comprises a transformer (T1, T2) having one primary winding with first and second terminals, a first secondary winding with first and second terminals, and a second secondary winding with first and second terminals, such that:

the first terminal of said primary winding is connected to a first reference signal, the second terminal of said primary winding is coupled through a switching circuit (Q1, C5, R5, Q2, C6, R6) to a second reference signal, said switching circuit being responsive to a pulse signal (I1, I2) for generating a pulse of a first polarity across said primary winding;

the first terminal of said first secondary winding is connected through a first diode (D5, D7) to a first terminal of a first capacitor (C1, C2) and a first terminal of a first resistor (R1, R2) and the second terminal of said first secondary winding is connected to a second terminal of said first capacitor (C1, C2) and a second terminal of said first resistor (R1, R2), so that an output pulse (U1, U2) is generated between the first terminal and the second terminal of said first resistor (R1, R2) in response to said pulse across said primary winding; and

the first terminal of said second secondary winding is connected





through a second diode (D6, D8) to a first terminal of a second capacitor (C3, C4) and a first terminal of a second resistor (R3, R4) and the second terminal of said second secondary winding is connected to a second terminal of said second capacitor (C3, C4) and
5 a second terminal of said second resistor (R3, R4), so that an output pulse (U3, U4) is generated between the first terminal and the second terminal of said second resistor (R3, R4) in response to said pulse across said primary winding.

- 10 10. An inverter according to claim 9, characterized in that said first diode (D5, D7) and said second diode (D6, D8) are configured to isolate said first secondary winding from said first capacitor (C1, C2) and from said first resistor (R1, R2) and to isolate said second secondary winding from said second capacitor (C3, C4) and from said second resistor (R3, R4) when said
15 pulse across said primary winding is not of said first polarity.

11. An inverter according to claim 3, characterized in that said power switch circuit (5) comprises a power transistor (S5), the drain of said power transistor (S5) being connected to said bridge circuit (3), the source of said
20 power transistor (S5) being connected to said second DC input (16), and the gate of said transistor (S5) being coupled to said intermittent cycle pulse signal (I3).

12. An inverter according to claim 3, characterized in that said power
25 switch circuit (5) comprises:

- (a) a first power transistor (S5), the drain of said first power transistor (S5) being connected to said bridge circuit (3), and the gate of said first power transistor (S5) being coupled through a first resistor (R7) to said intermittent cycle pulse
30 signal (I3);
- (b) a second power transistor (S6), the gate of said second power transistor (S6) being coupled to said intermittent cycle pulse





signal (I3) and the source of said second power transistor (S6) being coupled to the source of said first power transistor (S5);

(c) a third transistor (Q3);

5 (d) a second resistor (R8) coupled between the source of said first power transistor (S5) and the base of said third transistor (Q3);

(e) a third resistor (R9) coupled between the source of said second power transistor (S6) and the second DC input (16) for detecting the magnitude of the current between said first output terminal (O1) and said second output terminal (O2);
10 and

(f) a fourth resistor (R10) coupled between the drain of said first power transistor (S5) and the drain of said second power transistor (S6) for limiting the magnitude of said current between said first output terminal (O1) and said second output terminal (O2) when said magnitude exceeds a threshold value;
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