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DRAWINGS ATTACHED

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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices.

Copending U.K. Application No. 21832/71 (Serial No. 1,340,619) describes a semiconductor device adapted for storing and sequentially transferring electronic signals representing information in the form of packets of excess minority carriers localised in artificially induced potential wells, e.g. such as can be associated with a metal-insulator-semiconductor (MIS) structure. In one embodiment a plurality of metal electrodes are disposed in a row over an insulator which in turn overlies and is contiguous with the surface of a semiconductor body. Sequential application of voltages to the metal (gate) electrodes induces potential wells adjacent the surface of the semiconductor body in which excess minority carriers can be stored and between which these minority carriers can be transferred. To ensure predictable directionality of charge transfer, at least three-phase clock pulses are required, as described in the said copending application. This presents a problem in some applications because separate conduction paths must be used for each separate phase. It is usually desirable to minimise the number of conduction paths (and attendant conduction path crossovers) in monolithic semiconductor devices.

According to one aspect of the present invention a semiconductor device includes a body of semiconductive material in which electrical charge carriers are storable in a potential well produceable in said body and are transferable to successive potential wells produceable in said body, said device being such that, in operation, the leading part, in the direction of charge carrier transfer to the next successive well, of each well has a larger average depth than the trailing part of the same well, thereby to enhance charge carrier transfer in the said direction relative to the opposite direction. There may be provided insulating material on a surface of said body, and a succession of electrodes disposed on said insulating material, the spacing between the leading part, in said direction, of each of said electrodes and said surface being less than that between the trailing part of the same electrode and said surface.

According to another aspect of the present invention a semiconductor device includes a body of semiconductive material, insulating material on a surface of said body, and a succession of electrodes disposed on said insulating material, each said electrode overlying a portion of said insulating material of non-uniform thickness, said device being such that, in operation, suitable energisation of a said electrode produces an asymmetrical potential well thereunder in said body for storing electrical charge carriers, the asymmetry of said well being such as to enhance charge carrier transfer in the direction of the next successive electrode relative to the opposite direction. The spacing between the leading part, in said direction, of each of said electrodes and said surface may be less than that between the trailing part of the same electrode and said surface.

The trailing part of each of said electrodes except the first, may overlie, at least partially, and be insulated from the leading part of the preceding one of said electrodes.

Each electrode may include a part intermediate the leading and trailing parts, the spacing between said leading part and said

surface being greater than and less than that between said intermediate and trailing parts respectively and said surface.

There may be, in the succession of electrodes, a plurality of odd-numbered electrodes interconnected with each other, and a plurality of even-numbered electrodes interconnected with each other.

The device may include input means for injecting said electrical charge carriers into an input position in said body. The input means may comprise an input electrode overlying and insulated from said input position.

The device may include means for detecting the presence or absence of said electrical charge carriers at an output position in said body. The detecting means may comprise a region of semiconductive material of opposite type conductivity to and forming a p-n junction with said body, and an electrode contacting said region.

The invention will now be described and explained with reference to the accompanying drawings, in which:

Fig. 1 is a cross-sectional view of a device in accordance with the invention;

Fig. 2 shows the device of Fig. 1 and the approximate shape and position therein of potential wells with a clock pulse applied;

Fig. 3 shows appropriate two-phase voltage waveforms;

Fig. 4 is a cross-sectional view of another device in accordance with the invention;

Fig. 5 shows the device of Fig. 4 and the approximate shape and position therein of potential wells with a clock pulse applied;

Fig. 6 shows the device of Figs. 4 and 5 at another point in time; and

Fig. 7 is a schematic block diagram of a two-dimensional arrangement of devices in accordance with the invention.

It will be noted that the figures have not been drawn to scale, but that certain portions have been exaggerated in relative size for reasons of clarity.

Referring now to Fig. 1, the device *10* includes a semiconductive bulk portion 11 of a first type conductivity (shown illustratively as N-type) overlying the surface of which is a dielectric layer 12 of non-uniform thickness. A plurality of electrodes 13*a*, 14*a*, 13*b*, . . . 13*n*, 14*n* overlie dielectric layer 12, each electrode overlying and being contiguous with the surface of a dielectric portion having three distinct thicknesses. Electrodes 13 (including 13*a* to 13*n*) are connected to a first conduction path 13^1 and electrodes 14 (including 14*a* to 14*n*) are connected to a second conduction path 14^1, both of the conduction paths being adapted for coupling clock pulses applied to terminals 13^{11} and 14^{11} to the electrodes to which they are connected.

Electrode 15, to which an input terminal is connected, overlies a relatively thin portion of the dielectric layer and is adapted for causing the introduction of excess minority carriers, e.g. by field-induced avalanche injection, into the semiconductive portion thereunder. In this manner, input pulses can be coupled into a potential well induced under electrode 13*a*, as will be described in more detail with reference to Fig. 2.

A localised P-type zone 17 in combination with an electrode 16 which makes low resistance electrical contact thereto, a battery 18, and a resistor 19, serve to detect any excess minority carriers which may be in a potential well under electrode 14*n*, as will also be described in more detail in reference to Fig. 2.

A metallic electrode 21, formed on the back surface of bulk portion 11, is connected to ground. This is the presently preferred mode of operation. However, it should be appreciated that bulk portion 11 could be connected to any fixed reference potential provided the clock pulse voltages were correspondingly adjusted. The device can also be operated with bulk portion 11 "floating".

With reference now to Fig. 2, there is shown the device of Fig. 1 with pulses from a two-phase clock 31 applied, the voltage waveforms of which are shown in Fig. 3.

As described in the above mentioned copending application, if silicon and silicon dioxide are used as the semiconductive portion and the dielectric respectively, a preferred method of operation makes use of a continuous uniform bias on all gate electrodes 13*a*—13*n* and 14*a*—14*n* to maintain at least a shallow depletion layer over the entire surface of the device at all times so as to minimise the effect of surface states which are inevitably present at the silicon-silicon oxide interface. These surface states can be troublesome as they contribute to surface recombination of some fraction of the excess minority carriers which in turn leads to signal degradation. Maintenance of a suitable bias on all gate electrodes tends to minimise the adverse effects of such surface states. Accordingly, as shown in Fig. 3, the clock outputs are always some amount negative (V_B), to provide this bias. Of course, if surface states are not a problem, this bias need not be used, in which case the clock voltage could alternate, for example, between zero volts and some negative voltage.

Also shown in Fig. 2 are schematic representations of the boundaries (33*a*—33*n* and 34*a*—34*n*) of the depletion regions formed in semiconductive bulk portion 11 at some time just past t=0, i.e. when ϕ_1 is most negative (V_N) and ϕ_2 is least negative (V_B). Because a more negative potential is applied

to electrodes 13 then is applied to electrodes 14, depletion regions 33 (under electrodes 13) extending significantly further into bulk portion 11 than do depletion regions 34 (under electrodes 14). Further, it should be noted that all depletion regions under electrodes 13 and 14 are asymmetrical, i.e. least extensive under that portion of their corresponding electrode where the dielectric is thickest, most extensive under that portion of their corresponding electrode where the dielectric is thinnest, and of intermediate extent under that portion of their corresponding electrode under which the dielectric is of thickness intermediate to the thickest and thinnest. The more negative the field potential at the semiconductor-dielectric interface, the greater will be the extent of the depletion region into the semiconductor. Accordingly, the depletion region boundaries 33 and 34 may also be thought of representative of the electric field profile which then exists at the semiconductor-dielectric interface.

With the potentials as just described, assume an input pulse is applied to the input terminal sufficient to inject a number of minority carriers (holes), indicated as "+" into the semiconductor material under electrode 15. Because depletion layer 35, under electrode 15, overlaps depletion layer 33*a*, under gate electrode 13*a*, these excess holes will be drawn into the most negative potential (under the centre portion of electrode 13*a*). Until the clock voltages switch polarity, these excess minority carriers will remain localised (in what is termed a "charge packet") under the centre of electrode 13*a* i.e. at the region of most negative potential, a so-called potential well.

Then, in the next half of the clock cycle, when electrodes 14 are at the most negative potential (V_N) and electrodes 13 are at a less negative potential (V_B), those excess minority carriers will have moved to the right under the now most negative point under the centre portion of electrode 14*a*. In this half of the clock cycle, of course, the field profiles and depletion regions depths will be under electrodes 14 as they were under electrodes 13 during the previous first half of the clock cycle, and vice versa.

Considering the transfer process one more step, during the first half of the next clock cycle (when electrodes 13 are most negative and electrodes 14 are least negative) the charge packet will again move to the right and become localised at the local potential minimum under the centre portion of electrode 13*b*.

The charge packets will never move to the left because the built-in asymmetry of the potential wells is such that the potential at the right of a local minimum is always more negative than the potential immediately to the left of that local minimum, i.e. the built-in asymmetry of the potential wells is such as to enhance charge transfer in the desired direction (in this case, to the right) and to impede charge transfer in the opposite direction (in this case, to the left).

Assume now that "n" clock cycles have gone by so that the charge packet has moved into the potential well under the last gate electrode 14*n*. This is the output end of the device. Battery 18 supplies a sufficient voltage through electrode 16 to keep the PN junction associated with localised zone 17 reverse-biased by an amount sufficient that its space charge depletion region partially overlaps the depletion region 34*n* under electrode 14*n*. Accordingly, the charge packet is swept to the right and is collected by the PN junction in much the same fashion as carriers are collected in the collector-base junction of an ordinary transistor. This charge carrier collection manifests itself as a current which flows through battery 18 and resistor 19, causing a corresponding detectable output voltage to be developed at terminal 20.

The embodiment described is of course capable of operating as a shift register. It will be appreciated that at any intermediate point, e.g. at electrode 14*f*, the shift register chain could be tapped into and fan-in or fan-out could be achieved if desired for some logic application. Further, it will be appreciated that the shift register can be operated in a recirculation mode, either for increasing the storage duration or delay, or for regenerating the signal to overcome noise, charge losses, or other forms of signal degradation by simply connecting the output signal back to the input stage through an appropriate regeneration circuit.

Referring again to Figs. 1 and 2, it will be understood that a three-step dielectric thickness under each gate electrode need not be used, but that a two-step oxide thickness could be used. In this case the two leftmost portions of each gate electrode, i.e. the thickest and the thinnest would be retained, and the rightmost third, i.e. of intermediate thickness would not. Two-phase clock operation would be the same as previously described.

Selection of a two-step or a three-step oxide depends on the following considerations. In a semiconductor, charge carriers move by one or both of two processes, drift and diffusion. Drift is electric field-motivated, but diffusion involves random movement from points of greater charge density to points of lesser charge density. It will be apparent to those skilled in the art that under certain extreme conditions the diffusion component to the left could tend to overcome the drift component to the right.

However, this would be much less likely to happen in the three-step case because the intermediate step (at the right of each potential well) will tend to cause a preferred "diffusion leak" to the right, i.e. in the desired direction of propagation.

With reference now to Fig. 4 adjacent gate electrodes, in addition to being formed on non-uniform dielectric thicknesses, partially overlap each other. This is considered advantageous for many applications because the overlapping of adjacent gate electrodes tends: (1) to reduce the practical problem of having to form closely spaced electrodes on one plane surface, and (2) to facilitate the coupling of adjacent potential wells which further enhances the ease of transferring charge packets from one potential well to the one next adjacent in the desired direction.

The device *40* includes a semiconductive bulk portion 41 of a first type conductivity (again, illustratively N-type), overlying which there is a substantially uniform first dielectric layer 42. A plurality of gate electrodes 43*a*—43*n* and 44*a*—44*n* overlie layer 42, adjacent ones of the gate electrodes overlapping each other, as shown. A plurality of additional dielectric portions 45*a*—45*n* and 46*a*—46*n* also overlie layer 42 and are disposed between the overlapping electrodes so that there is no direct electrical connection at the points of overlap. Input electrode 47, and output elements 48, 49, 50, 51 and 52 are analagous to the corresponding elements described with reference to Figs. 1 and 2.

Clock pulses similar to those shown in Fig. 3 and described with reference to Figs. 1 and 2 can be used to shift charge packets in the device shown in Figs. 4, 5 and 6. Accordingly, the same two-phase clock 31 shown in Fig. 2 is shown again in Figs. 5 and 6.

Referring now to Fig. 5, broken line features 63*a*—63*n* and 64*a*—64*n* represent schematically the boundaries of the depletion regions formed in bulk portion 41 at some time just past t=0, i.e. when ϕ_1 is most negative (V_N) and ϕ_2 is least negative (V_B). Of course, the above discussion with respect to the relation between depletion region depth and electric field potential applies also to the structure of Figs. 4, 5 and 6. However, it should be noted in Fig. 5 that the dielectric thicknesses and the least negative clock voltage (V_B) have been adjusted in relation to each other such that V_B is insufficient to create a depletion region under the portions of the gate electrodes overlying the thicker dielectric, i.e. there is a gap between depletion regions 63*a* and 64*a*, 63*b* and 64*b*, etc. This gap is preferred in order to completely eliminate the possibility of charge diffusion to the left. Also, any positive charges introduced under input electrode 47 will be immediately swept into depletion region 63*a* and will be trapped there while ϕ_1 is most negative (V_N).

Fig. 6 shows the approximate positions of depletion regions 63 and 64 *while* the clock pulses are reversing polarity, i.e. while ϕ_1 is switching from V_N to V_B and ϕ_2 is switching from V_B to V_N. At the selected intermediate point in time, the previous gap between depletion regions 63*a* and 64*a*, 63*b* and 64*b*, etc. has been bridged, and similar gaps have formed between depletion regions 64*a* and 63*b*, 64*b* and 63*c*, 64*n*—1 and 63*n*, etc. It will be appreciated that this alternate depletion region decoupling (gapping) and coupling is such as to enhance charge transfer to the right (toward the output) and to impede charge transfer to the left. Additionally, in view of the obvious asymmetry in the depletion regions shown in Figs. 5 and 6 it will be apparent that with each reversal of the clock pulse polarity, there will be a strong tendency for any charge packets trapped in any given potential well to transfer to the right, as desired, towards the output.

Detection at the output of the device of Figs. 4, 5 and 6 is directly analagous to the output detection described with reference to Figs. 1 and 2, and thus will not be described further.

Fig. 7 shows schematically a two-dimensional array of devices such as described above. Each row of blocks labelled "GATE" may be similar to any of the devices shown in cross-section in Figs. 1, 2, 4, 5 and 6. Each block labelled "GATE" schematically represents one of the gate electrodes numbered 13, 14, 43 or 44 in those aforementioned figures. Application of the two-phase clock, as shown, to conduction paths 101 and 102 will cause the contents of the top row to be shifted out and detected sequentially by the "DETECTOR" and translated to an appropriate output signal. This shifting of the contents of the top row will not affect the contents of signals stored in the other rows because at most only one, 102, of the clock pulse conduction paths connected to the gates in those rows is pulsed.

After the contents of the top row have been completely shifted out to the right and detected, the clock and the detector would then be connected to conduction paths 102 and 103 and the contents of the second row would be shifted out in like manner. Of course, for optimum results, suitable switching and timing means should be included to switch the clock and the detector from one pair of conduction paths to another and for appropriately timing the output from the detector. Various circuits are suitable

for this purpose and their design is well within the capability of those skilled in the art.

It will be apparent that a two-dimensional array may find use as the photosensitive element in a video camera, in much the same manner as described in copending U.K. Application No. 21832/71 (Serial No. 1,340,619). Each device may represent one raster line in the video system. Each raster line would be read-out electronically by serially transferring the photo-generated charge packets to a detector at the end of the row. A video frame would be constructed by sequentially reading each raster line.

It will be also apparent that a two-dimensional array may also find use as a solid state image display device such as is described in copending U.K. Application No. 21830/71 (Serial No. 1,340,617).

In copending U.K. Application No. 21832/71 (Serial No. 1,340,619) a wide variety of means are proposed for providing input stages and output stages. Such means can also be used in the device described herein, and accordingly will not be described further.

The fabrication of and choice of suitable materials for the devices described are well within the capabilities of those skilled in the art. For example, the use of silicon for the semiconductive portions and silicon dioxide as the dielectric portions will be straightforward and in accordance with well established practice. Combinations of dielectrics such as silicon oxide-silicon nitride, or silicon oxide-aluminium oxide, may be especially advantageous in certain circumstances as the dielectric layer. Known electrode materials such as gold, aluminium, platinum, molybdenum, titanium and combinations thereof may of course be used.

For the purpose of illustration only, a device as shown in Figs. 1, 2, 4 and 5 could employ 10 ohm-cm N-type silicon as the semiconductive bulk portion and silicon oxide thicknesses of 1000 Å—2000 Å for the thinner dielectric layer portions and 5000 Å—10000 Å for the thicker portions. Electrodes may be of gold or gold-platinum-titanium combinations in any typical thickness, e.g. 0.1 to several microns.

The dimensions of the devices can also vary widely. Of course, the spacings of the electrodes (in order to provide the requisite depletion region overlap) will depend upon the lateral extent of the depletion regions under operating voltages. For example, in 10 ohm-cm silicon, a voltage of 15 volts over a 1000 Å silicon oxide will produce a depletion region of about 5 microns. This would suggest that an interelectrode spacing of no greater than several microns should be used. It should be apparent that the interelectrode spacings in the embodiment of Figs. 4, 5 and 6 are much less critical than in Figs. 1 and 2.

Clearly, materials other than silicon can be used in carrying out the invention.

WHAT WE CLAIM IS:—

1. A semiconductor device including a body of semiconductive material in which electrical charge carriers are storable in a potential well produceable in said body and are transferable to successive potential wells produceable in said body, said device being such that, in operation, the leading part, in the direction of charge carrier transfer to the next successive well, of each well has a larger average depth than the trailing part of the same well, thereby to enhance charge carrier transfer in the said direction relative to the opposite direction.

2. A device as claimed in claim 1 wherein there is provided insulating material on a surface of said body, and a succession of electrodes disposed on said insulating material, the spacing between the leading part, in said direction, of each of said electrodes and said surface being less than that between the trailing part of the same electrode and said surface.

3. A semiconductor device including a body of semiconductive material, insulating material on a surface of said body, and a succession of electrodes disposed on said insulating material, each said electrode overlying a portion of said insulating material of non-uniform thickness, said device being such that, in operation, suitable energisation of a said electrode produces an asymmetrical potential well thereunder in said body for storing electrical charge carriers, the asymmetry of said well being such as to enhance charge carrier transfer in the direction of the next successive electrode relative to the opposite direction.

4. A device as claimed in claim 3 wherein the spacing between the leading part, in said direction, of each of said electrodes and said surface is less than that between the trailing part of the same electrode and said surface.

5. A device as claimed in claim 2 or 4 wherein the trailing part of each of said electrodes, except the first, overlies, at least partially, and is insulated from the leading part of the preceding one of said electrodes.

6. A device as claimed in claim 2 or 4 wherein each of said electrodes includes a part intermediate the leading and trailing parts, the spacing between said leading part and said surface being greater than and less than that between said intermediate and trailing parts respectively and said surface.

7. A device as claimed in any one of claims 2 to 6 wherein in the succession of electrodes there are a plurality of odd-

for this purpose and their design is well within the capability of those skilled in the art.

It will be apparent that a two-dimensional array may find use as the photosensitive element in a video camera, in much the same manner as described in copending U.K. Application No. 21832/71 (Serial No. 1,340,619). Each device may represent one raster line in the video system. Each raster line would be read-out electronically by serially transferring the photo-generated charge packets to a detector at the end of the row. A video frame would be constructed by sequentially reading each raster line.

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In copending U.K. Application No. 21832/71 (Serial No. 1,340,619) a wide variety of means are proposed for providing input stages and output stages. Such means can also be used in the device described herein, and accordingly will not be described further.

The fabrication of and choice of suitable materials for the devices described are well within the capabilities of those skilled in the art. For example, the use of silicon for the semiconductive portions and silicon dioxide as the dielectric portions will be straightforward and in accordance with well established practice. Combinations of dielectrics such as silicon oxide-silicon nitride, or silicon oxide-aluminium oxide, may be especially advantageous in certain circumstances as the dielectric layer. Known electrode materials such as gold, aluminium, platinum, molybdenum, titanium and combinations thereof may of course be used.

For the purpose of illustration only, a device as shown in Figs. 1, 2, 4 and 5 could employ 10 ohm-cm N-type silicon as the semiconductive bulk portion and silicon oxide thicknesses of 1000 Å—2000 Å for the thinner dielectric layer portions and 5000 Å—10000 Å for the thicker portions. Electrodes may be of gold or gold-platinum-titanium combinations in any typical thickness, e.g. 0.1 to several microns.

The dimensions of the devices can also vary widely. Of course, the spacings of the electrodes (in order to provide the requisite depletion region overlap) will depend upon the lateral extent of the depletion regions under operating voltages. For example, in 10 ohm-cm silicon, a voltage of 15 volts over a 1000 Å silicon oxide will produce a depletion region of about 5 microns. This would suggest that an interelectrode spacing of no greater than several microns should be used. It should be apparent that the interelectrode spacings in the embodiment of Figs. 4, 5 and 6 are much less critical than in Figs. 1 and 2.

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2. A device as claimed in claim 1 wherein there is provided insulating material on a surface of said body, and a succession of electrodes disposed on said insulating material, the spacing between the leading part, in said direction, of each of said electrodes and said surface being less than that between the trailing part of the same electrode and said surface.

3. A semiconductor device including a body of semiconductive material, insulating material on a surface of said body, and a succession of electrodes disposed on said insulating material, each said electrode overlying a portion of said insulating material of non-uniform thickness, said device being such that, in operation, suitable energisation of a said electrode produces an asymmetrical potential well thereunder in said body for storing electrical charge carriers, the asymmetry of said well being such as to enhance charge carrier transfer in the direction of the next successive electrode relative to the opposite direction.

4. A device as claimed in claim 3 wherein the spacing between the leading part, in said direction, of each of said electrodes and said surface is less than that between the trailing part of the same electrode and said surface.

5. A device as claimed in claim 2 or 4 wherein the trailing part of each of said electrodes, except the first, overlies, at least partially, and is insulated from the leading part of the preceding one of said electrodes.

6. A device as claimed in claim 2 or 4 wherein each of said electrodes includes a part intermediate the leading and trailing parts, the spacing between said leading part and said surface being greater than and less than that between said intermediate and trailing parts respectively and said surface.

7. A device as claimed in any one of claims 2 to 6 wherein in the succession of electrodes there are a plurality of odd-

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numbered electrodes interconnected with each other, and a plurality of even-numbered electrodes interconnected with each other.

8. A device as claimed in any one preceding claim including input means for injecting said electrical charge carriers into an input position in said body.

9. A device as claimed in claim 8 wherein said input means comprises an input electrode overlying and insulated from said input position.

10. A device as claimed in any one preceding claim including means for detecting the presence or absence of said electrical charge carriers at an output position in said body.

11. A device as claimed in claim 10 wherein said detecting means comprises a region of semiconductive material of opposite type conductivity to and forming a p-n junction with said body, and an electrode contacting said region.

12. A semiconductor device substantially as herein described with reference to Fig. 1 or 4 of the accompanying drawings.

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