

08/11/02
2002067528

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



ACTION

(43) International Publication Date
22 November 2001 (22.11.2001)

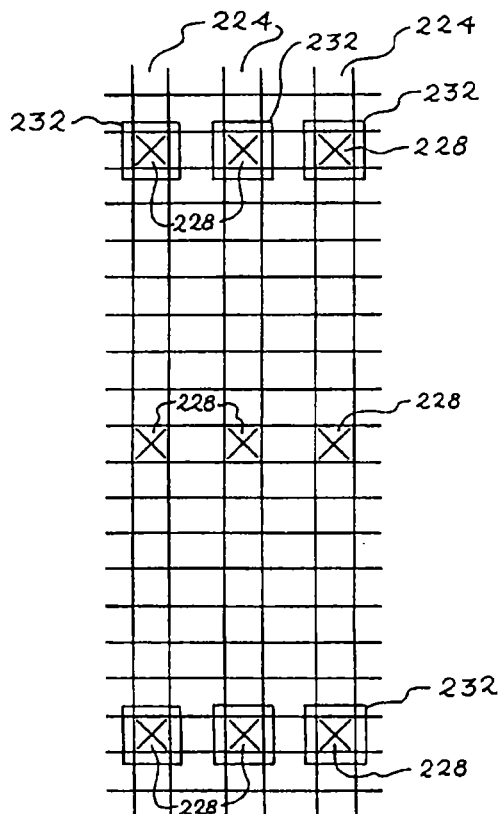
PCT

(10) International Publication Number
WO 01/88985 A3

- (51) International Patent Classification⁷: **H01L 21/8246**, 27/115
- (21) International Application Number: PCT/US01/14122
- (22) International Filing Date: 1 May 2001 (01.05.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/204,621 16 May 2000 (16.05.2000) US
09/721,035 22 November 2000 (22.11.2000) US
- (71) Applicant: **ADVANCED MICRO DEVICES, INC.**
[US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).
- (72) Inventors: **RANDOLPH, Mark, W.**; 3637 Kendra Way, San Jose, CA 95130 (US). **HOLLMER, Shane, Charles**; 1964 Conifer Lane, San Jose, CA 95132 (US). **CHEN, Pau-Ling**; 12947 Arroyo De Arguello, Saratoga, CA 95070 (US). **FASTOW, Richard, M.**; Apartment #2, 10203 Parkwood Drive, Cupertino, CA 95014 (US).
- (74) Agent: **RODDY, Richard, J.**; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

[Continued on next page]

(54) Title: UNIFORM BITLINE STRAPPING OF A NON-VOLATILE MEMORY CELL



(57) Abstract: An array of memory cells that includes a plurality of memory cells interconnected via a grid of M wordlines and M bitlines (224), wherein M = 2, 3, 4, 5, ... and each of the M bitlines (224) is buried. The array further includes a plurality of contacts (228), wherein each of the plurality of contacts (228) is formed every N wordlines, N = 1, 2, 3, ..., wherein each of the plurality of contacts (228) overlies a gate (229) of a different one of the plurality of memory cells. A strap (231) connects one of the buried bitlines (224) to a gate (229) that underlies one of the plurality of contacts (228) and a select transistor (232) is formed every P wordlines, wherein P is greater than N.

WO 01/88985 A3



162162

WO 01/88985 A3

(84) **Designated States (regional):** ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

(88) **Date of publication of the international search report:**
23 May 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— with international search report