CLAIMS

1. A manufacturing method for a semiconductor device, comprising:

providing a substrate and a stacked structure located on the substrate, the stacked structure comprising semiconductor layers and interlayer insulating layers that are alternately stacked;

forming a plurality of channel holes running through the stacked structure, wherein the semiconductor layers located between adjacent channel holes are configured to form back gates;

performing oxidation processing on the semiconductor layers exposed at sidewalls of the channel holes to form first gate dielectric layers; and

sequentially forming a channel layer, a second gate dielectric layer, and a gate that cover sidewalls of each of the channel holes; the channel layer, the second gate dielectric layer, and the gate jointly forming a transistor, wherein each of the back gates is configured to regulate a threshold voltage of the transistor.

2. The manufacturing method for a semiconductor device according to claim 1, before the forming a plurality of channel holes running through the stacked structure, further comprising:

forming a plurality of groove groups running through the stacked structure and arranged in a first direction, each of the groove groups comprising a first groove and a second groove that are disposed side by side in a second direction, wherein the remaining stacked structure comprises a first stacked sub-structure located between the first groove and the second groove, a second stacked sub-structure located between adjacent first grooves, a third stacked sub-structure located between adjacent second grooves, a fourth stacked sub-structure located between adjacent first stacked sub-structures, and a fifth stacked sub-structure located on a side of the first groove and a side of the second stacked sub-structure, and both the first direction and the second direction are parallel to the substrate and the first direction and the second direction intersect with each other; and

filling the first grooves and the second grooves with an isolation material to form isolation structures.

3. The manufacturing method for a semiconductor device according to claim 2, wherein

the forming a plurality of channel holes running through the stacked structure comprises:

etching at least the fourth stacked sub-structure in the remaining stacked structure to form the plurality of channel holes running through the stacked structure and arranged in the first direction.

4. The manufacturing method for a semiconductor device according to claim 3, after the sequentially forming a channel layer, a second gate dielectric layer, and a gate covering sidewalls of each of the channel holes, further comprising:

removing the interlayer insulating layers in the first stacked sub-structure to form first gaps, the first gaps exposing parts of the channel layer that are disposed opposite to each other in the first direction;

removing the channel layer exposed through the first gaps; and

filling the first gaps with an isolation material to form first interlayer isolation layers.

5. The manufacturing method for a semiconductor device according to claim 4, wherein the removing the interlayer insulating layers in the first stacked sub-structure to form first gaps comprises:

performing etching to form a threshold voltage regulation hole running through the first stacked sub-structure, the threshold voltage regulation hole being located between adjacent channel holes, wherein the remaining semiconductor layers located between the adjacent channel holes serve as the back gates; and

performing lateral etching along the threshold voltage regulation hole to remove the interlayer insulating layers to form the first gaps, the threshold voltage regulation hole and the first gaps being in communication.

6. The manufacturing method for a semiconductor device according to claim 5, wherein the filling the first gaps with an isolation material to form first interlayer isolation layers comprises:

filling the first gaps and the threshold voltage regulation hole with the isolation material;

removing the isolation material from the threshold voltage regulation hole, wherein the isolation material located in the first gaps forms the first interlayer isolation layers; and

filling the threshold voltage regulation hole with a conductive material to form a threshold voltage regulation structure electrically connected to the back gates, the threshold

voltage regulation structure being configured to regulate the threshold voltage of the transistor.

7. The manufacturing method for a semiconductor device according to any one of claims 4 to 6, after the sequentially forming a channel layer, a second gate dielectric layer, and a gate covering sidewalls of each of the channel holes, further comprising:

removing the interlayer insulating layers in the second stacked sub-structure, the third stacked sub-structure, and the fifth stacked sub-structure to form second gaps, the second gaps exposing parts of the channel layer that are disposed opposite to each other in the second direction;

removing the channel layer exposed through the second gaps; and

filling the second gaps with an isolation material to form second interlayer isolation layers, wherein the first interlayer isolation layers and the second interlayer isolation layers divide the channel layer in each of the channel holes into channel portions of a plurality of transistors, two opposite sidewalls of each of the channel portions in the second direction respectively form a first source/drain and a second source/drain, a plurality of transistors arranged in a third direction are connected to a same gate, and the third direction is perpendicular to the substrate.

8. The manufacturing method for a semiconductor device according to claim 7, after the filling the second gaps with an isolation material to form second interlayer isolation layers, further comprising:

removing the semiconductor layers in the fifth stacked sub-structure to form third gaps, the third gaps exposing the first source/drain; and

filling the third gaps with a conductive material to form a plurality of bit lines extending in the first direction and electrically connected to the first source/drain.

9. The manufacturing method for a semiconductor device according to claim 7 or 8, after the filling the second gaps with an isolation material to form second interlayer isolation layers, further comprising:

removing the semiconductor layers in the third stacked sub-structure to form fourth gaps, the fourth gaps exposing the second source/drain; and

forming, in the fourth gaps, storage capacitors electrically connected to the second source/drain.

10. The manufacturing method for a semiconductor device according to any one of claims 7 to 9, after the filling the second gaps with an isolation material to form second interlayer isolation layers, further comprising:

removing the semiconductor layers in the fifth stacked sub-structure to form third gaps, the third gaps exposing the first source/drain; and

performing etching to form a threshold voltage regulation hole running through the first stacked sub-structure, the threshold voltage regulation hole being located between adjacent channel holes, wherein the remaining semiconductor layers located between the adjacent channel holes serve as the back gates; and

simultaneously filling the third gaps and the threshold voltage regulation hole with the conductive material to respectively form the plurality of bit lines extending in the first direction and electrically connected to the first source/drain and a threshold voltage regulation structure electrically connected to the back gates, the threshold voltage regulation structure being configured to regulate the threshold voltage of the transistor.

11. A semiconductor device, comprising:

a substrate;

a plurality of channel portions arrayed in a first direction and a third direction, the first direction being parallel to the substrate, and the third direction being perpendicular to the substrate;

a gate extending in the third direction and passing through the channel portions;

a second gate dielectric layer located between the channel portions and the gate, each of the channel portions, the second gate dielectric layer, and the gate jointly forming a transistor;

a first gate dielectric layer covering two sidewalls that are of each of the channel portions and that are disposed opposite to each other in the first direction; and

back gates located between adjacent transistors arranged in the first direction, the back gates being in contact with the first gate dielectric layer, and each of the back gates being configured to regulate a threshold voltage of the transistor.

12. The semiconductor device according to claim 11, wherein two opposite sidewalls of each of the channel portions in a second direction respectively form a first source/drain and a second source/drain; the second direction is parallel to the substrate and intersects with the

first direction; and the semiconductor device further comprises:

bit lines extending in the first direction, wherein a plurality of first sources/drains arranged in the first direction are connected to a same bit line; and

a plurality of storage capacitors, the storage capacitors being connected to the second source/drain.

13. The semiconductor device according to claim 11 or 12, further comprising:

a threshold voltage regulation structure located between adjacent back gates of adjacent channel portions arranged in the first direction, the threshold voltage regulation structure extending in the third direction and being electrically connected to a plurality of back gates arranged in the third direction.

14. The semiconductor device according to any one of claims 11 to 13, wherein each of the channel portions is of a ring-shaped structure parallel to the substrate; and

a size of the channel portion in the second direction is greater than or equal to a size of the back gate in the second direction.

15. The semiconductor device according to any one of claims 11 to 13, wherein a material of the back gate comprises polysilicon.

16. The semiconductor device according to claim 15, wherein a doping concentration of the back gate is 1E21 cm^{-3} to 1E23 cm^{-3}.

17. The semiconductor device according to claim 12, wherein an isolation structure is disposed between the back gate and the bit line.

18. The semiconductor device according to claim 17, wherein a material of the isolation structure comprises a low dielectric constant material.