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Carrier Signal Leakage Suppression in Modulated Backscattered Interrogator Receivers

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Field of Invention

The present invention relates to signal attenuators. More specifically, the present invention relates to carrier signal leakage suppression in modulated backscattered interrogator receivers.

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Background of Invention

Backscattered interrogator receivers are commonly used in radio frequency identification (RFID) applications where data or information from a transponder to an interrogator is modulated using various modulation schemes including, for example, on-off keying (OOK), amplitude shift keying (ASK) and phase shift keying (PSK). Commonly used receiver architecture for implementing the interrogator for recovering data transmitted from the transponder is a direct conversion receiver architecture (also known as a homodyne architecture). Using the homodyne architecture to recover data transmitted from the transponder involves multiplying the modulated signal backscattered from the transponder with the reference extracted from the carrier signal used by the interrogator for transmission. This architecture has the advantage of providing good receiver sensitivity. However, a concern for this architecture is the carrier signal leakage from the interrogator transmitted signal. The amplitude of this carrier leakage signal is undesirably high compared with the signal received from the transponder and as such poses a problem to the receiver (interrogator) sensitivity as it also operates at the same frequency.

The signal at the receiver input of the Interrogator is the sum of the modulated backscattered signal from the transponder and the carrier signal leaked from the transmitter of the interrogator. Passive (battery-less) RFID systems require interrogators to transmit continuous carrier signal after it has transmitted the command signal to the transponder. This is required to power up the transponder and maintain it in the powered-



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up state. It can be seen that the signal from the transponder rides on top of the leaked carrier signal. The leaked carrier signal may get worse with the use of some antennas that may not have a good voltage standing wave ratio (VSWR). When the leakage of the carrier signal at the receiver input of the interrogator is significant, the receiver input stage needs to employ low noise amplifier and mixer with high power handling capability so that the weak backscattered signal is not corrupted. Otherwise the amplifier gets saturated. Further, the low noise amplifier has to operate in low gain mode. This would require that majority of the receiver signal gain be pushed to the base-band stages. In certain cases, if the carrier signal leakage is significantly adverse, it may not be possible to use a low noise amplifier at the input stage the receiver.

Some prior art methods employed to overcome the problems associated with the carrier signal leakage in RFID applications are described below. One method involves employing phase shifters and amplitude correction circuits to generate signals of the same amplitude but opposing phase to the leaked carrier signal to cancel each other. However, the cancellation that can be achieved depends on the resolution of the phase shifter and amplitude equalizing circuits. Implementing such circuits is costly and complex. Yet another prior art method is to make use of a phase lock loop (PLL) technique to track the carrier signal leakage and regenerate a copy of the leaked carrier signal to cancel the same. However, implementing the PLL with extremely low phase jitter and phase accuracy and regeneration of signal with opposite phase and same amplitude is costly and complex.

Therefore, there is a need for a substantially simple and more cost effective approach to address at least some of the foregoing challenges caused by the carrier signal leakage in a modulated backscattered interrogator receiver.

Summary of Invention

Carrier signal leakage suppression circuits in modulated backscattered interrogating receivers are disclosed. Accordance to an aspect of the invention, a carrier signal leakage suppression circuit includes first and second diodes, the first diode being coupled in

parallel but in opposing polarity to the second diode to provide a first diode pair arrangement. The carrier signal leakage suppression circuit further including a second diode pair arrangement connected in series to the first diode pair arrangement.

5 According to another aspect of the invention, a carrier signal leakage suppression circuit includes first, second, third and fourth diodes, the first and second diodes being coupled in series to each other and in parallel but in opposing polarity to the third and fourth diodes, wherein the third and fourth diodes being coupled in series to each other.

10 According to another aspect of the invention, a selectable carrier signal leakage suppression circuit includes a signal level detector for detecting the strength of an incoming signal; a processor for receiving the detected signal strength and providing a control signal corresponding to the detected signal strength; a first switch coupled to the signal level detector and an input port of a first signal suppression circuit; and a second
15 switch coupled to an output port of the first signal suppression circuit. The first and second switches are responsive to the control signal from the processor. The first signal suppression circuit includes first and second diodes and the first diode being coupled in parallel but in opposing polarity to the second diode.

20 The selectable carrier signal leakage suppression circuit further includes a second signal suppression circuit coupled between the first and second switches. The second signal suppression circuit includes first, second, third and fourth diodes, the first and second diodes being coupled in series to each other and in parallel but in opposing polarity to the third and fourth diodes, wherein the third and fourth diodes being connected in series to
25 each other, the control signal at the first and second switches being indicative of which of the first and second signal suppression circuit to activate.

According to yet another aspect of the invention, a selectable carrier signal leakage suppression circuit includes a signal level detector for detecting the strength of an
30 incoming signal; a processor for receiving the detected signal strength and providing a control signal corresponding to the detected signal strength; a first signal suppression

circuit having input and output ports, the input port thereof being coupled to the signal level detector for receiving the incoming signal; and a first switch coupled to the output port of the first signal suppression circuit and being responsive to the control signal from the processor. The first signal suppression circuit comprising first and second diodes wherein the first diode being coupled in parallel but in opposing polarity to the second diode.

The selectable carrier signal leakage suppression circuit further includes a second signal suppression circuit having input and output ports, the input port thereof being coupled to the signal level detector; and a second switch coupled to the output port of the second signal suppression circuit and being responsive to the control signal from the processor. The second signal suppression circuit includes first, second, third and fourth diodes, the first and second diodes being coupled in series to each other and in parallel but in opposing polarity to the third and fourth diodes, wherein the third and fourth diodes being coupled in series to each other.

Brief Description of the Drawings

Embodiments of the invention are herein described, purely by way of example, with references made to the accompanying drawings, in which:

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Figure 1 shows a signal suppression circuit according to an embodiment of the present invention;

Figure 2 shows exemplary input and output signal traces of the signal suppression circuit of Figure 1;

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Figure 3 shows signal suppression circuits according to alternative embodiments of the present invention;

Figure 4 shows an interrogator receiver according to a first embodiment of the present invention;

Figure 5 shows a two-stage signal suppression and amplification of an interrogator receiver according to a second embodiment of the present invention;

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Figure 6 shows an interrogator receiver according to a third embodiment of the present invention;

Figure 7 shows an interrogator receiver according to a fourth embodiment of the present invention; and

5 Figure 8 shows an interrogator receiver according to a fifth embodiment of the present invention.

Detailed Description of the Invention:

The invention proposes cost effective approaches to address at least some of the impacts
10 the carrier signal leakage has on RFID systems in particular and direct conversion
receivers in general. The approaches involve making use of the inherent property of
diodes to suppress or attenuate the amplitude of a leaked carrier signal from an
interrogator. The amplitude of the leaked carrier signal is significantly greater than that of
the signal (backscattered signal) transmitted from a transponder. Thus the signal at the
15 input of the interrogator receiver is a composite signal comprising of the carrier leakage
signal from the interrogator transmitter and the modulated backscattered signal from the
transponder as shown in 200. The invention describes a method of suppressing the
amplitude of a composite signal containing both the leaked carrier signal and
backscattered signal at the input of the interrogator in such a way that the amplitude of
20 the carrier leakage signal is suppressed without substantially reducing the amplitude of
the backscattered signal. Once the amplitude of the composite signal is reduced, low
noise amplifier with sufficiently higher gain can be used without the need of high power
handling capability. Further, handling signals with relatively smaller amplitude enables
flexibility in the design of the receiver architecture whereby some of the gain
25 requirements of the receiver can be pushed from the IF or base-band section (i.e. input
stage of the interrogator) to the RF section. Lower gain at the IF section helps to
minimize the problems caused by the DC offset in the direct conversion receiver
architecture.

30 Figure 1 shows a signal suppression circuit 100 according to an embodiment for
suppressing high amplitude RF signals. The signal suppression circuit 100 having an

input port 102 and an output port 104 includes two diodes 106 and 108 connected in parallel but in opposing polarity to each other. The diodes can be any commonly available diodes including pin diodes and low drop voltage diodes. Incoming RF signals (i.e. a composite signal) at the input port 102 pass through the two diodes 106 and 108 resulting in suppressed RF signals at the output port 104. An example of the RF signals is a signal trace 200 as shown in Figure 2. This signal is a composite signal comprising of the carrier leakage signal and the modulated backscattered signal which is significantly smaller in amplitude compared to the carrier leakage signal. The positive half cycle of the RF signal 200 passes through diode 106 while the negative half cycle of the RF signal 200 passes through diode 108. Due to the inherent characteristic of the diodes, high amplitude signals have a signal drop corresponding to the forward bias voltage of the diode. A silicon diode may have a typical voltage drop of 0.7 volts. In this case, the high amplitude carrier leakage signal is attenuated leaving the smaller amplitude backscattered signal substantially unaffected. Signal trace 250 as shown in Figure 2 shows an example of the suppressed RF signals at the output port 104 of the signal suppression circuit 100. Thus the signal suppression circuit 100 removes a portion of the amplitude of the RF signals from both the positive and negative cycles starting from a zero DC reference voltage line.

If further signal suppression is needed, the suppression circuit 100 may be cascaded. This is particularly useful in situation where the carrier signal leakage is substantially high. Figure 3 shows signal suppression circuits 300, 320, 340 and 360 according to alternative embodiments. The signal suppression circuit 300 includes two pairs of diodes wherein diodes 302 and 306 are connected in series but in parallel and in opposing polarity to diodes 304 and 308, which are connected in series to each other as shown in Figure 3. The signal suppression circuit 320 is a general extension to the signal suppression circuit 300 having n-pairs of diode arranged in similar manner. The number of pairs of diode needed depends on the magnitude of the carrier signal leakage and the desired performance of the receiver system wherein the signal suppression circuit 320 is employed. Suppression circuit 340 is another alternative way to cascade the suppression

circuit 300. Similarly, suppression circuit 360 is another alternative way to cascade the suppression circuit 100.

Figure 4 shows a carrier signal leakage suppression architecture used in a modulated backscattered interrogator receiver 400 according to an embodiment. The receiver 400 includes an antenna 402 coupled to an optional circulator 404, a band-pass filter 406, a suppression circuit 408, a low noise amplifier (LNA) 410 and a down-converter mixer stage 412.

The suppression circuit 408 can be made of anyone of the suppression circuits shown in Figures 1 and 3. The suppression circuit 408 reduces the carrier leakage signal as explained in the foregoing. Thus, the amplitude of RF signals at the inputs of the LNA 410 and mixer stage 412 are considerably lower. This result in a lower DC offset voltage at the output of the mixers, which is an inherent problem of a direct conversion receiver. Another benefit of having a substantially lower amplitude RF signal is that the LNA 410 can be operated with a higher gain without being driven into saturation thereby improving the overall receiver sensitivity.

LNA normally has a specified output power rating. If higher gain is desirable multiple stages can be used. According to an alternative embodiment, the suppression circuit 408 coupling to the LNA 410 configuration can be repeated resulting in a two-stage signal suppression and amplification configuration 500 as shown in Figure 5.

Figure 6 shows a carrier signal leakage suppression architecture used in a modulated backscattered interrogator receiver 600 according to an alternative embodiment. The receiver 600 includes an antenna 602 coupled to a low isolation circulator coupler 604, a band-pass filter 606, a directional detector 608, an analogue to digital converter (ADC) 610, a processor 612, a selectable suppression circuit 613, a low noise amplifier (LNA) 624 and a down-converter mixer stage 625.

In the receiver 600, the directional detector 608 is a signal level detector, which provides a DC voltage proportional to the strength of the carrier signal leakage. The ADC 610 converts this DC voltage into a corresponding digital signal and feeds the information to the processor 612 controlling the selectable suppression circuit 613 for selecting an appropriate suppression circuit. The selectable suppression circuit 613 includes two RF switches 614 and 622 coupled to an array of signal suppression circuits 616, 618, 620 as shown in Figure 6. These RF switches 614 and 622 are controlled by the processor 612 to enable one of the signal suppression circuits to operate depending on the detected strength of the carrier signal leakage. The processor 612 selects the number diodes required for the optimum reduction of the carrier leakage based on the signal from the ADC 610. If the carrier signal leakage is strong, the output of the directional detector 608 is high and the processor 612 selects maximum number of diodes combination to reduce the amplitude of the leaked carrier signal. If the carrier leakage is very low, the processor may select a signal path 615 without any diode as shown in Figure 1. This implementation is capable of selecting the number of operational diodes in the described configuration based on the carrier signal leakage for the optimum performance of the interrogator receiver 600.

Figure 7 shows an example of an extension of the interrogator receiver 600 of Figure 6 whereby the selectable suppression circuit 613 thereof is cascaded to provide multiple selectable signal suppression stages.

Figure 8 shows an interrogator receiver 800 having a selectable suppression circuit 810 according to an alternative embodiment. The selectable suppression circuit 810 includes an array of suppression circuits 814, 818 and 822 and an array of switches 816, 820 and 824 coupled to each of the suppression circuits respectively as shown in Figure 8. A processor 812 depending on the detected strength of the carrier signal leakage controls the array of switches.

The present invention is described in terms of particular arrangements, elements and methods for convenience of explanation and is not intended to be limiting. A person

skilled in the art will understand based on the description herein that the present invention applies to other arrangements, choices of elements and other methods that accomplish substantially the same result in substantially the same way. Accordingly, the scope of the present disclosure is not to be limited to the details given herein, but may be modified
5 within the scope and equivalents of the appended claims.

Claims

1. A carrier leakage signal suppression circuit having an input port and an output port comprising:

5 first and second diodes, the first diode being coupled in parallel but in opposing polarity to the second diode to provide a first diode pair arrangement such that an incoming signal received at the input port resulting in an attenuated carrier leakage signal at the output port without significantly reducing the amplitude of the modulated backscattered signal.

10 2. The circuit of claim 1 further comprising a low noise amplifier coupled to the output port.

3. The signal suppression circuit of claim 1 further comprising a second diode pair arrangement coupled in series to the first diode pair arrangement, the second diode pair arrangement comprising third and fourth diodes, the third diode being coupled in parallel
15 but in opposing polarity to the fourth diode to provide a second diode pair.

4. A signal suppression circuit having an input port and an output port comprising:
first, second, third and fourth diodes, the first and second diodes being coupled in
20 series to each other and in parallel but in opposing polarity to the third and fourth diodes, wherein the third and fourth diodes being coupled in series to each other.

5. A selectable signal suppression circuit comprising:
a signal level detector for detecting the strength of an incoming signal;
25 a processor for receiving the detected signal strength and providing a control signal corresponding to the detected signal strength;
a first switch coupled to the signal level detector and an input port of a first signal suppression circuit; and
a second switch coupled to an output port of the first signal suppression circuit,
30 the first and second switches being responsive to the control signal from the processor,

the first signal suppression circuit comprising first and second diodes, the first diode being coupled in parallel but in opposing polarity to the second diode.

6. The circuit of claim 5 further comprising a second signal suppression circuit
5 coupled between the first and second switches, the second signal suppression circuit comprising first, second, third and fourth diodes, the first and second diodes being coupled in series to each other and in parallel but in opposing polarity to the third and fourth diodes, wherein the third and fourth diodes being coupled in series to each other, the control signal at the first and second switches being indicative of which of the first
10 and second signal suppression circuit to activate.

7. A selectable signal suppression circuit comprising:
a signal level detector for detecting the strength of an incoming signal;
a processor for receiving the detected signal strength and providing a control
15 signal corresponding to the detected signal strength;
a first signal suppression circuit having input and output ports, the input port thereof being coupled to the signal level detector for receiving the incoming signal; and
a first switch coupled to the output port of the first signal suppression circuit and being responsive to the control signal from the processor, the first signal suppression
20 circuit comprising first and second diodes, the first diode being coupled in parallel but in opposing polarity to the second diode.

8. The circuit of claim 7 further comprising:
a second signal suppression circuit having input and output ports, the input port
25 thereof being coupled to the signal level detector; and
a second switch coupled to the output port of the second signal suppression circuit and being responsive to the control signal from the processor, the second signal suppression circuit comprising first, second, third and fourth diodes, the first and second diodes being coupled in series to each other and in parallel but in opposing polarity to the
30 third and fourth diodes, wherein the third and fourth diodes being coupled in series to each other.

9. An interrogator receiver comprising:
an antenna for receiving an incoming signal;
a band-pass filter for filtering the incoming signal;
5 a signal suppression circuit for processing the incoming signal;
a low noise amplifier coupled to the signal suppression circuit; and
a down-converter mixer, the signal suppression circuit comprising any one of the
circuits of claims 1, 3, 4, 5, 6, 7 and 8.
- 10 10. The receiver of claim 9 further comprising a circulator coupler coupled between
the antenna and the band-pass filter.
11. An integrated circuit structure having an interrogator receiver formed as a part
thereof, the interrogator receiver comprising:
15 an antenna for receiving an incoming signal;
a band-pass filter couple for filtering the incoming signal;
a signal suppression circuit for processing the incoming signal;
a low noise amplifier coupled to the signal suppression circuit; and
a down-converter mixer, the signal suppression circuit comprising any one of the
20 circuits of claims 1, 3, 4, 5, 6, 7 and 8.