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PROCESS FOR FORMING COMPLEMENTARY INTEGRATED CIRCUIT DEVICES.

This invention relates to the manufacture of semiconductive integrated circuit devices and more particularly to such devices which include complementary types of elements.

A significant trend in semiconductor manufacture is the steady increase in the number of elements that are included on a single chip. This has involved making the individual elements smaller and packing them closer to increase the density. With the increase in packing density, there has grown the need for isolation barriers between elements. Typically these isolation barriers take the form of guard rings or chanstops, which are regions of relatively high doping, to reduce leakage between neighbouring elements, as might be caused by spurious inversion of the regions between active elements. Such inversions are apt to occur because of the voltages on the conductive runners overlying the chip used for applying operating voltages to the active elements. These chanstops advantageously are usually formed underneath a field oxide, which is a relatively thick oxide used to overlie the chip at passive regions between the active elements.

In complementary integrated circuits, there will be instances where contiguous transistors in the chip are of the same conductivity type in which case a single

chanstop will generally be sufficient for isolation and instances where contiguous transitors are of opposite conductivity type in which case a chanstop of each type is usually desirable for optimum isolation. For saving space it is usually advantageous that this pair of complementary chanstops be back-to-back and it will be convenient to refer to such a structure as a twin chanstop.

On consideration which is pervasive in the manufacture of integrated circuit devices, particularly in high densities, is a fabrication process which results in low cost. Typically this requires a process which permits high yields, which end in turn is best served by a process which includes few critical steps, particularly masking steps requiring accurate registration.

With the present invention as claimed by the addition of a single masking step beyond those normally required, there can be provided, where desired, single chanstops of either type or twin chanstops, self-aligned under the field oxide. The dosages of the implanted donor and acceptor ions are substantially the same and use is made of the known differences in segregation characteristics of the donor and acceptor ions at the growing oxide/silicon interface to control the doping levels of the differently implanted regions and provide the desired doping in individual tubs.

In an illustrative embodiment of the invention there is first formed in each chip portion of a silicon wafer at least one pair of contiguous n-type and p-type tubs at a common surface of a layer of relatively high resistivity. The n-type tub is designed to accommodate the p-channel enhancement mode transistors and the p-type tub is designed to accommodate the n-channel enhancement mode transistor of a complementary pair of such transistors. Then there are formed the nitride/oxide islands which define where the active transistor regions are to be formed in the tubs. Advantageously the resist which is used to define the islands is also maintained over the islands and a p-type implant is done over all the

exposed area. The resist-covered islands act as a mask and shield from this implantation the covered areas where the transistors are to be formed. The ions implanted in the exposed regions of each n-type tub will eventually form the p-type chanstops there.

Then the resist is removed from the islands and a new resist layer is formed over the p-type tub such that only the surfaces of the n-type tub regions not already covered by the nitride/oxide islands are exposed. This is the only additional masking operation that is required to the normal sequence of masking steps. Next, an n-type implant is performed. The implanted ions enter only the unprotected regions of the n-type tubs and these will eventually form the n-type chanstop there. Then the resist is removed from the surface of the p-type tub and the wafer is selectively oxidized in the regions not covered by the nitride/oxide islands. If the doses and energies of the two implants are adjusted appropriately, at the end of this oxidation step there will have been formed beneath the newly formed localized thick oxide regions p-type chanstops at the desired regions of the p-type tubs, n-type chanstops at the desired regions of the n-type tubs, and twin chanstops between contiguous p-type and n-type tubs.

One possible technique for achieving this desired result would be to make the donor implant dose sufficiently higher than the acceptor implant dose that the donor ions overcompensate the acceptor ions in the n-type regions which have been exposed to both. This would have the disadvantage that the p-n junction formed between the two chanstops tends to have a low reverse breakdown value, a factor which may be limiting for some applications.

In our preferred embodiment, boron is chosen as the acceptor and either phosphorus and arsenic as the donors and use is made of their known different segregation properties at a silicon/silicon oxide growing interface to relax the compensation problem. In particular, during the local oxidation step, boron tends

to segregate in the growing oxide rather than accumulating in the silicon, whereas phosphorus and arsenic tend to "snowplough" and accumulate in the silicon rather than enter the growing oxide. As a result, there is an increased concentration of phosphorus or arsenic in the silicon region adjacent the oxide. The amount of phosphorus or arsenic needed to be implanted to ensure that regions, which are to serve as the n-type chanstops, have the requisite high donor doping is consequently reduced. Moreover, of the two donors mentioned, the higher diffusion rate of phosphorus usually makes it preferred since it permits the use of lower implant energies for a desired depth of chanstop.

After formation of the chanstop regions, the p-channel transistors are formed in the n-type tubs and the n-channel transistors are formed in the p-type tubs in any suitable fashion. Advantageously, this involves acceptor ion implantation of localized regions of the n-type tubs using the gate electrode as a mask to form the source/drain regions of the p-type MOS transistors and donor ion implantations of localized regions of the p-type tubs using the gate electrode as a mask to form the source/drain regions of the n-type MOS transistors.

Alternatively other forms of transistors can be formed in the separate tub regions.

An embodiment of the invention will now be described with reference to the accompanying drawings in which:-

FIGS. 1 through 10 show cross-sections of a portion of a silicon wafer at various stages of a process according to the invention.

In FIG. 1 there is shown a portion of a silicon wafer 10 corresponding to a portion of a silicon chip in which there will be formed complementary transistors, for example, as part of a very large scale integrated circuit involving a number of complementary transistors. Typically after the processing is complete each wafer is divided into a number of chips for individual packaging.

Like reference numbers are usually used throughout the figures to denote the same part or regions in different stages of processing. The drawing is not to scale because of the much smaller vertical dimensions typically involved.

There is first prepared in the silicon wafer portion being viewed a pair of contiguous p-type and n-type tubs to form the preferred twin-tub structure in which will be formed the complementary transistors.

To this end, the silicon bulk region 11 which is n-type and of relatively low resistivity, first has grown thereon a lightly doped epitaxial n-type layer 12. The use of relatively lightly doped epitaxial layer on a relatively heavily doped substrate of the same resistivity type is known to provide protection against parasitic SCR-type latchup in CMOS devices.

Then a relatively thin, typically 350 Angstroms, silicon dioxide layer 13 is thermally grown on the surface of the epitaxial layer; and over it is formed a thicker silicon nitride layer 14, approximately 1200 Angstroms thick, preferably by a low pressure chemical vapour deposition process. As is known, the use of the intermediate oxide layer serves as a buffer layer and makes the silicon surface less vulnerable to high temperature steps.

Next as shown in FIG. 2, the silicon nitride/silicon oxide layer 13,14 is patterned in known fashion to remove it from the regions 15 in which the n-type tubs are to be formed and thereafter the wafer is exposed to an implantation of donor ions, preferably phosphorus. The ions, shown by the negative sign, penetrate the silicon essentially only in region 15 where the layer 13,14 has been removed. The donor dosage and implantation energy are chosen to provide, after ion activation, the desired characteristics to the n-type tubs.

After this implantation, the wafer is cleaned in the usual fashion, and then as shown in FIG. 3 a relatively thick layer 16 of silicon dioxide, about 4000 Angstroms

thick, is thermally grown selectively over the region 15. The region 17 underlying the remaining silicon nitride layer 14 remains essentially unaffected by this oxidation step because of the masking effect of the nitride layer 14.

It is to be noted, as seen in FIG. 3, that this process leaves a small ledge 18 in the silicon at the edge of the donor implanted region. Next, the remainder of the silicon nitride layer 14 is selectively removed by a suitable etch (typically aqueous H_3PO_4) which does not significantly affect the silicon dioxide layers 13 and 16. Then as illustrated in FIG. 4, the wafer is bombarded with acceptor ions, advantageously boron, with an energy sufficient to penetrate readily the comparatively thin oxide layer 13 but insufficient to penetrate the thick oxide layer 16, and there is implanted selectively in region 17 acceptor ions, shown as plus signs, to a concentration adequate to convert, after ion activation, the region 17 to p-type with the doping desired for forming the p-type tub.

After removing the oxide layers 13 and 16 by suitable etching and after annealing to drive in and activate the implanted ions by moving them to lattice positions, there results a portion of a wafer as shown in FIG. 5 comprising a layer 12 in which are formed contiguous p-type tub 19 and n-type tub 20, forming a p-n junction at ledge 18. While the two tubs are shown penetrating to equal depths into layer 12, this is not necessary so long as each is deep enough to house the transistors to be incorporated therein.

It should be noted that in some instances it may be unnecessary to have used at this state an annealing step specifically to drive in and activate the implanted ions since it may be possible to depend, for this purpose, on the heating steps that will occur in later steps of the process.

As the next step, there is defined in each tub the active region where its transistors are to be formed.

In commercial devices, there normally will be a plural number of transistors of the one appropriate type in each tub. Since the usual circuit includes more n-type transistors than p-type transistors, the p-type tubs which house the n-type transistors will normally be larger to accommodate more transistors. However, for simplifying the exposition, two transistors only are being shown in each tub. To this end, there is formed again over the entire surface a composite layer typically including a thermally grown silicon oxide layer about 100 Angstroms thick contiguous to the silicon chip and an overlying silicon nitride layer about 1200 Angstroms thick. Conventional processing is then used to form photoresist-covered silicon nitride/silicon oxide islands in each tub region, which will essentially define the regions of the tub in which its transistors will be formed. Anisotropic dry etching advantageously is used in known fashion to form the islands. In FIG. 6, the islands 22 are shown still covered with the photoresist protective coating 23 used to mask the islands during the reactive ion etching. The wafer is then bombarded with boron ions to implant selectively the uncovered surface regions as indicated by the positive signs. This advantageously is a high energy implant, typically using 100 thousand electron volt energies and a dose of $5 \times 10^{12}/cm^2$.

Then the photoresist 23 covering the islands is removed and a new photoresist layer is patterned to cover selectively all of the p-type tubs. This is best done by forming a photoresist layer over the entire wafer and using photolithographic techniques to remove selectively the portion covering the n-type tubs. In this process, use can be made of the ledge 18 in the silicon which effectively marks the interface between the p-type and n-type tubs. As seen in FIG. 7, the photoresist layer 25 covers only the surface of the p-type tub 19 including the islands 22A associated with this tub. Some portions of n-type tub 20 will be

covered by the islands 22B but other portions will be exposed. Then the wafer is subjected to a relatively low energy phosphorus ion implant (typically 30 thousand electron volt energies) at a dose of $5x10^{12}/cm^2$ to implant phosphorus ions in the exposed region of the n-type tub 20 and these are shown by negative signs. The regions of tub 20 underlying the islands 22B are kept substantially free of such ions. The photoresist 25 is then removed and the wafer cleaned with little disturbance of the islands 22A and 22B.

Then the wafer is heated in an oxidizing atmosphere for the selective oxidation of the exposed silicon surface lying between the islands, as in the conventional localized oxidation process, for growing the thick field oxide between the islands.

During the growth of the field oxide, advantage is taken of the fact that phosphorus (or arsenic) has a greater tendency than boron to move out of the growing oxide region and to accumulate in the underlying silicon. As a result, in regions as in portions of tub 20 where both boron and phosphorus were implanted, as the field oxide grows it tends to retain the boron but to reject the phosphorus. Consequently in the underlying silicon, the phosphorus concentration quickly builds up and soon overwhelms the boron even when the implanted concentrations of boron and phosphorus had been initially substantially equal. For this reason it is practical to make the two implants of substantially the same dosage, which has been found to be advantageous.

As a result, as shown in FIG. 8, there is formed in the regions of the n-type tub 20 underlying the field oxide 27 heavily phosphorus-doped n-type chanstops 28. Similarly, underlying the field oxide 27, in the p-type tub 19, there will be formed the heavily boron-doped p-type chanstops 29. Where the two tubs are contiguous, there is formed the twin chanstop with each individual chanstop 28,29 in its appropriate tub. Each chanstop accurately underlies the overlying field oxide.

Because of the fabrication process utilized, there is possible a high degree of control of the dopings of each of the various regions. This makes it possible to minimize the need for overcompensation, which in turn makes it feasible to maintain relatively high the reverse breakdown voltage between the chanstops and other regions of the tubs. Similarly, good control of the chanstop doping minimizes parasitic coupling to active devices.

The islands 22A,22B are now removed to expose the wafer where the active devices are to be formed to provide the structure shown in FIG. 9 where the p-type tub 19 includes p-type chanstops 29 at its surface, where they underlie the thick field oxide 27, and the n-type tub 20 includes n-type chanstops 28 at its surface where they underlie the thick field oxide 27.

In one typical application of the described process, each chanstop of a twin chanstop located at the interface between two tubs had a narrowest dimension of about 5 microns, while the single chanstops located on interior regions of a tub had a narrowest dimension of about 3.5 microns. In the n-type tub, the active region had an excess phosphorus doping of $2x10^{16}$ per cm^3 and in the p-type tub, the active region had an excess boron doping also of $2x10^{16}$ per cm^3. Each of the chanstops was a fraction of a micron deep and each p-type chanstop had an excess boron concentration of about $4x10^{16}$ ions per cubic centimetre, and each n-type chanstop had an excess phosphorus concentration of about $1x10^{17}$ ions per cubic centimetre.

After this stage of processing is reached, a variety of techniques are available for further fabrication, and a particular choice would be dictated primarily by the end result sought.

The process is expected to find principal application to the situation where complementary enhancement-mode MOS transistors are to be formed in the separate active regions, the n-channel enhancement-mode

type in the p-type tubs and the p-channel enhancement-mode type in the n-type tubs. However, in some instances, it may be desirable to form depletion-type transistors in one or both tubs.

Also in some instances, it may prove advantageous to form one or more bipolar junction transistor or junction field-effect transistor in one or more of the tubs.

One illustrative technique for forming complementary enhancement-mode MOS transistors in the tubs begins by forming a thin gate oxide layer over the surface of each of the active regions in the p-type and n-type tubs. This is followed by formation of the gate electrodes. Usually it is advantageous to use the same doped-polycrystalline silicon material for the gate electrode conductor of each of the two transistor types and to have the same threshold voltage for the two types. This may require some extra treatment of the surface of one of the two tubs if this factor was not adequately provided for when the two tubs were formed initially. For example, if n-doped polysilicon is to be used for the gate conductor, it may be necessary to use a shallow boron implant at the surface of the n-tubs to make more positive the threshold voltage of the p-channel transistors to be formed there. In this instance the p-type tubs would be masked with a photoresist while boron ions were implanted into the n-tubs.

After any threshold adjustment implant, the photoresist mask used is removed and a polysilicon layer is deposited over the surface of the chip. The polysilicon layer is then patterned to define the gate electrodes which are localized appropriately in the active regions and also to define any conductive runners to be used for interconnection purposes. The thin oxide remaining on the exposed regions where the sources and drains are to be located may then be removed, but typically it is preferred to do the source and drain implantations through this oxide so that it can protect the

silicon surface from damage.

Then there follows a boron implant which serves to form the p-type source and drain zones of the p-channel transistors in the n-type tubs. It typically is unnecessary to mask the p-type tub during this operation since the boron implanted there can readily be overdoped subsequently by a phosphorus implantation. However, before such phosphorus implantation to form the n-type source and drain regions of the n-channel transistors in the p-type tubs, the n-type tubs are masked against such implantation. This is readily done by appropriately patterning a photoresist layer deposited initially uniformly over the wafer. After the mask is provided, the wafer is exposed to a phosphorus ion beam for formation of the desired source and drain regions of the n-channel transistor. This implantation typically also serves to dope the polysilicon gate electrodes and any runners to increase their conductivity.

It will generally be usual next to provide a protective phosphorus-doped glass layer over the surface of the wafer and flow it at elevated temperature to smooth out the topography. This heating also serves to activate the source and drain implants. Then openings are formed to the silicon surface through which source, drain and gate electrode connections are made to the appropriate regions for handling the operating voltages.

In FIG. 10, there is shown the basic structure of a portion of a completed device made in the fashion described. It includes the portion of a silicon wafer including the bulk layer 11 on which lies the epitaxial layer 12, which includes the p-type tub 19 and the n-type tub 20. Within the p-type tub 19 are a pair of n-channel enhancement-mode transistors formed by the n-type source/drain regions 31,32 with their electrodes 31A,32A and the gate oxides 33 with their gate electrodes 33A. Within the n-type tub 20 are a pair of p-channel enhancement-mode transistors formed by the p-type source/drain regions 34,35, their electrodes 34A,35A, the

gate oxides 36 and their gate electrodes 36a. Separating the individual transistors are portions of the thick field oxide 27 under which lie the chanstop. Separating the two n-type transistors in the p-type tub is the single p-type chanstop 29, and separating the two p-type transistors in the n-type tub is the single n-type chanstop 28. Separating the two tubs is the twin chanstop 28,29. A phosphorus-doped glass 40 covers all portions of the surface of the chip through which protrudes the various electrodes.

It should be understood that the specific process described is illustrative of the preferred embodiment of the invention but that variations may be made consistent with the general principles of the invention. For example, though it has proved advantageous to apply the invention to twin-tub technology, the principles should be applicable to other technologies that provide surface regions of appropriate doping for the formation of complementary transistors in such surface regions.

CLAIMS

1. A process for forming complementary chanstops at the surface of a silicon wafer whose surface includes p-type and n-type regions comprising implanting acceptor ions selectively in the surface regions of the wafer where the chanstops are to be formed, implanting donor ions selectively into the n-type regions where the n-type chanstops are to be formed, the dosages of the implanted donor and acceptor ions being substantially the same, and heating the wafer in an oxidizing atmosphere while the portions of the wafer in which chanstops are to be formed are exposed so as to oxidise the surface regions where chanstops are to be formed, the respective segregation characteristics of the implanted donor and acceptor ions at the growing oxide/silicon interface being such that underlying the oxide there are formed in the p-type surface regions localized p-type chanstops where acceptor ions are in excess and in the n-type surface regions localized n-type chanstops where the donor ions are in excess.

2. A process as claimed in claim 1 in which boron is the acceptor and either phosphorus or arsenic is the donor.

3. A process as claimed in claim 1 or claim 2 in which the p-type and n-type regions are in the form of p-type and n-type tubs formed in a layer of higher resistivity.

4. A process as claimed in any of the preceding claims wherein the p-type and n-type surface regions are contiguous and form a p-n junction and there is formed a twin chanstop underlying the oxide.

5. A process as claimed in claim 4 in which the process of forming contiguous surface regions of opposite conductivity type includes forming on a substrate of relatively low resistivity an epitaxial layer of higher resistivity and like type, forming a composite silicon oxide-silicon nitride layer over the epitaxial layer and removing the composite layer from selected regions of the epitaxial layer, implanting donor ions selectively into regions of the epitaxial layer where the composite layer has been removed, heating the substrate in an oxidising atmosphere to form over the

implanted region an oxide layer appreciably thicker than the oxide layer in the composite layer, removing the silicon nitride portion of the composite layer, and implanting acceptor ions selectively into regions of the epitaxial layer covered only by the remaining oxide layer portion of the composite layer, whereby there results in the epitaxial layer contiguous regions rich in acceptor and donor implanted ions respectively.

6. A process as claimed in claim 5 in which the donor and acceptor ions implanted in the epitaxial layer are of phosphorus and boron, respectively.

7. A process for forming complementary chanstops substantially as herein described with reference to the accompanying drawings.

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