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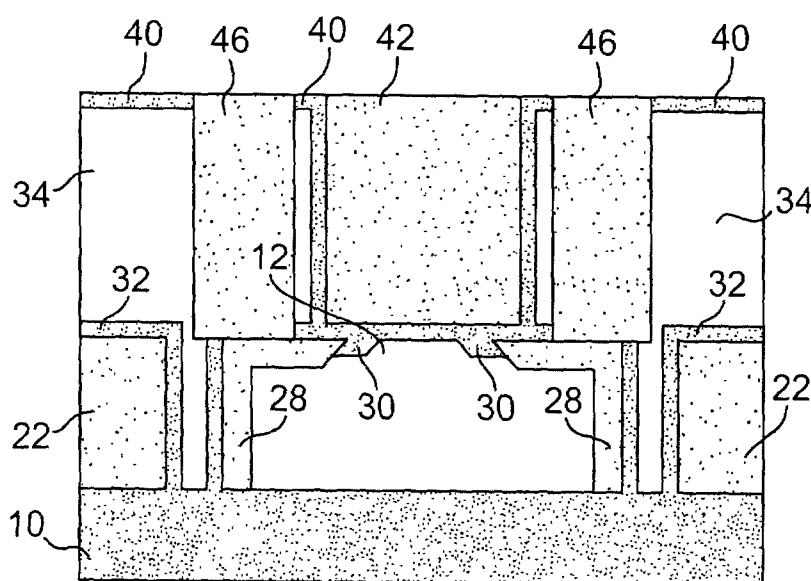
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(54) Title: METHOD FOR WRAPPED-GATE MOSFET



(57) Abstract: The present invention relates to a wrapped-gate transistor including a substrate having an upper surface and first and second side surfaces opposing to each other. Source and drain regions (28) are formed in the substrate with a channel region therebetween. The channel region extends from the first side surface to the second side surfaces of the substrate. A gate dielectric layer (40) is formed on the substrate. A gate electrode (42) is formed on the gate dielectric layer (40) to cover the channel region from the upper surface and the first and second side surfaces with the gate dielectric (40) therebetween. The substrate is a silicon island (12) formed on an insulation layer of an SOI (silicon-on-insulator) substrate or a conventional non-SOI substrate, and

has four side surfaces including the first and second side surfaces. The source and drain regions (28) are formed on the portions of the substrate adjoining the third and fourth side surfaces which are perpendicular to the first and second side surfaces. The wrapped-gate structure provides a better and quicker potential control within the channel area, which yields steep sub-threshold slope and low sensitivity to the "body-to-source" voltage.



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