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PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(19)



(54) FABRICATION OF COMPLEMENTARY SEMICONDUCTOR DEVICES

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the fabrication of semiconductor devices, and especially to the fabrication of integrated circuit devices conaining field effect transistors of different type conductivity.

Certain types of integrated circuit devices include a plurality of field effect transistor components each comprising an insulating layer disposed between a gate electrode and a semiconductor channel region, the electrode and channel region being accurately aligned with one another. In some instances, it is desired that various ones of the components comprise P type channel field effect transistors while other components on the same substrate comprise N type channel field effect transistors. Devices containing such different type conductivity transistors are referred to as "complementary" devices.

A problem, heretofore, was that of providing, in a simple and reproducible manner, such complementary devices. For example, because of the different conductivity characteristics of the various components, a relatively large number of masking and doping sequences, requiring the use of several photomasks and careful register thereof, has been required. These various operations are difficult and time-consuming, providing low yields of product at high cost.

According to the invention we provide a method of fabricating semiconductor devices of the complementary type characterized by comprising: forming spaced islands of a semiconductor material on or in a substrate, one of said islands being of P type conductivity and another of said islands being of N type conductivity, providing a laminate structure on a portion of each of said islands, said structures comprising a first layer of dielectric material and a covering layer of semiconductor material, providing on said P type island, including the laminate structure thereon, a solid-to-solid diffusion source layer containing N type conductivity-defining impurities, providing on said N type island, including the laminate structure thereon, a solid-to-solid diffusion source layer containing P type conductivity-defining impurities, and driving the conductivity defining impurities in said source layers into the materials covered thereby to provide gate electrodes and source and drain regions for a transistor formed in each of said islands, said transistors being of opposite type conductivity.

In the accompanying drawings:—

FIGURE 1 is a plan view of a workpiece used in one embodiment of the invention;

FIGURE 2 is a section along line 2-2 of FIGURE 1;

FIGURES 3 and 4 are views similar to that of FIGURE 2 but showing the workpiece at later stages in the fabrication process according to one embodiment of the present invention

FIGURE 5 is a plan view of the workpiece shown in FIGURE 4;

FIGURE 6 is a view similar to that of FIGURES 3 and 4 but at a later step in the fabrication process;

FIGURE 7 is a section along line 7-7 of FIGURE 6;

FIGURES 8, 9, 10 and 11 are views similar to that of FIGURE 6 but at successively later steps in the fabrication process; and

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FIGURE 12 is a plan view of the workpiece at still a later step in the fabrication process.

The process, according to one embodiment of the invention, begins with a workpiece (FIGURES 1 and 2) comprising an insulating substrate 12 having a plurality of spaced islands 14, 16, and 18 thereon, each island comprising a layer of a semiconductor material, e.g., silicon, germanium, silicon carbide, various III-V compounds. The embodiment described herein utilizes silicon as the semiconductor material. The substrate 12 can comprise any of a number of materials on which the various semiconductor materials can be deposited. Examples of suitable substrate materials are sapphire, spinel, diamond, and silicon carbide. Sapphire is used in the embodiment. In another embodiment of the invention, not illustrated, the substrate comprises a semiconductor material, e.g., one of the above-identified materials, and, instead of forming spaced raised islands on a surface of the substrate, spaced islands or regions of different conductivity characteristics are provided within the substrate, the regions extending to a surface of the substrate. The various processes described hereinafter, in connection with raised islands, can be performed on the surface of the semiconductor substrate.

The islands 14 and 18 are of N conductivity type, having a resistivity of about 10 omh-cm, and the island 16 is of P conductiyity type, having a resistivity of about 1 ohm-cm, each of the islands having a thickness of the order of 1 micron. For convenience of illustration and description, only three islands are shown. However, in actual practive, a relatively large number of spaced islands are generally formed on a substrate, the number, size and shape of the islands depending upon the particular integrated circuit being made.

Processes for providing the workpiece (FIGURES 1 and 2) are known, and while not being shown, can comprise, for example, depositing a first layer of silicon of N conductivity type on the substrate 12, segmenting the silicon layer into the individual islands 14 and 18 (the remains of the first layer being designated by the reference numberal 20 in FIGURE 2), covering the islands 14 and 18 with a masking layer, depositing a second layer of P conductivity type onto the workpiece, and removing portions of the second layer (the remains thereof being designated by the reference numeral 22) leaving the island 16. The masking layer covering the islands 14 and 18 is then removed to provide the workpiece shown in FIGURES 1 and 2.

Thereafter, as shown in FIGURE 3, a third layer 24 of a dielectric material, such a silicon dioxide, silicon nitride, aluminum oxide, is provided on each of the islands 16 and 18, but not on the island 14. In the embodiment, the layer 24 is of silicon dioxide and has a thickness of 1,000 Å. It can be provided, for example, by known thermal growth or deposition techniques. A thermal growth technique is preferred as providing a more dense and impervious layer. This, we have found, provides better results with respect to the performance of the field effect transistors fabricated therewith.

A fourth layer 26, of conductive material, or a material convertible into a conductive material e.g., germanium or silicon which is preferably intrinsic, is then provided on the workpiece. A layer of undoped polycrystalline silicon, having a thickness in the order of one micron, is used in the embodiment, provided, for example, by known deposition techniques.

Thereafter, as shown in FIGURES 4 and 5, a photosensitive material layer 28 is deposited on the workpiece, and two latent images 30 and 32, overlying the islands 16 and 18, respectively, are photoprinted in the layer 28 using a single photomask, according to known processes. As shown in FIGURE 5, the latent images 30 and 32 extend beyond opposite edges of the islands 16 and 18. The layer 28 is developed and fixed, leaving masking areas 28′ (FIGURES 6 and 7) overlying each island 16 and 18 and extending beyond two opposite sides of each of the islands, as shown in FIGURE 7. Photolithographic processes for performing these steps are known.

All of the exposed portions of the two layers 24 and 26 are then removed using etchants which do not attack the masking areas 28′. For example, using the aforementioned photoresist material, an etchant comprising dilute potassium hydroxide is used to remove the exposed portions of the poly-crystalline silicon layer 26, and an etchant comprising buffered hydrofluoric acid is used to remove the exposed portions of the silicon dioxide layer 24.

The masking areas 28′ are then removed, the resulting structure appearing as shown in FIGURE 8. The remaining portions of the layers 24 and 26, referred to hereinafter as the "laminate structures 36", overlie a region 38 of each island 16 and 18.

As described hereinafter, the island regions 38 comprise the channel regions of field effect transistors to be fabricated within the islands 16 and 18. An advantage of the hereindescribed process is that the performance of the simple and easily performed above-described steps results in a highly accurate definition of the transistor channel

regions, a process normally requiring considerable care and accuracy according to prior art processes. For example, in the hereindescribed process, the laminate structures 36, and the channel regions 38 defined thereby, are formed using a single photomask and a single masking layer, whereas, in the prior art, two such masking and alignment steps are required for complementary transistors. Registration of the photomask with the workpiece, often requiring a high degree of accuracy in the prior art, requires comparatively little accuracy in the described process, requiring merely that the images on the photomask defining the laminate structures 36 be merely approximately centered over the islands 16 and 18. This follows because the relative sizes of the source and drain regions of each transistor are relatively unimportant with respect to the transistor performance.

Further, the layers 24 of the laminate structures 36 comprise the gate insulating layer of the field effect transistors to be fabricated, as described hereinafter. A further advantage of the hereindescribed process is that after the layer 24 is first provided on the workpiece, and prior to the definition thereof, the layer 24 is covered by the layer 26 which serves as a mask for the layer 24 in the subsequent processes. That is, once formed, the gate insulating layer 24 is thereafter protected by the covering layer 26. This, it is found, increases the yield of devices as it prevents damage of the gate insulating layers during subsequent processing of the device; this being a problem associated with devices made according to prior art techniques.

Thereafter, as shown in FIGURE 9, the island 18, including the laminate structure 36 thereon, is covered with a layer 42 of silicon dioxide having a high concentration, e.g., in the order of 1×10^{20} atoms/cc, of P type conductivity type impurities, e.g. boron atoms. Also, the islands 14 and 16 are each provided with a covering layer 44 of silicon dioxide having a high concentration, e.g., in the order of 1×10^{20} atoms/cc of N type conductivity type impurities, e.g., phosphorus. The layers 42 and 44 can have a thickness, for example of the order of 1,500 A. Techniques for providing these two layers 42 and 44, e.g., by successive deposition and photolithographic defining sequences, are known.

Of importance is the fact that the definition of each of the layers 42 and 44 is not critical, requiring only a small degree of accuracy. That is, all this is required is that the two layers 42 and 44 cover completely the various islands 14, 16 and 18, as shown in FIGURE 9. Overlap of the layers onto the substrate surface, and even onto each other is immaterial. This greatly simplifies the fabrication of the present devices.

The layers 42 and 44 comprise solid-to-solid diffusion sources for the various materials thereunder. Accordingly, in the next step, the workpiece is heated in an inert atmosphere, e.g., argon, at 1,100°C., to drive the impurities within the layers 42 and 44 into the materials covered thereby. The result of this step is shown in FIGURE 10.

Owing to the N type impurities in the layer 44, the island 14, originally of moderately doped N conductivity, is made highly (N+) doped, e.g., having a resistivity of about .001 ohms-cm.

Within the island 16, the diffusion of N type impurities from the layer 44 causes doping of the polycrystalline layer 26 (referred to hereinafter by the reference numberal 26') of the laminate structure 36 to N type conductivity, of, e.g., about .01 ohms-cm resistivity. Continued diffusion of the N type impurities into the underlying channel region 38 of the island 16 is largely prevented by the presence of the silicon dioxide layer 24 which, as known, is effective as a diffusion barrier. Thus, the channel region 38 remains of P conductivity type.

The diffusion of the N type impurities from the layer 44 of the island 16 into the layer 22 on either side of the channel region 38 provides wo regions 48 and 50 of N conductivity type of, e.g., about .001 ohm-cm resistivity. The resulting structure, comprising two N type regions 48 and 50 on opposite sides of a P type channel region 38, a silicon dioxide layer 24 covering the surface of the channel region 38, and a highly doped layer 26' of low electrical resistivity overlying the channel region 38, comprises an insulated gate field effect transistor of the N-MOS type, i.e., a device having N conductivity source 48 and drain 50 regions, a gate electrode 26', and an oxide layer 24 disposed between the gate electrode 26' and a silicon channel 38.

Likewise, the diffusion of P type impurities from the layer 42 covering the island 18 results in the formation of a P-MOS device, that is, a device having a P conductivity type source region 52, a P conductivity type drain region 54, and a gate electrode 26' of P conductivity.

Advantages of the hereindesoribed process are that the gate electrodes, i.e, the now highly doped and thus conductive polycrystalline layers 26' of the laminate structures 36, are automatically aligned to a high degree of accuracy with the channel regions 38. This follows, as above-described, owing to the fact that the laminate structures 36 serve as the mask in the formation of the regions 38. The alignment of the gate electrode with the channel region of a field effect

transistor is important, as known, for efficient device operation, especially at high frequencies.

Also, the laminate structures 36 serve as a mask in the process of forming the source and drain regions on either side of the channel regions. Although some lateral diffusion of the impurities beneath the laminate structures 36 does occur, the amount of lateral diffusion is very small owing to the extreme thinness of the layers 20 and 22, and the amount of overlap between the gate electrodes and the source and drain regions is minimal. This is effective to minimize the inter-electrode capacitance of the device, which is desirable, as known, for improving the device performance. Thus, as above noted, although the doping source layers 42 and 44 are provided using simple and reproducible processes, requiring a low order of accuracy, various components, having different conductivity characteristics, and having a high degree of dimensional accuracy, are provided.

Additionally, the use of a semiconductor material for the layer 26, in contrast with, for example, the use of a metal, allows greater flexibility in the design of the various components. That is, by selection of the doping of the layers 26, different gate electrodes 26′ having different characteristics, e.g., different work function, best suited for the particular components being fabricated, can be provided.

To complete the device, the doping source layers 42 and 44 are removed, as by etching in buffered hydrofluoric acid, and a thermal oxide layer 60 (FIGURE 11) is grown on the exposed silicon portions of the islands 14, 16 and 18. Since the silicon dioxide layers 24 of the laminate structures 36 are covered by a silicon layer 26′, the thickness of the silicon dioxide layers 24 is not affected by this last thermal growth step. This is advantageous since it allows the use of a thick oxide layer 60, e.g., in the order of 5,000 Å, desired for providing good electrical isolation of the various device components from one another, while allowing the use of a thin channel oxide layer 24, e.g., in the order of 1,000 Å, desired for efficient device performance.

Thereafter, various contact openings 62 are made through the oxide layer 60 exposing, as shown in FIGURE 11, a surface portion of the silicon layer 20 of the island 14, and surface portions of the source and drain regions of the islands 16 and 18. Also, although not shown, surface portions of each gate electrode 26′, at positions not overlying the islands 16 and 18 are also exposed. The off-set relation of the contact holes of the gate electrode 26′ with respect to the islands 16 and 18 is provided because, in the usual instance, the channel regions 38 of the islands, with which the gate electrodes 26′ are aligned, are so small as not to provide a large enough area over the islands to which contacts can be readily made.

A layer (not shown) of metal, e.g., aluminium, having a thickness of 1 micron, is next deposited onto the workpiece and into contact with the various exposed surface portions, and then defined, as by known means, to provide electrical connections 64 (FIGURE 12) for the device. As shown, the elongated island 14 is used as a circuit connector between various components on the substrate 12, e.g., between the source region 48 of the transistor of the island 16 and the gate electrode 26′ of the transistor of the island 18. The thick insulating thermal oxide layer 60 (FIGURE 11) covering the conductive layer 20 of the island 14 allows crossing of other connectors 64 over the island 14 without causing shorting together of the connectors.

In an embodiment using a semiconductor substrate, as previously briefly described, the connector island corresponding to the connector island 14 of the illustrated embodiment is preferably a raised island on the surface of the substrate rather than, as is the case of the transistor islands, a region within the substrate. This is to provide greater electrical isolation of the connector from the substrate and greater freedom of its shape. Also, to further isolate it from the substrate, an insulating layer, e.g., silicon dioxide, is provided between the conductive layer of the connector island and the substrate surface.

WHAT WE CLAIM IS:—

1. A method of fabricating semiconductor devices of the complementary type characterized by comprising: forming spaced islands of a semiconductor material on or in a substrate, one of said islands being of P type conductivity and another of said islands being of N type conductivity, providing a laminate structure on a portion of each of said islands, said structures comprising a first layer of dielectric material and a covering layer of semiconductor material, providing on said P type island, including the laminate structure thereon, a solid-to-solid diffusion source layer containing N type conductivity-defining impurities, providing on said N type island, including the laminate structure thereon, a solid-to-solid diffusion source layer containing P type conductivity-defining impurities, and driving the conductivity defining impurities in said source layers into the materials covered thereby to provide gate electrodes and source and drain regions for a transistor formed in each of said islands, said transistors being of opposite type conductivity.

2. A method as claimed in claim 1 in which said islands are formed of silicon, and

transistor is important, as known, for efficient device operation, especially at high frequencies.

Also, the laminate structures 36 serve as a mask in the process of forming the source and drain regions on either side of the channel regions. Although some lateral diffusion of the impurities beneath the laminate structures 36 does occur, the amount of lateral diffusion is very small owing to the extreme thinness of the layers 20 and 22, and the amount of overlap between the gate electrodes and the source and drain regions is minimal. This is effective to minimize the inter-electrode capacitance of the device, which is desirable, as known, for improving the device performance. Thus, as above noted, although the doping source layers 42 and 44 are provided using simple and reproducible processes, requiring a low order of accuracy, various components, having different conductivity characteristics, and having a high degree of dimensional accuracy, are provided.

Additionally, the use of a semiconductor material for the layer 26, in contrast with, for example, the use of a metal, allows greater flexibility in the design of the various components. That is, by selection of the doping of the layers 26, different gate electrodes 26' having different characteristics, e.g., different work function, best suited for the particular components being fabricated, can be provided.

To complete the device, the doping source layers 42 and 44 are removed, as by etching in buffered hydrofluoric acid, and a thermal oxide layer 60 (FIGURE 11) is grown on the exposed silicon portions of the islands 14, 16 and 18. Since the silicon dioxide layers 24 of the laminate structures 36 are covered by a silicon layer 26', the thickness of the silicon dioxide layers 24 is not affected by this last thermal growth step. This is advantageous since it allows the use of a thick oxide layer 60, e.g., in the order of 5,000 Å, desired for providing good electrical isolation of the various device components from one another, while allowing the use of a thin channel oxide layer 24, e.g., in the order of 1,000 Å, desired for efficient device performance.

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In an embodiment using a semiconductor substrate, as previously briefly described, the connector island corresponding to the connector island 14 of the illustrated embodiment is preferably a raised island on the surface of the substrate rather than, as is the case of the transistor islands, a region within the substrate. This is to provide greater electrical isolation of the connector from the substrate and greater freedom of its shape. Also, to further isolate it from the substrate, an insulating layer, e.g., silicon dioxide, is provided between the conductive layer of the connector island and the substrate surface.

WHAT WE CLAIM IS:—

1. A method of fabricating semiconductor devices of the complementary type characterized by comprising: forming spaced islands of a semiconductor material on or in a substrate, one of said islands being of P type conductivity and another of said islands being of N type conductivity, providing a laminate structure on a portion of each of said islands, said structures comprising a first layer of dielectric material and a covering layer of semiconductor material, providing on said P type island, including the laminate structure thereon, a solid-to-solid diffusion source layer containing N type conductivity-defining impurities, providing on said N type island, including the laminate structure thereon, a solid-to-solid diffusion source layer containing P type conductivity-defining impurities, and driving the conductivity defining impurities in said source layers into the materials covered thereby to provide gate electrodes and source and drain regions for a transistor formed in each of said islands, said transistors being of opposite type conductivity.

2. A method as claimed in claim 1 in which said islands are formed of silicon, and

wherein said laminate structure providing step comprises: thermally growing a layer of silicon dioxide on each of said islands, depositig an intrinsic layer of silicon on said thermally grown layers, covering said intrinsic layer with a photosensitive material layer, forming a latent image of said laminate structures in said photosensitive material using a single photomask, and defining said photosensitive material, said silicon dioxide layer, and said intrinsic layer to provide said laminate structures.

3. A method as claimed in claim 1 including: forming an additional island of semiconductor material on said substrate, covering said additional island with one of said diffusion source layers, and, after said driving step, providing an insulating layer on said additional island.

4. The method as claimed in claim 3 wherein said driving step for the impurities of both of said diffusion source layers is performed at the same time, whereby doping of all of said islands occurs simultaneously.

5. A method of fabricating semiconductor devices of the complementary type substantially as herein described.

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