

SPECIFICATION

Power output circuit

- 5 The present invention relates to a power output circuit.

A known type of protective circuit for a power output circuit as disclosed in Japanese Patent Application publication No. 3064/73 protects the load (loudspeaker) of the power output circuit of the Output Condenser Less (hereinafter referred to as OCL) type.

In order to prevent the loudspeaker from being damaged by a deviation in the output D.C. level (mid-point potential) of the OCL type power output circuit, the known protective circuit detects that the output D.C. level has exceeded a predetermined voltage, and using the detection output it renders non-conducting (or turns "off") switching means such as a relay connected between the output of the power output circuit and the loudspeaker. Thus, the voice coil of the loudspeaker can be protected from damage due to the passage of a direct current.

However, we have found that, in the case of constructing this sort of protective circuit in a semiconductor integrated circuit, detecting transistors for effecting the above detection are damaged by any abnormal operation of the power output circuit or by various surge voltages applied to the semiconductor integrated circuit.

When the detecting transistors have been damaged, there is the danger that the turning-off of the switching means, such as a relay connected between the output of the electric circuit such as an OCL type power output circuit and the loudspeaker load, will not occur, resulting in damage to the loudspeaker load.

We have also discovered the following facts. For protecting the load, such as a loudspeaker, from the abnormal output of the electric circuit, for example an OCL type power output circuit, it is favourable when considering the enhancement of the reliability of the protective operation that, not only the output D.C. level as previously described, but also the abnormal current increase of output transistors caused to thermal runaway, short-circuit of the load, or similar malfunctions is detected and that the switching means is turned non-conducting "off" on the basis of either of these detection outputs.

Detecting transistors for detecting the current of the output transistors are damaged in the same manner as that previously described.

According to the present invention there is provided a power output circuit including:

- 55 load means to be driven by an output of said power output circuit;
switching means connected between said output of the power output circuit and said load means;
a first detector circuit for detecting a first operating
60 status of the power output circuit;
a second detecting circuit for detecting a second operating status of the power output circuit;
a first detecting transistor which receives an output signal of said first detector circuit;
65 a second detecting transistor which receives an

output signal of said second detector circuit; and

a driving transistor which receives an output signal of said first detecting transistor and an output signal of said second detecting transistor and which operates to drive said switching means into an "off" or "on" state;

wherein under a condition in which said first operating status and said second operating status of said power output circuit lie in predetermined normal operating ranges, respectively, the first and second detecting transistors are biased respectively into "on" states by the first and second detector circuits so as to permit predetermined currents to flow therethrough, and wherein said driving transistor is controlled into an "on" state by said output signals of the first and second detecting transistors so as to drive the switching means into the "on" state;

said power output circuit further including:

- 85 a first reference transistor which is connected to the first detecting transistor in a differential manner;
a second reference transistor which is connected to the second detecting transistor in a differential manner;

90 a first constant-current source which is connected to an emitter electrode of the first detecting transistor and an emitter electrode of said first reference transistor;

95 a second constant-current source which is connected to an emitter electrode of the second detecting transistor and an emitter electrode of said second reference transistor;

a protective transistor whose collector and emitter electrodes are respectively connected to a base electrode and an emitter electrode of the driving transistor;

100 a first group of controlling transistors whose base-emitter junctions have collector signals of the first and second detecting transistors applied thereto and whose collector electrodes are connected to said base electrode of said driving transistor in common; and

110 a second group of controlling transistors whose base-emitter junctions have collector signals of the first and second reference transistors applied thereto and whose collector electrodes are connected to a base electrode of said protective transistor in common;

115 wherein when said first operating status or said second operating status of said power output circuit has fallen outside the predetermined normal operating range, said protective transistor is controlled into an "on" state by collector signals of said second group of controlling transistors so as to control said driving transistor into an "off" state, thereby isolating said load means.

The present invention will now be described in greater detail, by way of example, with reference to the accompanying drawings, wherein:-

125 *Figure 1* is a circuit diagram showing a first embodiment of the present invention;

Figures 2 and 3 are circuit diagrams each showing an embodiment of a detector circuit;

130 *Figure 4* is a circuit diagram showing a second embodiment of the present invention; and

Figure 5 is a circuit diagram showing a third embodiment of the present invention.

Referring first to Figure 1, the first embodiment is shown as applied to a complementary push-pull

5 output circuit with two supply voltages. The embodiment detects a fluctuation in an output mid-point potential and an excess output current so as to protect the load and the output transistors.

10 An n-p-n transistor Q_1 and a p-n-p transistor Q_2 form a complementary push-pull output circuit of the OCL type. This push-pull power output circuit operates with a positive supply voltage $+V$ and a negative supply voltage $-V$ as its operating voltages.

15 A resistor R_1 is the load of a driver circuit (not shown), and series diodes D_1 and D_2 form a bias circuit for the transistors Q_1 and Q_2 .

20 A level shift circuit 1a forms a first part of an output D.C. level-detector circuit, and converts the output mid-point potential V_o (at zero volts) into a positive voltage V_s . This level shift output V_s is applied to the base electrode of a detecting transistor Q_4 in a differential transistor circuit 1b which forms a second part of the output D.C. level-detector

25 circuit. The base electrode of a reference transistor Q_5 has a bias voltage V_{B1} applied to it so that, at a normal output, the reference transistor Q_5 is turned "off" whereas the detecting transistor Q_4 is turned "on".

30 In the case of detecting the deviation of the mid-point potential in the negative direction, a circuit (not shown) which is similar to that described above and in which the input and bias voltage of transistors are inverted is employed.

35 A circuit block 2a forms a first part of a detector circuit for detecting an excess current in the output transistor Q_2 . It forms a signal which is at a high level in normal operation, and applied the signal to the base electrode of a detecting transistor Q_6 is a differential transistor circuit 2b. The base electrode

40 of a reference transistor Q_7 has a base voltage V_{B2} applied to it so that, at the normal output, the reference transistor Q_7 is turned "off" whereas the detecting transistor Q_6 is turned "on".

45 The common emitter electrodes of the differential transistor circuits formed by transistors Q_4 and Q_5 and by Q_1 and Q_7 are provided with circuits supplying a constant-current I_p .

50 The collector electrodes of the respective differential transistors Q_4 to Q_7 are provided with diodes D_5 to D_8 which form current mirror circuits. The collector electrodes of corresponding transistors Q_8 and Q_9 , of the P-N-P type controlling transistors Q_8 to Q_{11} which form output transistors of the current mirror

55 circuits, are connected together so as to cause collector currents to flow into a diode D_3 . The forward voltage of this diode D_3 is applied across the base and emitter electrodes of a driving transistor Q_3 , via a capacitor C and a resistor R_{10} connected in parallel across the diode D_3 and forming a smoothing circuit.

60 A relay RL is energized by the current flowing through the transistor Q_3 , to close a contact which is connected between the push-pull output terminal of the circuit comprising transistors Q_1 and Q_2 and a

load SP.

The collector electrodes of corresponding transistors Q_{10} and Q_{11} of the P-N-P transistors Q_8 to Q_{11} which the output transistors of the current mirror

70 circuits, are also made common so as to cause common collector currents to flow into the base electrode of a transistor Q_{12} which short-circuits the base-emitter path of the driving transistor Q_3 .

80 In the circuit of the first embodiment, when the push-pull output circuit is in normal operation, the detecting transistors Q_4 and Q_5 turn "on", and a constant current $2I_o$ flows into the diode D_3 , to turn the driving transistor Q_3 "on" and to connect the output terminal of the push-pull circuit to the load

85 When either of the two detected outputs is in an abnormal state, a constant current I_o flows into the base electrode of the protective transistor Q_{12} , so that a large current of $I_o \times h_{FEQ_{12}}$ (where $h_{FEQ_{12}}$ is the current gain) is absorbed as the output collector current. The driving transistor Q_3 consequently turns "off" because no base current flows therethrough, and it opens the contact of the relay RL to protect the loudspeaker SP or the output transistors Q_1 and Q_2 .

90 Due to the fact that open circuits account for the great majority of the faults occurring in the detecting transistors, the present invention sets the correlations between detection signals and transistors so as to turn "on" all the detecting transistors which

95 receive the detection signals in a normal operation state.

In the circuit of the first embodiment, when the detecting transistors Q_4 and Q_5 are open circuited constant currents will flow through the transistors

100 Q_6 and Q_7 . Therefore, the relay RL is turned "off" to break the connection between the push-pull output terminal and the load and to inhibit the driving of the load by the output circuit in the unprotected state. An enhancement in reliability can thus be achieved.

105 In the first embodiment, the level shift circuit 1a is not necessary. This is because the transistor Q_4 can be turned "on" in normal operation by suitably selecting the bias voltage V_{B1} .

In the case where a level shift is required, a voltage of zero volts at the mid-point is subjected to a level

110 shift in the positive direction by means of resistors R_5 and R_6 as illustrated in Figure 2. The excess output current detector circuit 2 can employ the collector resistors R_7 and R_8 of a phase inverting

115 transistor Q_{13} .

A voltage divider circuit which is made up of a temperature sensor R_s of positive temperature characteristic and a resistor R_9 as shown in Figure 3 may be used as a temperature detector circuit, the divider

120 voltage output being applied to a differential circuit similar to that previously described.

In addition, a circuit, for detecting the short-circuit condition of the load may also be provided, a similar output being applied to a differential circuit similar

125 to that previously described.

The detecting transistor circuit may be constructed according to the second embodiment shown in Figure 4, in which detecting transistors Q_{14} to Q_{16} are connected in series, the collector output of the series transistors being received by a p-n-p type controlling

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transistor Q_{17} , the collector output of which is used to control the relay driving transistor Q_3 as previously described.

In this case, only when all the detecting transistors Q_{14} to Q_{16} turn "on" can the transistor Q_{17} turn "on" to turn the relay driving transistor Q_3 "on", so that the same protective operation as previously described is effected.

The present invention can be extensively utilized, not only for the push-pull output circuit with two supply voltages, but also for power output circuits such as a push-pull circuit with a single supply voltage. In this case, detection signals may be formed as are necessary.

Referring now to the third embodiment shown in Figure 5, an electric circuit 100 includes an OCL type power output circuit, in which circuit elements enclosed by a broken line IC are constructed within a semiconductor integrated circuit and the other circuit elements are discrete electronic components. The power output circuit in the electric circuit 100 operates using a positive supply voltage $+V$ applied to a terminal P_{12} and a negative supply voltage $-V$ applied to a terminal P_8 as its operating voltages.

An input signal applied to an input terminal T_{in} is transmitted to a first-stage differential amplifier circuit 10 through an input capacitor C_{100} . A terminal P_1 has earth potential applied thereto as a D.C. bias voltage by means of a resistor R_{100} . The first-stage differential amplifier circuit 10 comprises a differential pair of N-P-N transistors Q_{20} and Q_{21} , a transistor Q_{22} functioning as a constant-current source, and load resistors R_{21} and R_{22} .

Two differential output signals from the first-stage differential amplifier circuit 10 are applied to a driving differential amplifier circuit 11. The driving differential amplifier circuit 11 comprises a differential pair of P-N-P transistors Q_{23} and Q_{24} , an emitter resistors R_{23} , N-P-N transistors Q_{25} and Q_{26} forming constant-current loads, and a phase compensating capacitor C_{101} .

An output signal from the driving differential amplifier circuit 11 is transmitted to an emitter-follower circuit 12. The emitter-follower circuit 12 comprises transistors Q_{27} and Q_{28} connected as a Darlington pair, diodes D_{21} to D_{23} for adjusting an idling current, and a transistor Q_{29} functioning as a constant-current circuit.

Two output signals obtained from the emitter-follower circuit 12 are applied to an OCL type power output circuit 13. The OCL type power output circuit 12 comprises a quasi-complementary push-pull circuit which includes N-P-N transistors Q_{30} to Q_{32} , a P-N-P transistor Q_{33} , and emitter resistors R_{24} and R_{25} .

The output signal of the OCL type power output circuit 13 provided from a terminal P_{11} is transmitted to a loudspeaker SP through a switch SW of a relay RL. In addition, the output signal of the OCL type power circuit 13 provided from a terminal P_5 is applied to a terminal P_2 through a D.C. to A.C. negative feedback circuit 14 which comprises resistors R_{101} and R_{102} and a capacitor C_{102} .

Under the negative feedback action of the D.C. to A.C. negative feedback circuit 14, the output D.C.

level at the output terminals P_5 and P_{11} during normal operation of the OCL type power output circuit 13 follows the D.C. bias voltage (earth potential) applied to the terminal P_1 . At any abnormal operation of the OCL type power output circuit 13, however, the output D.C. level at the output terminals P_5 and P_{11} deviates from this to a positive or negative voltage.

A resistor R_{26} and a capacitor C_{103} which are connected to a terminal P_8 smooth the output signal of the OCL type power output circuit 13 so as to produce an output D.C. level V_o . Resistors R_{27} and R_{28} generate a D.C. level V_s subjected to a positive level shift, while resistors R_{29} and R_{30} generate a D.C. level V_s' subjected to a negative level shift.

Resistors R_{31} , R_{32} , R_{33} and R_{34} and a diode D_{24} are connected in series between the terminal P_{12} and the terminal P_8 , whereby reference voltages V_{ref1} , V_{ref2} and V_{ref3} are generated. The junction between the resistors R_{32} and R_{33} is connected to earth through a terminal P_7 , whereby the reference potential V_{ref2} is made equal to earth potential.

A differential amplifier circuit 15 comprises a detecting transistor Q_{34} , a reference transistor Q_{35} , a transistor Q_{36} functioning as a constant-current source, and diodes D_{25} and D_{26} . The relation of $V_{ref1} > V_s'$ is set so that, during normal operation of the OCL type power output circuit 13, the detecting transistor Q_{34} is turned "off" whereas the reference transistor Q_{35} is turned "on".

A differential amplifier circuit 16 comprises a reference transistor Q_{37} , a detecting transistor Q_{38} , a transistor Q_{39} functioning as a constant-current source, and diodes D_{27} and D_{28} . The relation of $V_{ref3} < V_s$ is set so that, during normal operation of the OCL type power output circuit 13, the reference transistor Q_{37} is turned "off" whereas the detecting transistor Q_{38} is turned "on".

A differential amplifier circuit 17 comprises a reference transistor Q_{40} , a detecting transistor Q_{41} , a transistor Q_{42} functioning as a constant-current source, and diodes D_{29} and D_{30} . The emitter current of the output transistor Q_{32} of the OCL type power output circuit 13 is detected by a current mirror circuit which is formed of a diode D_{31} and a transistor Q_{43} . Letting V_{cd} denote a detection voltage at the junction between resistors R_{35} and R_{36} , the resistance of the resistor R_{35} is set so that $V_{cd} > V_{ref2}$ may be met during the normal operation of the OCL type power output circuit 13 and that the reference transistor Q_{40} is turned "off" whereas the detecting transistor Q_{41} is turned "on".

The transistors Q_{36} , Q_{39} , and Q_{42} functioning as the constant-current sources are biased by the diode D_{24} . Thus, constant currents I_o flow through these transistors.

During normal operation of the OCL type power output circuit 13, the constant currents I_o flow through respective controlling transistors Q_{44} , Q_{45} and Q_{46} because the transistors Q_{35} , Q_{38} and Q_{41} are "on" in the differential amplifier current of $3 \cdot I_o$ flows through a diode D_{32} connected to the collector electrodes of the controlling transistors Q_{44} , Q_{45} and Q_{46} with the result that a driving transistor Q_{50} is turned "on". Thus, the relay RL is energized, the

contact SW is closed, and the output signal of the OCL type power output circuit 13 at the terminal P₁₁ is transmitted to the loudspeaker SP.

On the other hand, when the output D.C. level V_o of the OCL type power output circuit 13 has changed to a negative level due to abnormal operation thereof, the relation of $V_{ref3} > V_s$ occurs. As a result, the reference transistor Q₃₇ turns "on" whereas the detecting transistor Q₃₈ turns "off". Then, the constant current I_o flows through a controlling transistor Q₄₈, and a large current expressed by $I_o \times h_{FEQ51}$ flows through the collector electrode of a transistor Q₅₁. Thus, the driving transistor Q₅₀ is turned "off", and the output signal of the OCL type power output circuit 13 is not transmitted to the loudspeaker SP.

Alternatively, when the output D.C. level V_o of the OCL type power output circuit 13 has changed to a positive level on account of the abnormal operation thereof, the relation of $V_{ref1} < V_s$ occurs. As a result, the detecting transistor Q₃₄ turns "on" whereas the reference transistor Q₃₅ turns "off". Then, the constant current I_o flows through a controlling transistor Q₄₉, and the large current $I_o \times h_{FEQ51}$ flows through the collector electrode of the protective transistor Q₅₁. Similarly to the case previously described, the driving transistor Q₅₀ is turned "off", and the output signal of the OCL type power output circuit 13 is not transmitted to the loudspeaker SP.

When the emitter current of the output transistor Q₃₅ has increased abnormally due to the abnormal operation of the OCL type power output circuit 13 such as thermal runaway of the output transistor Q₃₅, the relation of $V_{cd} < V_{ref}$ occurs. As a result, the reference transistor Q₄₀ turns "on" whereas the detecting transistor Q₄₁ turns "off", to cause the constant current I_o to flow through a controlling transistor Q₄₇. Hence, the large current $I_o \times h_{FEQ51}$ flows through the collector electrode of the protective transistor Q₅₁, and the driving transistor Q₅₀ is turned "off".

Thus, in the case where any one of the various abnormal operations of the OCL type power output circuit 13 has occurred, the driving transistor Q₅₀ is turned "off" to disconnect the loudspeaker SP from the output of the OCL type power output circuit 13, whereby the loudspeaker can be protected from damage to its voice coil.

Furthermore, even when the transistor Q₃₈ or Q₄₁ among the detecting transistors Q₃₄, Q₃₈ and Q₄₁, becomes open-circuited, the reference transistor Q₃₇ or Q₄₀ turns "on" to open the contact SW of the relay RL. Thus, in case where an open circuit of the detecting transistor has occurred, the loudspeaker SP is disconnected from the output of the OCL type power output circuit 13, and hence, the enhancement of reliability can be achieved.

CLAIMS

1. A power output circuit including:
 - (a) load means to be driven by an output of said power output circuit;
 - (b) switching means connected between said output of the power output circuit and said load means;

(c) a first detector circuit for detecting a first operating status of the power output circuit;

(d) a second detector circuit for detecting a second operating status of the power output circuit;

(e) a first detecting transistor which receives an output signal of said first detector circuit;

(f) a second detecting transistor which receives an output signal of said second detector circuit; and

(g) a driving transistor which receives an output signal of said first detecting transistor and an output signal of said second detecting transistor and which operates to drive said switching means into an "off" or "on" state;

wherein under a condition in which said first operating status and said second operating status of said power output circuit lie in predetermined normal operating ranges, respectively, the first and second detecting transistors are biased respectively into "on" states by the first and second detector circuits so as to permit predetermined currents to flow therethrough, and wherein said driving transistor is controlled into an "on" state by said output signals of the first and second detecting transistors so as to drive the switching means into the "on" state;

said power output circuit further including:

(h) a first reference transistor which is connected to the first detecting transistor in a differential manner;

(i) a second reference transistor which is connected to the second detecting transistor in a differential manner;

(j) a first constant-current source which is connected to an emitter electrode of the first detecting transistor and an emitter electrode of said first reference transistor;

(k) a second constant-current source which is connected to an emitter electrode of the second detecting transistor and an emitter electrode of said second reference transistor;

(l) a protective transistor whose collector and emitter electrodes are respectively connected to a base electrode and an emitter electrode of the driving transistor;

(m) a first group of controlling transistors whose base-emitter junctions have collector signals of the first and second detecting transistors applied thereto and whose collector electrodes are connected to said base electrode of said driving transistor in common; and

(n) a second group of controlling transistors whose base-emitter junctions have collector signals of the first and second reference transistors applied thereto and whose collector electrodes are connected to a base electrode of said protective transistor in common;

wherein when said first operating status or said second operating status of said power output circuit has fallen outside the predetermined normal operating range, said protective transistor is controlled into an "on" state by collector signals of said second group of controlling transistors so as to control said driving transistor into an "off" state, thereby isolating said load means.

2. A power output circuit according to Claim 1,

contact SW is closed, and the output signal of the OCL type power output circuit 13 at the terminal P₁₁ is transmitted to the loudspeaker SP.

On the other hand, when the output D.C. level V_o of the OCL type power output circuit 13 has changed to a negative level due to abnormal operation thereof, the relation of $V_{ref3} > V_s$ occurs. As a result, the reference transistor Q₃₇ turns "on" whereas the detecting transistor Q₃₈ turns "off". Then, the constant current I_o flows through a controlling transistor Q₄₈, and a large current expressed by $I_o \times h_{FEQ51}$ flows through the collector electrode of a transistor Q₅₁. Thus, the driving transistor Q₅₀ is turned "off", and the output signal of the OCL type power output circuit 13 is not transmitted to the loudspeaker SP.

Alternatively, when the output D.C. level V_o of the OCL type power output circuit 13 has changed to a positive level on account of the abnormal operation thereof, the relation of $V_{ref1} < V_s$ occurs. As a result, the detecting transistor Q₃₄ turns "on" whereas the reference transistor Q₃₅ turns "off". Then, the constant current I_o flows through a controlling transistor Q₄₉, and the large current $I_o \times h_{FEQ51}$ flows through the collector electrode of the protective transistor Q₅₁. Similarly to the case previously described, the driving transistor Q₅₀ is turned "off", and the output signal of the OCL type power output circuit 13 is not transmitted to the loudspeaker SP.

When the emitter current of the output transistor Q₃₅ has increased abnormally due to the abnormal operation of the OCL type power output circuit 13 such as thermal runaway of the output transistor Q₃₅, the relation of $V_{cd} < V_{ref}$ occurs. As a result, the reference transistor Q₄₀ turns "on" whereas the detecting transistor Q₄₁ turns "off", to cause the constant current I_o to flow through a controlling transistor Q₄₇. Hence, the large current $I_o \times h_{FEQ51}$ flows through the collector electrode of the protective transistor Q₅₁, and the driving transistor Q₅₀ is turned "off".

Thus, in the case where any one of the various abnormal operations of the OCL type power output circuit 13 has occurred, the driving transistor Q₅₀ is turned "off" to disconnect the loudspeaker SP from the output of the OCL type power output circuit 13, whereby the loudspeaker can be protected from damage to its voice coil.

Furthermore, even when the transistor Q₃₈ or Q₄₁ among the detecting transistors Q₃₄, Q₃₈ and Q₄₁, becomes open-circuited, the reference transistor Q₃₇ or Q₄₀ turns "on" to open the contact SW of the relay RL. Thus, in case where an open circuit of the detecting transistor has occurred, the loudspeaker SP is disconnected from the output of the OCL type power output circuit 13, and hence, the enhancement of reliability can be achieved.

CLAIMS

1. A power output circuit including:

(a) load means to be driven by an output of said power output circuit;

(b) switching means connected between said output of the power output circuit and said load

means;

(c) a first detector circuit for detecting a first operating status of the power output circuit;

(d) a second detector circuit for detecting a second operating status of the power output circuit;

(e) a first detecting transistor which receives an output signal of said first detector circuit;

(f) a second detecting transistor which receives an output signal of said second detector circuit; and

(g) a driving transistor which receives an output signal of said first detecting transistor and an output signal of said second detecting transistor and which operates to drive said switching means into an "off" or "on" state;

wherein under a condition in which said first operating status and said second operating status of said power output circuit lie in predetermined normal operating ranges, respectively, the first and second detecting transistors are biased respectively into "on" states by the first and second detector circuits so as to permit predetermined currents to flow therethrough, and wherein said driving transistor is controlled into an "on" state by said output signals of the first and second detecting transistors so as to drive the switching means into the "on" state;

said power output circuit further including:

(h) a first reference transistor which is connected to the first detecting transistor in a differential manner;

(i) a second reference transistor which is connected to the second detecting transistor in a differential manner;

(j) a first constant-current source which is connected to an emitter electrode of the first detecting transistor and an emitter electrode of said first reference transistor;

(k) a second constant-current source which is connected to an emitter electrode of the second detecting transistor and an emitter electrode of said second reference transistor;

(l) a protective transistor whose collector and emitter electrodes are respectively connected to a base electrode and an emitter electrode of the driving transistor;

(m) a first group of controlling transistors whose base-emitter junctions have collector signals of the first and second detecting transistors applied thereto and whose collector electrodes are connected to said base electrode of said driving transistor in common; and

(n) a second group of controlling transistors whose base-emitter junctions have collector signals of the first and second reference transistors applied thereto and whose collector electrodes are connected to a base electrode of said protective transistor in common;

wherein when said first operating status or said second operating status of said power output circuit has fallen outside the predetermined normal operating range, said protective transistor is controlled into an "on" state by collector signals of said second group of controlling transistors so as to control said driving transistor into an "off" state, thereby isolating said load means.

2. A power output circuit according to Claim 1,



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wherein the first detector circuit detects the output D.C. level of the power output circuit, whilst the second detector circuit detects the level of the output current of an output transistor in the power output

5 circuit.

3. A power output circuit substantially as herein described with reference to Figures 1, 2 and 3 or Figure 4 or Figure 5 of the accompanying drawings.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1983.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.