PRESERVING THE ZERO MARK FOR WAFER ALIGNMENT

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to preserving the zero alignment mark for wafer alignment after wafer planarization and more particularly to preserving the primary or zero alignment mark for processes which use tungsten chemical mechanical polishing during the process sequence.

(2) DESCRIPTION OF THE RELATED ART

U.S. Pat. No. 5,496,777 to Moriyama describes a method of arranging alignment marks used in different process steps on scribing lines.

U.S. Pat. No. 5,532,520 to Haraguchi et al. describes alignment marks for the X direction alignment of a chip on a semiconductor wafer. The alignment marks comprise recesses and projections which are smaller than the X directional width of a grain on a metal film or the average particle size. The projections may be formed by an

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insulating layer formed on the semiconductor substrate.

U.S. Pat. No. 5,270,255 to Wong describes a method of metallization of an integrated circuit wafer which provides good step coverage and maintains a useful alignment mark. At least one contact opening to the semiconductor substrate and at least one lithography alignment cross mark opening structure are formed.

U.S. Pat. No. 5,627,624 to Yim et al. describes an integrated circuit test reticle for alignment mark optimization. A test reticle using alignment mark shapes, sizes, and depths is described.

U.S. Pat. No. 5,705,320 to Hsu et al. describes a method of preserving alignment marks after chemical mechanical polishing using a clear out window in the frame area of the contact via reticle.

U.S. Pat. No. 5,640,053 to Caldwell describes an inverse open frame alignment mark.

U.S. Pat. No. 5,271,798 to Sandhu et al. describes a method of selectively removing material from the alignment region of a wafer. Methods of confining etching materials to the alignment region are described.

SUMMARY OF THE INVENTION

Alignment marks are essential in photolithographic processing of semiconductor wafers for aligning the various masks used to pattern different levels of metallurgy and conductors to the wafer. As various processing steps are completed, care must be taken to insure that the alignment marks remain visible so that they can be used for subsequent processing steps. Fig. 1 shows a typical semiconductor wafer 10 having two alignment regions 12 and a device region 14. Fig. 2 shows typical alignment marks 22 formed in an alignment region 12 of the wafer 20. Typically the alignment marks 22 have sharp edges which can be detected automatically in a tool such as a wafer stepper used to project mask images onto the wafer. Wafer processing often comprises deposition of transparent layers of dielectric materials 24 such as silicon oxide or the like. After deposition of these transparent layers the alignment marks 22 are still visible and can still be detected using automatic means.

As shown in Fig. 3 metal conducting layers 26 are deposited on the dielectric layers 24. These metal conducting layers 26 are opaque and reflective and make the alignment marks 22 unusable unless steps are taken to preserve or recover the alignment marks. One method of

preserving the alignment marks is to etch away the dielectric in the alignment region before the metal is deposited, as shown in Fig. 4. With this method, however, subsequent wafer planarization, such as with chemical mechanical polishing, can distort the edges of the alignment marks 22 so that they lose effectiveness as alignment marks, as shown in Fig. 5.

It is a principle objective of this invention to provide a method of preserving alignment marks after metal layers have been deposited and the wafer has been planarized.

This objective is achieved by depositing a thicker layer of intermetal dielectric prior to the deposition of the metal layer. The metal layer is then deposited followed by planarization of the wafer. Since the dielectric is still in place in the alignment region the alignment marks are protected during the chemical mechanical polishing operation. The metal and dielectric are then etched away from the alignment regions of the wafer leaving the alignment marks in their original condition. The next layer of metal is then deposited and conform to the shape of the alignment marks so that the alignment marks can still be detected to align the wafer for subsequent process steps.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a top surface of a wafer showing two alignment regions.

Fig. 2 shows a cross section view of an alignment region of a wafer showing alignment marks and a layer of dielectric.

Fig. 3 shows a cross section view of an alignment region of a wafer with a layer of metal deposited on the layer of dielectric.

Fig. 4 shows a cross section of an alignment region of a wafer with the dielectric cleared from the alignment region before the layer of metal is deposited.

Fig. 5 shows a cross section view of an alignment region of a wafer with the dielectric cleared from the alignment region before the metal is deposited after planarization of the wafer.

Fig. 6 shows a cross section of an alignment region of a wafer after forming a layer of dielectric and depositing a layer of metal.

Fig. 7 shows a cross section of an alignment region of a wafer after forming a layer of dielectric, depositing a layer of metal, and planarizing the wafer.

Fig. 8 shows a cross section of an alignment region of a wafer after planarizing the wafer and removing dielectric from the alignment region.

Fig. 9 shows a cross section of an alignment region of a wafer after planarizing the wafer, removing dielectric from the alignment region, and depositing a subsequent layer of metal.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to Figs. 1, and 6-9 for a description of the preferred embodiment of this invention. Fig. 1 shows a top view of an integrated circuit wafer 10 having a device region 14 and two alignment regions 12. The device region 14 of the wafer is the region where the integrated circuit devices will be formed and interconnected. The alignment regions 12 of the wafer are reserved for alignment marks. Fig. 6 shows a cross section view of one of the alignment regions 12 having alignment marks 22 formed therein. In this example a layer of first conductor material 28, such as a metal, has been deposited in order to form conducting electrodes for the device region of the wafer. A layer of first intermetal dielectric, such as silicon oxide, has been deposited on the first layer of conductor material, however this first intermetal dielectric has been etched away from the alignment regions 12 in order to preserve the alignment marks 22 and is not shown in Fig. 6.

A layer of second conductor material 29, such as a metal, is then deposited in order to form conducting electrodes for the device region of the wafer. In the device region of the wafer, not shown here, the layer of second conductor material is formed on the layer of first intermetal dielectric. In the alignment regions, as shown

in Fig. 6, the layer of second conductor material 29 is deposited directly on the layer of first conductor material 28. The layer of first conductor material 28 and the layer of second conductor material 29 conform to the shape of the alignment marks 22 so that the alignment marks can still be used for accurate alignment of the wafer in a tool such as a wafer stepper.

The steps that follow are the key steps in this invention of a method to preserve alignment marks. As shown in Fig. 6, the alignment marks 22 are formed in an alignment region 12 having sidewalls and a bottom, the sidewalls having a depth 38 equal to a first thickness. The first thickness in this example is between about 36,000 and 44,000 Angstroms. Next, as shown in Fig. 6, a layer of second intermetal dielectric 30, having a second thickness, is deposited over the layer of second conductor material 29. The second intermetal dielectric 30 is a material such as silicon oxide or the like. The second thickness is increased over that which is often used for a second intermetal dielectric so that the second thickness is between about 18,000 and 20,000 Angstroms less than the first thickness, which is the depth of the sidewalls of the alignment region. In this example the second thickness is between about 20,000 and 22,000 Angstroms.

Next, as shown in Fig. 6, a layer of refractory metal 34, such as tungsten, having a thickness of between about 4000 and 5000 Angstroms is deposited on the layer of second intermetal dielectric 30. This example describes a layer of refractory metal 34 deposited on the layer of second intermetal dielectric 30. Those skilled in the art will recognize that the method of this invention will also work if a layer of other metal or amorphous silicon is deposited on the layer of intermetal dielectric 30 instead of the layer of refractory metal. The refractory metal 34 is typically used to fill via holes in the device region of the wafer, not shown. Next, as shown in Fig. 7, the wafer is planarized using a method such as chemical mechanical polishing. This planarization removes the refractory metal 34 from the top surface of the layer of second intermetal dielectric 30. The dishing effect of the planarization helps in removing the metal from the alignment region.

As shown in Fig. 8, a resist mask is then formed protecting the device region of the wafer and any refractory metal remaining in the alignment region of the wafer is etched away. The second intermetal dielectric is then etched away from the alignment region using dry etching with an etchant of CHF_3 + CF_4. The etching method and etchant are chosen to provide a strong oxide etch, which also helps to remove any remaining metal or metal residue.

As shown in Fig. 9, a layer of third conductor material 36, such as aluminum copper or the like, or a layer of other opaque material can then be deposited on the wafer and the alignment marks 22 are preserved. In the alignment region the layer of third conductor material 36 is deposited directly on the layer of second conducting material 29. In this method the layer of second intermetal dielectric protects the alignment marks during the chemical mechanical polishing operation. The second intermetal dielectric is then etched away and the alignment marks are preserved after deposition of the layer of third conductor material.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

1. A method of preserving alignment marks, comprising:

providing a semiconductor wafer having alignment regions and device regions;

providing alignment marks formed in said alignment regions;

forming a patterned layer of first conducting material on said alignment regions and said device region of said semiconductor wafer;

forming a layer of first intermetal dielectric on said layer of first conducting material;

clearing said first intermetal dielectric from said alignment regions;

forming a patterned layer of second conducting material on said alignment regions and said device regions of said semiconductor wafer, thereby forming alignment regions having sidewalls with a first thickness;

forming a layer of second intermetal dielectric having a second thickness on said alignment regions and said device regions of said semiconductor wafer, wherein said second thickness is between about 18,000 and 20,000 Angstroms less than said first thickness;

depositing a layer of refractory metal on said layer of second intermetal dielectric;

planarizing said semiconductor wafer after depositing said layer of refractory metal;

forming a photoresist mask on said wafer after planarizing said wafer wherein said photoresist mask covers said device regions and does not cover said alignment regions of said wafer;

etching away said refractory metal from said alignment regions of said wafer using said photoresist mask;

etching away said second intermetal dielectric from said alignment regions of said wafer using said photoresist mask;

removing said photoresist mask; and

forming a patterned layer of third conducting material on said wafer.

2. The method of claim 1 wherein said planarizing said semiconductor wafer uses chemical mechanical polishing.

3. The method of claim 1 wherein said layer of refractory metal is a layer of tungsten having a thickness of between about 4000 and 5000 Angstroms.

4. The method of claim 1 wherein said first thickness is between about 36,000 and 44,000 Angstroms.

5. The method of claim 1 wherein said second thickness is between about 20,000 and 22,000 Angstroms.

6. The method of claim 1 wherein said etching away said second intermetal dielectric from said alignment regions uses dry etching with an etchant of CHF_3 + CF_4.

7. The method of claim 1 wherein said second intermetal dielectric is silicon oxide.

8. The method of claim 1 wherein said layer of third conducting material is a layer of aluminum copper.

9. The method of claim 1 wherein said layer of third conducting material is a layer of opaque material.

10. The method of claim 1 wherein said layer of first intermetal dielectric is a layer of silicon oxide.

11. A method of preserving alignment marks, comprising:

providing a substrate having alignment regions and device regions, wherein said alignment regions have sidewalls having a first thickness and bottoms;

providing alignment marks formed on said bottoms of said alignment regions;

forming a layer of intermetal dielectric having a second thickness on said alignment regions and said device regions of said semiconductor wafer, wherein said second thickness is between about 18,000 and 20,000 Angstroms less than said first thickness;

depositing a layer of refractory metal on said layer of intermetal dielectric;

planarizing said substrate;

forming a photoresist mask on said substrate after planarizing said substrate wherein said photoresist mask does not cover said alignment regions of said substrate;

etching away said refractory metal from said alignment regions of said substrate using said photoresist mask;

etching away said intermetal dielectric from said alignment region of said wafer using said photoresist mask; and

removing said photoresist mask.



12. The method of claim 11 wherein said substrate is a semiconductor integrated circuit wafer.

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13. The method of claim 11 wherein said planarizing said substrate uses chemical mechanical polishing.

14. The method of claim 11 wherein said layer of refractory metal is a layer of tungsten having a thickness of between about 4000 and 5000 Angstroms.

15. The method of claim 11 wherein said first thickness is between about 36,000 and 44,000 Angstroms.

16. The method of claim 11 wherein said second thickness is between about 20,000 and 22,000 Angstroms.

17. The method of claim 11 wherein said etching away said intermetal dielectric from said alignment regions uses dry etching with an etchant of CHF_3 + CF_4.

18. The method of claim 1 wherein said intermetal dielectric is silicon oxide.