(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 October 2003 (02.10.2003)

PCT

(10) International Publication Number
WO 03/081678 A1

(51) International Patent Classification[7]: H01L 29/786

(21) International Application Number: PCT/US02/40399

(22) International Filing Date:
17 December 2002 (17.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/104,319 21 March 2002 (21.03.2002) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, P.O. Box 3453, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: WEI, Andy, C.; 9323 Manchaca Rd #125, Austin, TX 78748 (US). WRISTERS, Derick, J.; 13710 Overland Pass, Bee Caves, TX 78738 (US). FUSELIER, Mark, B.; 12232 Barrel Bend, Austin, TX 78748 (US).

(74) Agent: DRAKE, Paul, S.; Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, Mail Stop 562, Austin, TX 78741 (US).

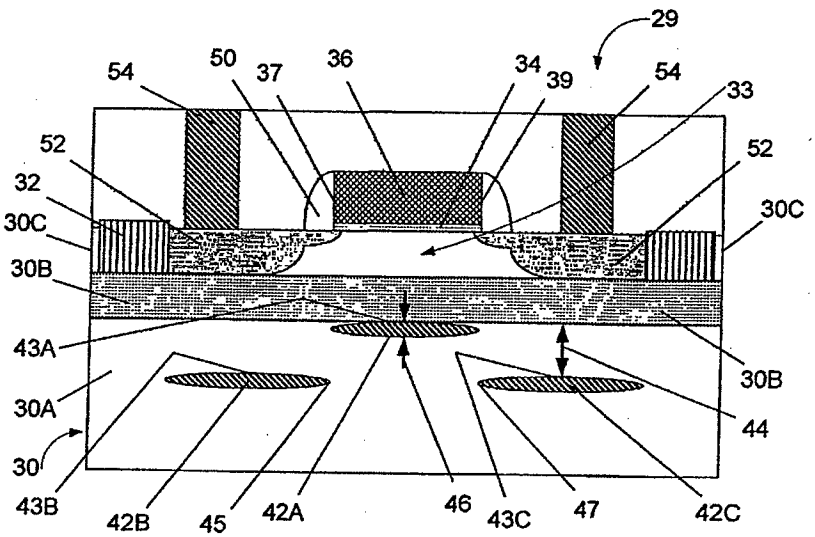
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: DOPING METHODS FOR FULLY-DEPLETED SOI STRUCTURES, AND DEVICE COMPRISING THE RESULTING DOPED REGIONS



(57) Abstract: The present invention is generally directed to doping methods for fully-depleted SOI structures, and a device comprising such resulting doped regions. In one illustrative embodiment, the device comprises a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate (30A), a buried oxide layer (30B) and an active layer (30C), the transistor being comprised of a gate electrode (36), the bulk substrate (30A) being doped with a dopant material at a first concentration level. The device further comprises a first doped region (42A) formed in the bulk substrate (30A), the first doped region (42A) being doped with a dopant material that is the same type as the bulk substrate dopant material, wherein the concentration level of dopant material in the first doped region (42A) is greater than the first dopant concentration level in the bulk substrate (30A), the first doped region (42A) being substantially aligned with the gate electrode (36).

WO 03/081678 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.