VIA ELECTROMIGRATION IMPROVEMENT BY CHANGING THE VIA BOTTOM GEOMETRIC PROFILE

ABSTRACT

An integration approach to improve electromigration resistance in a semiconductor device is described. A via is formed in a stack that includes an upper dielectric layer, a middle TiN ARC, and a lower first metal layer and is filled with a conformal diffusion barrier layer and a second metal layer. A key feature is that the etch process which forms the via may be selected to vary the shape and location of the via bottom. A round or partially rounded bottom is formed in the first metal layer to reduce mechanical stress near the diffusion barrier layer. On the other hand, a flat bottom which stops on or in the TiN ARC is selected when exposure of the first metal layer to subsequent processing steps is a primary concern. Electromigration resistance is higher than for a via structure with a flat bottom formed in a first metal layer.

Fig. 11