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A DUAL METAL GATE PROCESS: METALS AND THEIR SILICIDES

RELATED PATENT APPLICATION

U.S. Patent Application Serial # 09/___,___ to the same inventors, filed on _____. (CS-00-114)

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The present invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of fabricating dual-metal transistors having different work functions in the fabrication of integrated circuits.

(2) DESCRIPTION OF THE PRIOR ART

It is anticipated that a single metal gate with mid-gap work function values will not be suitable for CMOS applications due to buried channel effects. By using a single metal gate for both NMOSFET and PMOSFET, the threshold voltage becomes too high for both types of transistors. In order to achieve a lower threshold voltage, additional implantation is required and this will result in buried channel effects. The short channel effect control will then be degraded. However, with dual metal gates having different

metal layer in the second active area to form an implanted metal layer and the implanted metal layer is silicided to form a second metal silicide layer wherein the silicon concentration in the second metal silicide layer is higher than the silicon concentration in the first metal silicide layer. Thereafter, the first metal silicide layer and the second metal silicide layer are patterned to form a first metal silicide gate in the first area and a second metal silicide gate in the second area to complete formation of dual-metal gate CMOS transistors in the fabrication of an integrated circuit. The PMOS gate will be formed from the gate having the higher work function.

Also, in accordance with the objects of the invention, a fourth method for forming dual-metal gate CMOS transistors is achieved. First and second active areas of a semiconductor substrate are separated by isolation regions. One of the active areas will be PMOS and the other will be NMOS. A dummy gate is formed in each of the active areas. The dummy gates are covered with a dielectric layer which is planarized whereby a top surface of each of the dummy gates is exposed. The exposed dummy gates are removed, leaving gate openings to the semiconductor substrate. A gate dielectric layer is formed overlying the semiconductor substrate in each of the gate openings. A metal layer is

deposited within the gate openings to form metal gates. First silicon ions are implanted into the metal gate only in a first active area to form an implanted metal gate. The implanted metal gate is silicided to form a first metal silicide gate in the first active area. Second silicon ions are implanted into the metal gate in the second active area to form an implanted metal gate and the implanted metal gate is silicided to form a second metal silicide gate wherein the silicon concentration in the second metal silicide gate is different from the silicon concentration in the first metal silicide gate to complete formation of dual-metal gate CMOS transistors in the fabrication of an integrated circuit. The PMOS gate will be formed from the gate having the higher work function.

Also, in accordance with the objects of the invention, a dual-metal gate CMOS integrated circuit device is achieved. The device comprises first and second active areas of a semiconductor substrate separated by isolation regions. One of the active areas will be PMOS and the other will be NMOS. A metal gate in the first active area overlies a gate dielectric layer, and a metal silicide gate in the second active area overlies a gate dielectric layer wherein the metal in the metal gate is the same material as the metal in the metal silicide gate. The metal silicide may have a

higher or lower work function depending on the metal used. The PMOS gate will be formed from the gate having the higher work function.

Also, in accordance with the objects of the invention, another dual-metal gate CMOS integrated circuit device is achieved. The device comprises first and second active areas of a semiconductor substrate separated by isolation regions. One of the active areas will be PMOS and the other will be NMOS. A first metal silicide gate in the first active area overlies a gate dielectric layer, and a second metal silicide gate in the second active area overlies a gate dielectric layer wherein the metal in the two gates is the same metal and the silicon concentration is different in each of the two gates. The PMOS gate will be formed from the gate having the higher work function.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 5 are cross-sectional representations of a first preferred embodiment of the present invention.

Figs. 6 through 11 are cross-sectional representations of a second preferred embodiment of the present invention.

Figs. 12 and 13 are cross-sectional representations of two alternatives of a third preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention uses a metal and its metal silicide to form dual-metal gates having different work functions. In one embodiment, two different silicides of the metal are used as the dual-metal gates. It will be understood by those skilled in the art that the invention should not be limited to the embodiments described herein, but can be extended and applied to any application in which it is desired to have metal gates having differing work functions. The first embodiment of the invention will be described with reference to Figs. 1-5. The second embodiment of the invention will be described with reference to Figs. 6-11. The third embodiment of the invention will be described with reference to Figs. 12 and 13.

Referring now to Figs. 1-5, the first preferred embodiment of the present invention will be described. Referring now more particularly to Fig. 1, there is shown a semiconductor substrate 10. This is preferably monocrystalline silicon. Isolation regions, such as shallow trench isolation (STI) 12, are formed in the substrate to separate active regions. N-wells and P-wells, not shown, may be formed within the substrate, as is conventional. Punchthrough and threshold voltage adjustment implantations, not shown, are made as is conventional in the art.

A gate dielectric layer 14 is grown or deposited over substrate to a thickness of between about 15 and 150 Angstroms. For example, the dielectric layer may be a low dielectric constant material such as silicon dioxide, nitrided silicon dioxide, silicon nitride, or their combinations. Alternatively, the dielectric layer may be a high dielectric constant gate dielectric material such as zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxide.

Referring now to Fig. 2, a metal layer 16 is formed over the gate dielectric layer to a thickness of between about 500 and 3000 Angstroms. The metal layer 16 may be formed by sputtering, evaporation, chemical vapor

deposition (CVD), or electroplating. The deposited metal can be platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, or chromium.

Now, the metal layer is masked 20, as shown in Fig. 3, to expose a region where the metal will be silicided. Silicon ions are implanted 24 into the metal layer 16 where it is not covered by the mask 20. Silicon ions are implanted with a dosage of between about 5 E 15 to 5 E 17 ions/cm^2 and an energy of between about 1 to 50 KeV. It is important that the masking layer is thick enough to protect the underlying metal layer from implantation. The silicidation process is now to be accomplished by annealing in an inert gas ambient. Annealing can be performed in a furnace, rapid thermal process (RTP), or a laser system. The photomask must be removed prior to annealing in the inert gas. Silicided metal region 28 is the result of the silicidation process.

Referring now to Fig. 4, the metal and metal silicide layers, 16 and 28, respectively, are patterned to form gate electrodes. A chemical mechanical polishing (CMP) process may be applied to achieve planarization. In one embodiment, the silicide 28 is patterned to form the first

gate electrode and, subsequently, the metal layer is patterned to form the second gate electrode. In another embodiment, both gate electrodes are defined and etched at the same time. The etching can be achieved by alternating chemistry 1 and chemistry 2 with time and using a high selectivity etch chemistry when the etch process is getting close to the end point, with chemistry 1 having a higher etch rate for silicide and chemistry 2 having a higher etch rate for the metal, or vice versa. Thus, metal gates 16 and 28, having different work functions, are realized.

The metal silicide gate 28 may have a higher or lower work function than the metal gate 16 depending on the metal used. The PMOS gate will be the gate having the higher work function and the NMOS gate will be the gate having the lower work function.

Referring now to Fig. 5, source/drain regions 30 and sidewall spacers 32 may be formed, as is conventional. The spacers 32 may comprise either silicon nitride or silicon oxide. Processing continues as is conventional in the art, except that silicidation over the gates is not required.

The second preferred embodiment of the present invention will be described with reference to Figs. 6-11.

This embodiment is a damascene gate process. Referring now more particularly to Fig. 6, there is shown a semiconductor substrate 10. This is preferably monocrystalline silicon. Isolation regions, such as shallow trench isolation (STI) 12, are formed in the substrate to separate active regions. N-wells and P-wells, not shown, may be formed within the substrate, as is conventional. Punchthrough and threshold voltage adjustment implantations, not shown, are made as is conventional in the art.

Dummy gates are formed. A first layer of silicon oxide 42 is deposited over the substrate to a thickness of between about 15 and 150 Angstroms. A layer of silicon nitride 44 is deposited over the silicon oxide layer 42 to a thickness of between about 15 and 200 Angstroms. A layer of polysilicon 46 is deposited over the silicon nitride layer 44 to a thickness of between about 500 and 3000 Angstroms. The dummy gate stack is patterned to form a dummy gate 50 in each of the active areas, as shown in Fig. 6. Sidewall spacers 54 and source/drain regions 52 are formed as is conventional in the art. Now, an interlevel dielectric layer 58 is deposited over the dummy gates and planarized to the top of the dummy gates by CMP.

As shown in Fig. 7, the dummy gates 50 are removed where they are exposed by the CMP process. The dummy gates are removed by wet etching, dry etching, or a combination of the two.

Now, the dual-metal gates of the present invention are to be formed. A gate dielectric layer 60 is deposited or thermally grown on the exposed substrate surface within the gate openings to a thickness of between about 15 and 150 Angstroms, as shown in Fig. 8. As in the first embodiment, the dielectric layer may be a low dielectric constant material such as silicon dioxide, nitrided silicon dioxide, silicon nitride, or their combinations or a high dielectric constant gate dielectric material such as zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxide.

Referring now to Fig. 9, a metal layer 62 is formed over the gate dielectric layer 60. The metal layer 62 may be deposited by sputtering or CVD, for example. The deposited metal can be platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, or chromium. A CMP process polishes away the metal layer not within the gate openings, thus completing the damascene process.

Now, as shown in Fig. 10, a photomask 65 is formed to cover the intermetal dielectric layer 58 and the first gate. An opening is formed in the photomask to expose only the second gate that is to be silicided. Silicon ions are implanted 69 by a low energy implanter into the second gate where it is not covered by the mask 65. Silicon ions are implanted with a dosage of between about 5 E 15 to 5 E 17 ions/cm^2 and an energy of between about 1 to 50 KeV. It is important that the masking layer is thick enough to protect the first gate from implantation.

After stripping the photomask 65, an annealing step in an inert gas or a vacuum is performed to form a silicide from the silicon-implanted metal 72.

As shown in Fig. 11, metal gates 62 and 72, having different work functions, are realized. Gate 62 comprises a metal while gate 72 comprises metal silicide. The gate electrode with the higher work function will be the PMOSFET while the gate electrode with the lower work function will be the NMOSFET.

The work functions of the gate electrodes of the first two embodiments have been measured as shown in Table 1. The resistivity of almost all metals and their

silicides is much lower than the resistivity of polysilicon.

Table 1

gate material	work func (eV)
Pt	5.32 - 5.5
$PtSi_2$	~4.62
Ti	3.95 - 4.33
$TiSi_2$	~4.38
Ni	4.5 - 5.3
$NiSi_2$	~4.55
Co	4.41 - 5.00
$CoSi_2$	~4.52
Ta	4.12 - 4.25
$TaSi_2$	~4.35
Mo	4.3 - 4.6
$MoSi_2$	~4.42
W	4.1 - 5.2
WSi_2	~4.43
Zr	3.9 - 4.05
$ZrSi_2$	~4.33
Hf	N/A
$HfSi_2$	N/A
V	4.12 - 4.3
VSi_2	~4.37
Pd	4.8 - 5.22
PdSi	~4.6
Cr	4.5 - 4.6
$CrSi_2$	~4.41

The dual-metal gate can also be realized by adjusting the work function of the silicides since the work function of the metal silicides is closely related to the stoichiometry. That is, one gate electrode will be in the form of MSi_x while the other gate electrode will be in the form of MSi_y, where M is a metal which can be platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten,

zirconium, hafnium, vanadium, palladium, or chromium, and X is not equal to Y. The value of X and Y can be well adjusted by the implantation dose. The methods described for the first and second embodiments can also be used in this third embodiment dual-gate process.

As shown in Fig. 12, the conventional gate formation process described in the first embodiment can be used to form the two gates MSi_x and MSi_y. The metal layer can be implanted with two different dosages of silicon ions to form these two metal silicide gates having different work functions. For example, a first silicon ion dosage of between about 1 E 15 and 1 E 16 ions/cm^2 will form a gate having a lower work function and a second silicon ion dosage of between about 1 E 16 and 1 E 17 ions/cm^2 will form a gate having a higher work function.

Alternatively, instead of depositing an elemental metal layer for gate electrode 1, a silicide with a certain M/Si ratio can be deposited by CVD or sputtering. This will form the first gate electrode MSi_x. The stoichiometry of the second electrode MSi_y can be adjusted by the silicon ion implantation as described with for the first embodiment. For example, the silicon concentration of the first gate electrode having a lower work function is between

about 1 E 21 and 1 E 22 ions/cm^3 and the silicon concentration of the second gate electrode having a higher work function is between about 1 E 22 and 1 E 23 ions/cm^3.

As shown in Fig. 13, the damascene gate process described in the second embodiment can be used to form the two gates MSi_x and MSi_y. The gates will each be implanted with different dosages of silicon ions to form these two metal silicide gates having different work functions. Again, as an alternative, instead of depositing an elemental metal layer for gate electrode 1, a silicide with a certain M/Si ratio can be deposited by CVD or sputtering. This will form the first gate electrode MSi_x. The stoichiometry of the second electrode MSi_y can be adjusted by the silicon ion implantation as described with for the second embodiment.

The process of the present invention provides three simple, manufacturable dual-metal gate processes. The conventional CMOS process flow is maintained. The work function of the gates is simply tuned by the silicidation process. The dual-metal gates comprise a metal and a metal silicide, or two metal silicides having different work functions. The metal silicide having the higher work function will be used for the PMOS gate and the metal

silicide having the lower work function will be used for the NMOS gate.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a gate dielectric layer overlying said semiconductor substrate in each of said active areas;

depositing a metal layer overlying said gate dielectric layer;

implanting silicon ions into said metal layer in said first active area to form an implanted metal layer and siliciding said implanted metal layer to form a metal silicide layer; and

thereafter patterning said metal layer and said metal silicide layer to form a metal gate in said second active area and a metal silicide gate in said first active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

2. The method according to Claim 1 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

3. The method according to Claim 1 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

4. The method according to Claim 1 wherein said metal layer is selected from the group containing platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, and chromium.

5. The method according to Claim 1 wherein said silicon ions are implanted at a dosage of between about 5 E 15 and 5 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

6. The method according to Claim 1 wherein said step of siliciding said implanted metal layer comprises annealing in an inert gas and wherein said annealing is

performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

7. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a dummy gate in each of said active areas;

covering said dummy gates with a dielectric layer;

planarizing said dielectric layer whereby a top surface of each of said dummy gates is exposed;

removing said exposed dummy gates leaving gate openings to said semiconductor substrate;

forming a gate dielectric layer overlying said semiconductor substrate in each of said gate openings;

depositing a metal layer within said gate openings to form metal gates; and

implanting silicon ions into said metal gate only in said first active area to form an implanted metal gate and siliciding said implanted metal gate to form a metal silicide gate in said first active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function

than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

8. The method according to Claim 7 wherein said dummy gates comprise a first layer of silicon dioxide, a second layer of silicon nitride, and a third layer of polysilicon.

9. The method according to Claim 7 wherein said step of removing said dummy gates is selected from the group containing: wet etching, dry etching, and a combination of wet and dry etching.

10. The method according to Claim 7 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

11. The method according to Claim 7 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

12. The method according to Claim 7 wherein said metal layer is selected from the group containing platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, and chromium.

13. The method according to Claim 7 wherein said silicon ions are implanted at a dosage of between about 5 E 15 and 5 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

14. The method according to Claim 7 wherein said step of siliciding said implanted metal layer comprises annealing in an inert gas or vacuum wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

15. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a gate dielectric layer overlying said semiconductor substrate in each of said active areas;

depositing a metal layer overlying said gate dielectric layer;

implanting first silicon ions into said metal layer in said first active area to form an implanted metal layer and siliciding said implanted metal layer to form a first metal silicide layer;

implanting second silicon ions into said metal layer in said second active area to form an implanted metal layer and siliciding said implanted metal layer to form a second metal silicide layer wherein said first metal silicide layer has a different silicon concentration from said second metal silicide layer; and

thereafter patterning said first and second metal silicide layers to form a first metal silicide gate in said first active area and a second metal silicide gate in said second active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

16. The method according to Claim 15 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon

nitride, and a combination thereof.

17. The method according to Claim 15 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

18. The method according to Claim 15 wherein said metal layer is selected from the group containing platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, and chromium.

19. The method according to Claim 15 wherein said first silicon ions are implanted at a dosage of between about 5 E 15 and 5 E 16 ions/cm^2 and an energy of between about 1 and 50 KeV.

20. The method according to Claim 15 wherein said second silicon ions are implanted at a dosage of between about 5 E 16 and 5 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

21. The method according to Claim 15 wherein said steps of siliciding said implanted metal layer comprises annealing in an inert gas wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

22. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a dummy gate in each of said active areas;

covering said dummy gates with a dielectric layer;

planarizing said dielectric layer whereby a top surface of each of said dummy gates is exposed;

removing said exposed dummy gates leaving gate openings to said semiconductor substrate;

forming a gate dielectric layer overlying said semiconductor substrate in each of said gate openings;

depositing a metal layer within said gate openings to form metal gates;

implanting first silicon ions into said metal gate only in said first active area to form an implanted metal gate and siliciding said implanted metal gate to

form a first metal silicide gate in said first active area; and

implanting second silicon ions into said metal gate only in said second active area to form an implanted metal gate and siliciding said implanted metal gate to form a second metal silicide gate in said second active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

23. The method according to Claim 22 wherein said dummy gates comprise a first layer of silicon dioxide, a second layer of silicon nitride, and a third layer of polysilicon.

24. The method according to Claim 22 wherein said step of removing said dummy gates is selected from the group containing: wet etching, dry etching, and a combination of wet and dry etching.

25. The method according to Claim 22 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon

nitride, and a combination thereof.

26. The method according to Claim 22 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

27. The method according to Claim 22 wherein said metal layer is selected from the group containing platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, and chromium.

28. The method according to Claim 22 wherein said first silicon ions are implanted at a dosage of between about 5 E 15 and 5 E 16 ions/cm^2 and an energy of between about 1 and 50 KeV.

29. The method according to Claim 22 wherein said second silicon ions are implanted at a dosage of between about 5 E 16 and 5 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

30. The method according to Claim 22 wherein said steps of siliciding said implanted metal layer comprises annealing in an inert gas or vacuum wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

31. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a gate dielectric layer overlying said semiconductor substrate in each of said active areas;

depositing a first metal silicide layer overlying said gate dielectric layer;

implanting silicon ions into said first metal silicide layer in said first active area and siliciding implanted said first metal silicide layer to form a second metal silicide layer having a different silicon concentration than said first metal silicide layer; and

thereafter patterning said first and second metal silicide layers to form a first metal silicide gate in said first active area and a second metal silicide gate

in said second active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

32. The method according to Claim 31 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

33. The method according to Claim 31 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

34. The method according to Claim 31 wherein said first metal silicide layer is selected from the group containing platinum silicide, titanium silicide, nickel silicide, cobalt silicide, tantalum silicide, molybdenum silicide, tungsten silicide, zirconium silicide, hafnium silicide, vanadium silicide, palladium silicide, and chromium silicide.

35. The method according to Claim 31 wherein said steps of siliciding said implanted metal layer comprises annealing in an inert gas wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

36. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a dummy gate in each of said active areas;

covering said dummy gates with a dielectric layer;

planarizing said dielectric layer whereby a top surface of each of said dummy gates is exposed;

removing said exposed dummy gates leaving gate openings to said semiconductor substrate;

forming a gate dielectric layer overlying said semiconductor substrate in each of said gate openings;

depositing a first metal silicide layer within said gate openings to form first metal silicide gates; and

implanting silicon ions into said metal silicide gate only in said first active area to form an implanted metal silicide gate and siliciding said implanted metal

silicide gate to form a second metal silicide gate in said first active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

37. The method according to Claim 36 wherein said dummy gates comprise a first layer of silicon dioxide, a second layer of silicon nitride, and a third layer of polysilicon.

38. The method according to Claim 36 wherein said step of removing said dummy gates is selected from the group containing: wet etching, dry etching, and a combination of wet and dry etching.

39. The method according to Claim 36 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

40. The method according to Claim 36 wherein said gate dielectric layer is selected from the group containing

zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

41. The method according to Claim 36 wherein said metal silicide layer is selected from the group containing platinum silicide, titanium silicide, nickel silicide, cobalt silicide, tantalum silicide, molybdenum silicide, tungsten silicide, zirconium silicide, hafnium silicide, vanadium silicide, palladium silicide, and chromium silicide.

42. The method according to Claim 36 wherein said step of siliciding said implanted metal silicide layer comprises annealing in an inert gas or vacuum wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

43. A dual-metal gate CMOS integrated circuit device comprising:

an NMOS active area and a PMOS active area of a semiconductor substrate separated by isolation regions;

a metal gate in said NMOS area over a gate dielectric layer; and

a metal silicide gate in said PMOS area over a gate dielectric layer wherein said metal in said metal gate is the same material as said metal in said metal silicide gate and wherein said metal silicide gate in said PMOS area has a higher work function than said metal gate in said NMOS area.

44. The device according to Claim 43 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

45. The device according to Claim 43 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

46. The device according to Claim 43 wherein said metal layer is selected from the group containing platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, and chromium.

47. A dual-metal gate CMOS integrated circuit device comprising:

an NMOS active area and a PMOS active area of a semiconductor substrate separated by isolation regions;

a metal gate in said PMOS area over a gate dielectric layer; and

a metal silicide gate in said NMOS area over a gate dielectric layer wherein said metal in said metal gate is the same material as said metal in said metal silicide gate and wherein said metal gate in said PMOS area has a higher work function than said metal silicide gate in said NMOS area.

48. The device according to Claim 47 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

49. The device according to Claim 47 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

50. The device according to Claim 47 wherein said metal layer is selected from the group containing platinum, titanium, nickel, cobalt, tantalum, molybdenum, tungsten, zirconium, hafnium, vanadium, palladium, and chromium.

51. A dual-metal gate CMOS integrated circuit device comprising:

an NMOS active area and a PMOS active area of a semiconductor substrate separated by isolation regions;

a first metal silicide gate in said NMOS area over a gate dielectric layer; and

a second metal silicide gate in said PMOS area over a gate dielectric layer wherein said metal in said first metal silicide gate is the same material as said metal in said second metal silicide gate and wherein the concentration of silicon in said first metal silicide gate is different from said the concentration of silicon in said second metal silicide gate and wherein said second metal silicide gate has a higher work function than said first metal silicide gate.

52. The device according to Claim 51 wherein said gate dielectric layer is selected from the group containing silicon dioxide, nitrided silicon dioxide, silicon

nitride, and a combination thereof.

53. The device according to Claim 51 wherein said gate dielectric layer is selected from the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

54. The device according to Claim 51 wherein said metal silicide is selected from the group containing platinum silicide, titanium silicide, nickel silicide, cobalt silicide, tantalum silicide, molybdenum silicide, tungsten silicide, zirconium silicide, hafnium silicide, vanadium silicide, palladium silicide, and chromium silicide.