

ABSTRACT OF THE INVENTION

Circuit Array Substrate

Poly-silicon semiconductor layer 21 and dummy poly-silicon semiconductor layer 25 are formed in insulation from each other on glass substrate 3. Gate insulation film 31 is formed on poly-silicon semiconductor layer 21, dummy poly-silicon semiconductor layer 25 and glass substrate 3. Gate insulation film 31 is covered with scanning and gate lines 11, which is overlapped with poly-silicon semiconductor layer 21 and dummy poly-silicon semiconductor layer 25. Poly-silicon semiconductor layer 21 is coupled with scanning and gate line 11 to define capacitors Ca and is also coupled with a reference potential to define capacitor Cb. Likewise, dummy poly-silicon semiconductor layer 25 is coupled with scanning and gate line 11 to define capacitors Cc and is also coupled with a reference potential to define capacitor Cd. Capacitors Cc and Cd increase capacitance in parallel with those Ca and Cb to suppress increase in voltage applied to gate insulation film 31 between scanning and gate line 11 and poly-silicon semiconductor layer 21 due to electrostatic charges generated in a process after the formation of scanning and gate lines 11. Thus, it can suppress electrostatic breakdown at gate insulation film 31 and point defects of pixels 5.

Fig. 1



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