The invention relates to a circuit for transformation.

The article "High-Speed Discrete Cosine Transformation with the Aid of the µPD 77230" appeared on pages 91-96 of the magazine "Design & Elektronik", published by "Markt und Technik", Edition 20 of 30.09.1986. The associated block circuit diagram of the micro PD appeared on page 92. The 55-bit floating-decimal-point ALU processes one complete set of optical and logic operations.

US-A- 4293920 has described an analogue transformation circuit which can process only positive input signals and wherein the negative weighting of transformation coefficients is carried by means of a special circuit with FETs. The input signal is not split in respect of absolute value and sign.

The aim of the invention is to provide a circuit which permits a high-speed calculation of transformation values.

This aim is fulfilled by the features of Claim 1. Advantageous further developments of the invention are described in the dependent claims.

To facilitate the understanding of the invention an exemplary embodiment will be explained in detail in the following making reference to drawings wherein:

Figure 1 is a block circuit diagram and
Figure 2 illustrates a multiplication circuit for the calculation of transformation values.

Figure 1 shows a data bus 1 via which binary signals D0-D7 are transmitted from an input 2 to transformers 3 - 10. Via a further data bus 11 with a line, further digital signals are transmitted from an input 12 to the transformers 3 - 10

and to a multiplier 13. The multiplier 13 is advantageously formed by a PROM (programmable read only memory) 87S421 manufactured by the National Semiconductor Company. On the data line of the data bus 11 the data signal indicates whether either a 8*8 or 2*(4*8) DCT (discrete cosine transformation) matrix is being used. The signals on the data buses 1 and 11 function as address at the inputs of the transformers 3 - 10 and of the multiplier 13. As a factor stored in the transformers 3 - 10 amounts at the maximum to 1.4, advantageously the MSB (most significant bit) is externally calculated by the multiplier 13 and then emitted to the individual transformers 3 - 10. The LSBs (least significant bits) are generated in multipliers present in the transformers 3 - 10. The multiplier 13 transfers the MSB as digital signal from its outputs via eight data lines to an intermediate store 14. The intermediate store 14 intermediately stores the MSB and feeds it to the transformers 3 - 10 via eight data lines, in each case one data line for one transformer. Multiplications, additions and subtractions, and buffering take place in each of the transformers 3 - 10. The transformers 3 - 10 transform the data items present at the input 2 into a different domain.

In the case of a forwards transformation procedure, data items from the time domain are transformed into the frequency domain, whereas in the case of a reverse transformation procedure data items from the frequency domain are transformed into the time domain. Forwards transformation procedures take place in a source coder of a transmitter, while reverse transformation procedures take place in a source decoder of a receiver. Source coder and source decoder can form parts of a digital video recorder. In mathematics a matrix multiplication corresponds to the transformation. In the case of discrete cosine transformation (DCT), transformation coefficients, i.e. the factors of a matrix, which simulate a cosine function column

by column or row by row, are used. The formation of transformation coefficients of a DCT is explained for example on page 20 of the dissertation authorised by the Electrical Engineering Department of the Wuppertal Polytechnic "A Contribution to Information Reduction in Television Video Signals with Transformation Coding and Adaptive Quantization" by Robert Sell. A portion of a television picture comprising 8*8 picture elements, referred to in the following as a block, possesses the 8*8 luminance- or chrominance values to be transformed of a 8*8 matrix. The luminance- or chrominance values are digitalized video signals. A luminance- or chrominance value occurs in parallel as binary signal D0-D7 on the data bus 1, the breadth of which is 8 bits.

In a forwards transformation procedure and a reverse transformation procedure in each case three matrices are multiplied with one another. In the case of two-dimensional transformation, in the forwards transformation procedure firstly the block is transformed in the horizontal direction monodimensionally and then is transformed in the vertical direction monodimensionally. The opposite is also possible, i.e. firstly the vertical monodimensional transformation and then the horizontal monodimensional transformation. In the two-dimensional reverse transformation procedure, firstly transformation is carried out monodimensionally in the vertical direction and then monodimensionally in the horizontal direction. Here again the opposite is possible. In the monodimensional horizontal transformation, the matrix to be transformed is multiplied eight times row by row with the eight coefficients of a row, while in the monodimensional vertical transformation it is multiplied eight times by the eight coefficients of a column. Sine the two-dimensional forwards transformation and reverse transformation procedures can in each case be split into two monodimensional forwards transformation and reverse

transformation procedures, the same transformers 3 -10 are suitable for the two monodimensional multiplications of the forwards transformation and reverse transformation procedures. The 8*8 block and the 2*(4*8) block after the first monodimensional forwards transformation and reverse transformation procedures must then merely be transposed, i.e. the addresses in the horizontal and vertical directions must be exchanged. The two multiplications of three 8*8 matrices - each of which thus comprises 8 rows and 8 columns - are carried out serially. The values of a matrix which are to be transformed pass through the circuit according to Figure 1 twice in series and are intermediately stored via the output 26 in a RAM (not shown) and then returned to the input 2.

A counter 15 receives a block start signal from an input 16 via a line 17 and a clock signal from an input 18 via a line 19. With a block size of 64 values, which corresponds to a matrix of 8 x 8 values, the block start signal is sent at the start of the block and following the processing of the 64 values. The block start signal resets the counter to zero. The counter 15 is clocked by the block signal on the line 19 and in the case of 64 values counts up to 64. The block signal is fed via a clock network 20 to the intermediate stores 14 and 24 which advantageously are formed by 74LS374 manufactured by Texas Instruments. With its three LSB outputs, the counter 15 controls a sign PROM 21 and the addressing of the multiplier 13 and of the transformers 3 - 10. The eight coefficients of a row and column are contained in the eight transformers 3-10. As multiplication is carried out eight times in series row by row and column by column and as each row and column possesses different coefficients, the current row address or column address is in each case indicated by the counter 15 with the aid of three LSBs on three lines with the signal SZ (current column or row). The sign PROM 21 is a store which

operates as multiplier. Mathematically, signs are multiplied by one another in this store. Advantageously, the sign PROM 21 is formed by a 74S288 or 74S287 of the National Semiconductor Company. The sign bit, which belongs to the chrominance- or luminance value present at the input 2, occurs at the input 22 of the line 23. Signs of values are calculated separately from the values, as in this way a data bus 1 with a breadth of 8 bits is available for the absolute value of the values. The sign bit and the 3 LSBs of the counter 15 serve as address in the store 21, under which 8 values corresponding to a sign are called up and fed to the intermediate store 24. The intermediate store 24 buffers these eight values and in each case emits one of these eight values to one of the transformers 3 - 10. Each of the transformers 3 - 10 possesses twelve data outputs D0 - 11 which are combined to form a data bus 25. The transformers 3 - 10 emit digital signals which as binary value correspond to a transformed value and numerically represent a value of 2^{12}, i.e. 4,096, and occur at the output 26. The circuit according to Figure 1 can be applied to a source coder in a transmitter and to a source decoder in a receiver. The difference resides in the store contents of the transformers 3 - 10 and of the multiplier 13.

Each of the transformers 3-10 advantageously is constructed in accordance with Figure 2. The store 30 advantageously is formed by a PROM 87S421 and operates as multiplier. The data items D0-D7 present at the input 2 are multiplied in the multiplier 30 by the transformation coefficients. The transformation coefficients are contained in the wiring of the PROMs. In the 8*8 forwards transformation procedure the absolute values of the DCT coefficients are mirror-symmetrical, i.e. in each row of the transformation matrix the first coefficient is identical to the eighth, the second to the seventh, the third to the sixth and the fourth to the fifth. In the 2*(4*8) forwards transformation procedure and

in the 8*8 and 2*(4*8) reverse transformation procedure this mirror symmetry ids not present. The signal on the line 12 indicates the type of transformation (AT) with the signal AT, i.e. whether a 8*8 or a 2*(4*8) transformation has been selected. In the store content of the PROMs 13 and 30 it is taken into account whether a forwards transformation procedure in a transmitter or a reverse transformation procedure in a receiver is provided. After the multiplication, eight LSBs of the result are forwarded to an intermediate store 31. The intermediate store 31 advantageously is formed by a 74LS374. The intermediate store buffers the result and feeds the result as digital signal via eight lines to the adder 32. Via the line 33 the MSB passes from the intermediate store 14 to an input of the adder 32. The adder 32 advantageously is formed by three modules 74F382 manufactured by the firm Fairchild. Via the line 34 the associated sign is fed via a one-wire line from the intermediate store 24 to the adder 32. At the start of a transformation the intermediate store 35 is set at zero and via the twelve data lines of the data bus 37 supplies the addend zero to the adder 32. The first sum is composed of the product of the two multipliers 13 and 30. After the first sum formation the sum is stored as result via the twelve data lines of the data bus 36 in the intermediate store 35. After the second multiplication the product is added to the first product from the intermediate store 35 and in the next step is stored again in the intermediate store 35. After eight additions the result is applied via the intermediate store 38 to the output 26. The eight values from the transformers 3-10 are applied in serial fashion via the data bus 25 to the output 26. The clock network 20 controls the intermediate stores 30, 35 and 38 via the block signal.

Claims

1. A circuit for the transformation or retransformation of in each case N input binary signals (EG, D0-D7) into in each case N output binary signals (AG) between the time domain and the frequency domain by means of a DCT (discrete cosine transformation), characterised by:

- N transformers (3-10) in each case supplied with the absolute values of N binary signals and containing storage means (30) with transformation coefficients stored therein without associated sign information, for the addressing of which the absolute values of the binary signals are used consecutively and which output binary signals multiplied by the respective transformation coefficient without associated sign information;
- sign multiplier means (21) in which the signs of the transformation coefficients are stored and which link the sign (VSB) of the respective binary signal with the sign of the transformation coefficient which is in each case to be addressed;
- combination means (32, 35) arranged in the transformers in which in each case N of the binary signals multiplied by the transformation coefficients are combined in an adder (32) in accordance with the sign (VZ) in each case determined in the sign multiplier means and as a result form one of N transformed output signals (D0-D11).

2. A circuit as claimed in Claim 1, characterised in that in an additional multiplier circuit (13) in each case the highest-value bit (MSB) for the binary signals linked with the transformation coefficients is formed and is supplied to the combination means (32, 35) via intermediate storage means (14).

3. A circuit as claimed in Claim 1 or 2, characterised in that the storage means (30) and optionally the additional

multiplier circuit (13) can be switched over via a further address line (12) between different types of transformation, in particular for a 8*8- and a 2*(4*8)- DCT.

4. A circuit as claimed in one or more of Claims 1 to 3, characterised in that for the transformation or retransformation of two-dimensional blocks of binary signals (D0-D7) the binary signals are transformed or retransformed firstly row by row and then column by column, or vice versa.