

"EXCLUSIVE LOGIC CIRCUIT"

This invention relates to exclusive logic circuits and, in particular, to exclusive OR circuits and exclusive NOR circuits for use in driving circuits for display devices, such as, for example,
5 liquid crystal display devices.

According to one aspect of the present invention there is provided an exclusive logic circuit for a driving circuit of a display device including a first inverter connected to a first input, a clocked second inverter connected to a second input and clocked by a
10 signal appearing at the first input so that a signal appearing at an output is selectively inverted with respect to the signal appearing at the first input depending upon the logic level of the latter signal, and a transmission gate whose control path is coupled to the first inverter and to the first input and whose signal path is connected
15 between the second input and the output, so that, in operation, the mission gate is controlled by the signal appearing at the first input for selectively passing the signal appearing at the second input to the output.

Preferably the first and second inverters are each composed
20 of complementary metal oxide semiconductors.

According to another aspect of the present invention there is provided a driving circuit comprising a plurality of exclusive logic circuits as recited above in combination with a display device.

The first inverter preferably is common to all the exclusive
25 logic circuits.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1(a) is a block diagram of a conventional exclusive OR circuit;

Figure 1(b) is a circuit diagram of the conventional exclusive OR circuit of Figure 1(a);

5 Figure 1(c) is a timing chart illustrating the operation of the conventional exclusive OR circuit of Figures 1(a) and 1(b);

Figure 2(a) is a block diagram of one embodiment of an exclusive OR circuit according to the present invention;

10 Figure 2(b) is a circuit diagram of the exclusive OR circuit of Figure 2(a);

Figure 2(c) is a timing chart illustrating the operation of the exclusive OR circuit of Figures 2(a) and 2(b);

15 Figure 3(a) is a schematic circuit diagram of a static driving circuit including exclusive OR circuits as illustrated in Figures 2(a) and 2(b) for a liquid crystal display device;

Figure 3(b) is a timing chart illustrating the operation of the static driving circuit of Figure 3(a);

Figure 4(a) is a block diagram of one embodiment of an exclusive NOR circuit according to the present invention;

20 Figure 4(b) is a circuit diagram of the exclusive NOR circuit of Figure 4(a); and

Figure 4(c) is a timing chart illustrating the operation of the exclusive NOR circuit of Figures 4(a) and 4(b).

25 Referring first to Figures 1(a) and 1(b) a conventional exclusive OR circuit comprises two inverters 11, 13 and two clocked

inverters 12, 14. An output signal appearing at a terminal 3 is obtained from input signals applied to terminals 1, 2. As will be appreciated from Figure 1(b), when the input signal applied to the terminal 2 is low level, the clocked inverter 14 inverts the output signal from the inverter 13 and an inverted pulse appears at the terminal 3. When the signal applied to the terminal 2 is high level, the clocked inverter 12 operates to invert the input signal applied to the terminal 1 and an inverted pulse appears at the terminal 3. Figure 1(c) is a timing chart showing the state of the input signals applied to the input terminals 1, 2 and the output signal appearing at the terminal 3 of the conventional exclusive OR circuit shown in Figures 1(a) and 1(b).

The inverters 11, 13 consist of two field effect transistors and the clocked inverters 12, 14 each consist of four field effect transistors. Accordingly, the conventional exclusive OR circuit of Figures 1(a) and 1(b) has a total of twelve transistors.

Generally speaking, in a multiplex driving circuit for a display device one, two or three segments of the display device are driven by a single driving circuit. Thus it is necessary to use a considerable number of exclusive OR circuits connected in parallel when the display device has a relatively large number of segments to be driven. Therefore, the conventional exclusive OR circuit shown in Figures 1(a) and 1(b) has the disadvantage that the space occupied by the multiplex driving circuit is a relatively large proportion of the space available on an integrated circuit.

Referring now to Figures 2(a) and 2(b) there is illustrated one embodiment of an exclusive OR circuit according to the present invention. Like parts in Figures 1(a), 1(b), 2(a) and 2(b) have been designated by the same reference numerals.

5 The difference between the exclusive OR circuit shown in Figures 2(a) and 2(b) and that shown in Figures 1(a) and 1(b) is that a transmission gate 15 takes the place of the inverter 13. The transmission gate 15 has a control path coupled via the inverter 11 to the terminal 1 and a signal path connected between the terminal 2 and
10 the terminal 3. When the input signal applied to the terminal 2 is a positive going pulse, the gate of the clocked inverter 12 is open, thus resulting in the input signal applied to the terminal 1 being inverted and appearing at the terminal 3. In this case, the transmission gate 15 is closed presenting a high impedance at the output side thereof.
15 On the other hand, when the input signal applied to the terminal 2 is a negative going pulse, the gate of the clocked inverter 12 is closed and a high impedance is presented at the output side thereof, and the transmission gate 15 is opened. As the result, the input signal applied to the terminal 1 appears at the terminal 3. Figure 2(c) is a timing
20 chart showing the state of the input signals applied to the terminals 1, 2 and the output signal appearing at the terminal 3 of the exclusive OR circuit shown in Figures 2(a) and 2(b).

 The exclusive OR circuit shown in Figures 2(a) and 2(b) requires only a total of 8 field effect transistors, the transmission gate 15
25 consisting of two such transistors. Thus the exclusive OR circuit of Figures 2(a) and 2(b) performs the same logic function

as the conventional exclusive OR circuit of Figures 1(a) and 1(b) but using four less transistors and consequently a multiplex driving circuit using exclusive OR circuits as illustrated in Figures 2(a) and 2(b) occupies less space on an integrated circuit compared to the space occupied by the conventional exclusive OR circuit of Figures 1(a) and 1(b).

Moreover in a static driving circuit for a liquid crystal display device comprising exclusive OR circuits as illustrated in Figures 2(a) and 2(b), a portion indicated by reference numeral 101 may be common to all segments of the display device because a standard clock signal is applied to all segments. It is thus only necessary to provide a portion indicated by reference numeral 102 for each one, two or three segments connecting the plurality of portions 102 in parallel. Figure 3(a) illustrates such a static driving circuit for a liquid crystal display device. In Figure 3(a) COM indicates a common electrode of the liquid crystal display device to which a signal ϕ is applied. a, b, c, d ... g represent segment electrodes of the liquid crystal display device for displaying digits using seven segments. Signals a_{DEC} , b_{DEC} g_{DEC} from a decoder circuit (not shown) are applied in order to control energisation of each segment. The segment ϕ is used for driving the liquid crystal display device with an alternating voltage, and usually a signal having a frequency of 32 Hz is used. The signal ϕ is fed to the portion 101 common to all the exclusive OR circuits, while the signals a_{DEC} , b_{DEC} g_{DEC} are applied to the respective

portions 102 of the exclusive OR circuits.

Figures 3(b) is a timing chart of the signals applied to the segment a shown in Figure 3(a), wherein V is the voltage applied to the liquid crystal display device. When the signal a_{DEC} is low level the liquid crystal display device is not energised and uses no display but when the signal a_{DEC} is high level the liquid crystal display device is energised and produces a display. In Figure 3(a) seven exclusive OR circuits are necessary for driving the segments of one digit. However, the portion 101 is common to all exclusive OR circuits. Therefore the driving circuit can be simplified compared to a driving circuit using the conventional exclusive OR circuits of Figures 1(a) and 1(b).

It will be appreciated that exclusive OR circuits according to the present invention can be applied not only to static driving circuits as described in relation to Figure 3(a) but also to multiplex driving circuits with a duty ratio of 1/3 or 1/3 etc.

The present invention has been described above in relation to exclusive OR circuits for driving circuits of display devices, but it is possible to use exclusive NOR circuits instead, when the signal appearing at the terminal 3 is obtained as negative logic or the input signal applied to the terminal 1 is negative logic. Figures 4(a) and 4(b) illustrate an exclusive NOR circuit according to the present invention. The exclusive NOR circuit shown in Figures 4(a) and 4(b) is similar to the exclusive OR circuit of Figure 2(a) and so will not be described in detail, the difference

being that the input signals applied to the terminal 2 are opposite to one another. The exclusive NOR circuit of Figures 4(a) and 4(b) has the same advantages as the exclusive OR circuit of Figures 2(a) and 2(b) as already discussed above. Figure 4(c) is a timing chart illustrating the state of the input signals applied to the terminals 1, 2 and the output signal appearing at the terminal 3 of the exclusive NOR circuit shown in Figures 4(a) and 4(b).

An exclusive logic circuit according to the present invention may employ complementary metal oxide semiconductors for the field effect transistors thereby permitting it to be integrated.



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CLAIMS

1. An exclusive logic circuit for a driving circuit of a display device including a first inverter connected to a first input, a clocked second inverter connected to a second input and clocked by a signal appearing at the first input so that a signal appearing at
5 an output is selectively inverted with respect to the signal appearing at the first input depending upon the logic level of the latter signal, and a transmission gate whose control path is coupled to the first inverter and to the first input and whose signal path is connected between the second input and the output, so that, in operation, the
10 transmission gate is controlled by the signal appearing at the first input for selectively passing the signal appearing at the second input to the output.
2. An exclusive logic circuit as claimed in claim 1 in which the first and second inverters are each composed of complementary metal
15 oxide semiconductors.
3. An exclusive logic circuit as claimed in claim 1 or 2 constructed as an exclusive OR circuit.
4. An exclusive logic circuit as claimed in claim 1 or 2 constructed as an exclusive NOR circuit.
- 20 5. An exclusive logic circuit substantially as herein described with reference to and as shown in Figures 2(a) and 2(b), or Figures 4(a) and 4(b) of the accompanying drawings.



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6. A driving circuit including a plurality of exclusive logic circuits as claimed in any preceding claim in combination with a display device.
7. A combination as claimed in claim 6 in which the first
5 inverter is common to all the exclusive logic circuits.
8. A combination as claimed in claim 6 or 7 in which the display device is a liquid crystal display device.
9. A combination as claimed in claim 6 and substantially as herein described with reference to and as shown in Figure 3(a) of
10 the accompanying drawings.

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