What is claimed is:

1. A method of controlling on-die termination (ODT) in a multi-rank memory system including a plurality of memory ranks, the method comprising:

enabling ODT circuits of the plurality of memory ranks into an initial state when the multi-rank memory system is powered on;

enabling the ODT circuits of a write target memory rank and non-target memory ranks among the plurality of memory ranks during a write operation; and

disabling the ODT circuit of a read target memory rank among the plurality of memory ranks while enabling the ODT circuits of non-target memory ranks among the plurality of memory ranks during a read operation;

wherein each of the ODT circuits of the plurality of memory ranks has a first resistance value in the initial state; and

wherein enabling the ODT circuits during the write operation further comprises: changing a resistance value of the ODT circuit of the write target memory rank from the first resistance value to a second resistance value different from the first resistance value during the write operation.

2. The method of claim 1, wherein the second resistance value is greater than the first resistance value.

3. The method of claim 1, wherein enabling the ODT circuit of non-target memory ranks during the read operation comprises:

maintaining the ODT circuits of the non-target memory ranks in the initial state to have the first resistance value during the read operation.

4. The method of claim 1, wherein the ODT circuits of the plurality of memory ranks are configured to terminate data input-output pins of the plurality of memory ranks.

5. The method of claim 4, wherein the ODT circuits of the plurality of memory ranks maintain the initial state even while a data input-output operation through the data input-output pins is not performed.

6. The method of claim 1, wherein the ODT circuits of the non-target memory ranks among the plurality of memory ranks except the write target memory rank or the read target memory rank have a constant resistance value regardless of a memory access command from a memory controller.

7. The method of claim 6, wherein the constant resistance value of the non-target memory ranks is determined based on a value stored in a mode register of the multi-rank memory system.

8. The method of claim 1, wherein the write target memory rank or the read target memory rank is converted from a power-down mode to a normal operation mode to perform the write operation or the read operation, and the non-target memory ranks among the plurality of memory ranks except the write target memory rank or the read target memory rank maintain the power-down mode during the write operation or the read operation.

9. A system comprising:

a plurality of memory ranks including a plurality of memory devices; and

a memory controller configured to control the plurality of memory ranks,

wherein on die termination (ODT) circuits of the plurality of memory ranks are enabled into an initial state when the system is powered on, the ODT circuits of the plurality of memory ranks are enabled during a write operation with respect to a write target memory rank and non-target memory ranks among the plurality of memory ranks, and the ODT circuit of a read target memory rank among the plurality of memory ranks is disabled while the ODT circuits of non-target memory ranks among the plurality of memory ranks are enabled during a read operation;

wherein the ODT circuits of the plurality of memory ranks have a first resistance value in the initial state; and

wherein, when the ODT circuits are enabled during the write operation, a resistance value of the ODT circuit of the write target memory rank is changed from a first resistance value to a second resistance value different from the first resistance value during the write operation.

10. The system of claim 9, wherein the ODT circuits of the non-target memory ranks among the plurality of memory ranks except the write target memory rank or the read target memory rank have a constant resistance value regardless of a memory access command from the memory controller.

11. The system of claim 9 or claim 10, wherein the second resistance value is greater than the first resistance value.

12. A system comprising:

a first memory rank comprising a plurality of first memory devices connected to a

first on die termination (ODT) circuit; and

a second memory rank comprising a plurality of second memory devices connected to a second ODT circuit,

wherein the first and second ODT circuits are enabled during a write operation of the first memory rank, and the first ODT circuit is disabled and the second ODT circuit is enabled during a read operation of the first memory rank;

wherein each of the first and second ODT circuits has a first resistance value in the initial state; and

wherein when the first ODT circuit is enabled during the write operation, the resistance value of the first ODT circuit is changed from a first resistance value to a second resistance value different from the first resistance value during the write operation.

13. The system of claim 12, wherein each enabled ODT circuit provides termination impedance to a transmission line coupled to a data input-output pin of the corresponding memory rank.

14. The system of claim 13, wherein the first ODT circuit is disabled during the read operation only while read data corresponding to the read operation is output from the data input-output pin.

15. The system of any of claims 12 to 14, wherein the second resistance value is greater than the first resistance value.