

1/10

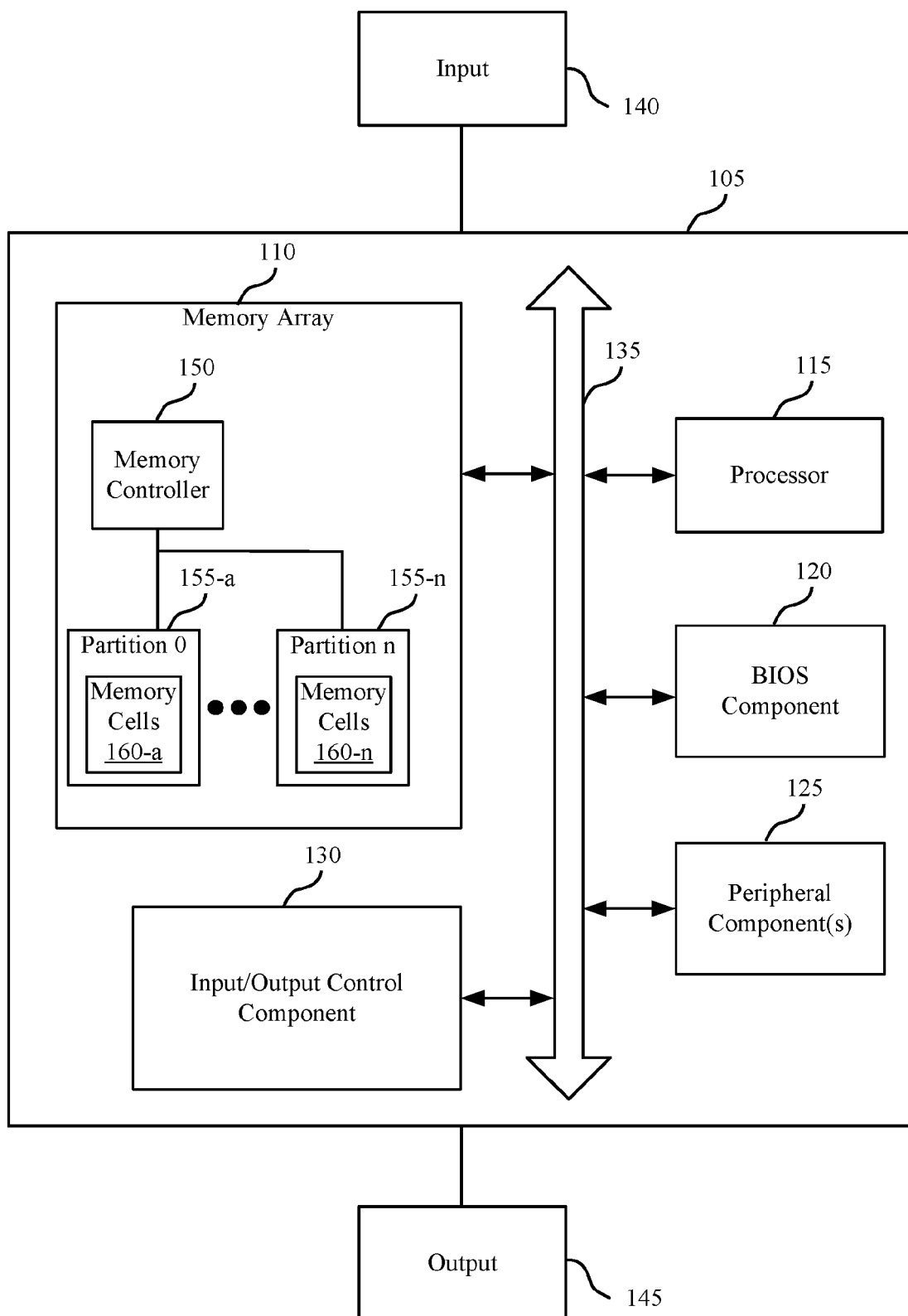


FIG. 1

100

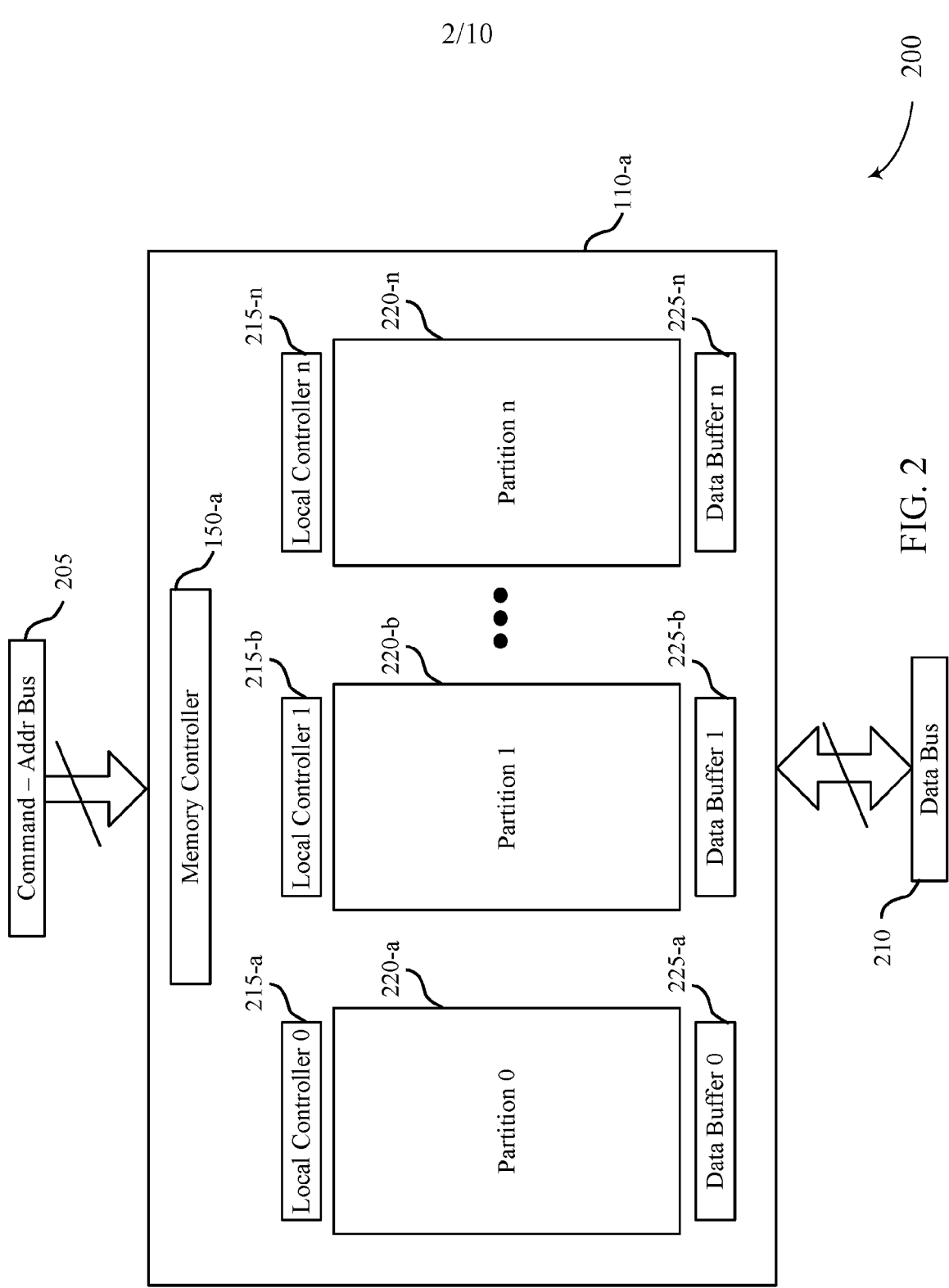


FIG. 2



Pin	Command Address Cycle							
	0	1	2	3	4	5	6	7
CA4	CMD3	RFU	RFU	MA	MA	MA	MA	MA
CA3	CMD2	PA3	RFU	MA	MA	MA	MA	MA
CA2	CMD1	PA2	RFU	MA	MA	MA	MA	MA
CA1	CMD0	PA1	RFU	MA	MA	MA	MA	MA
CA0	RFU	PA0	MA	MA	MA	MA	MA	MA

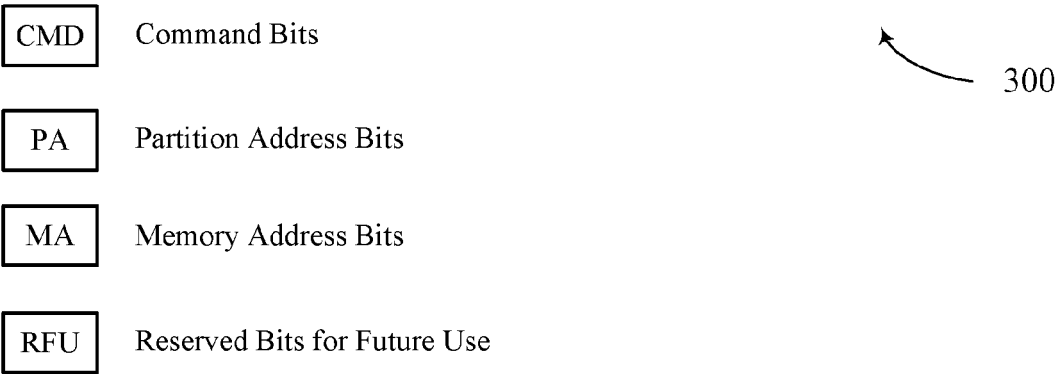


FIG. 3



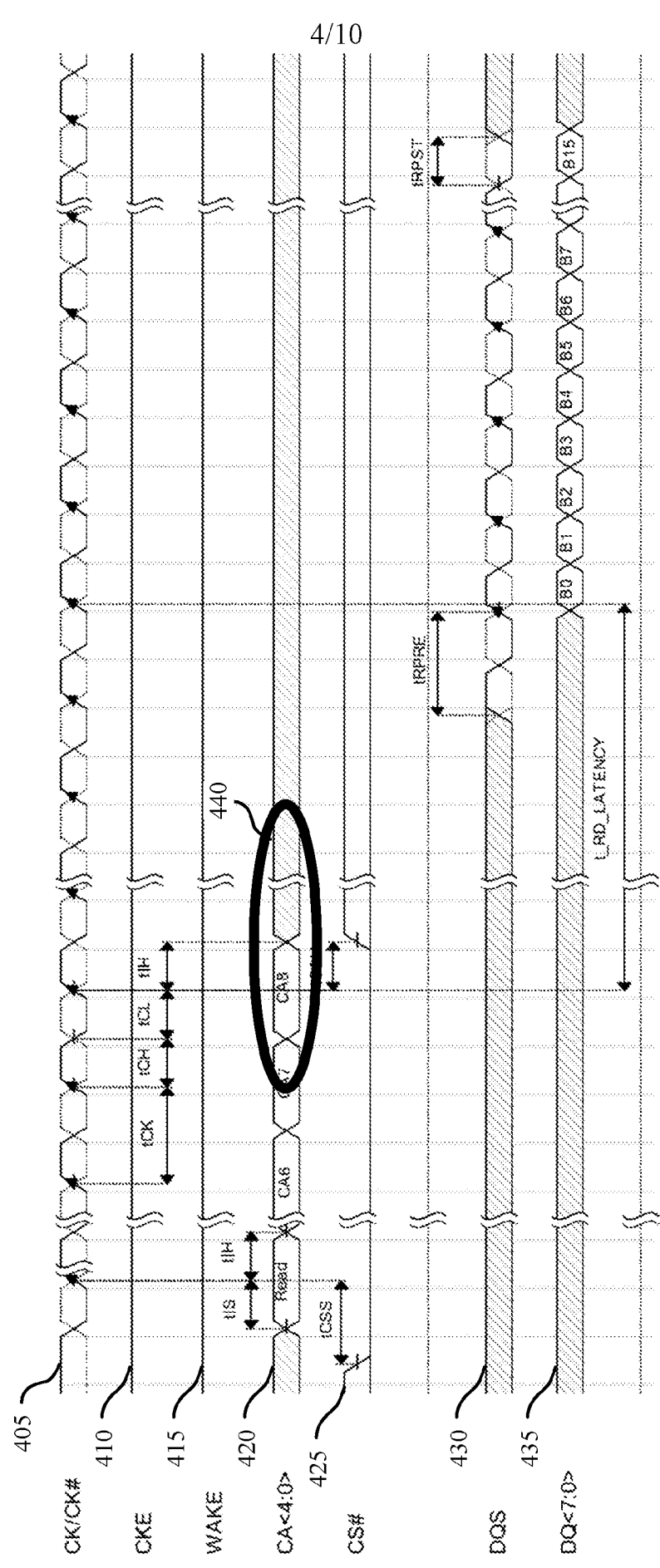


FIG. 4

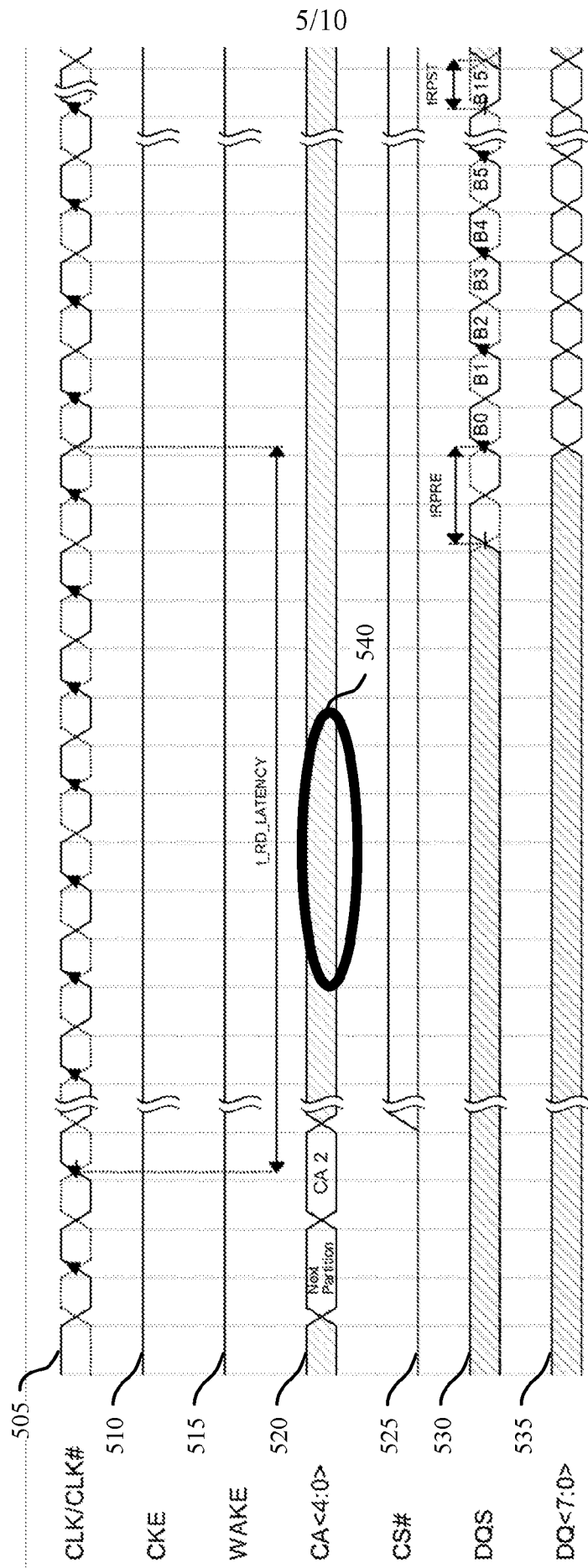


FIG. 5

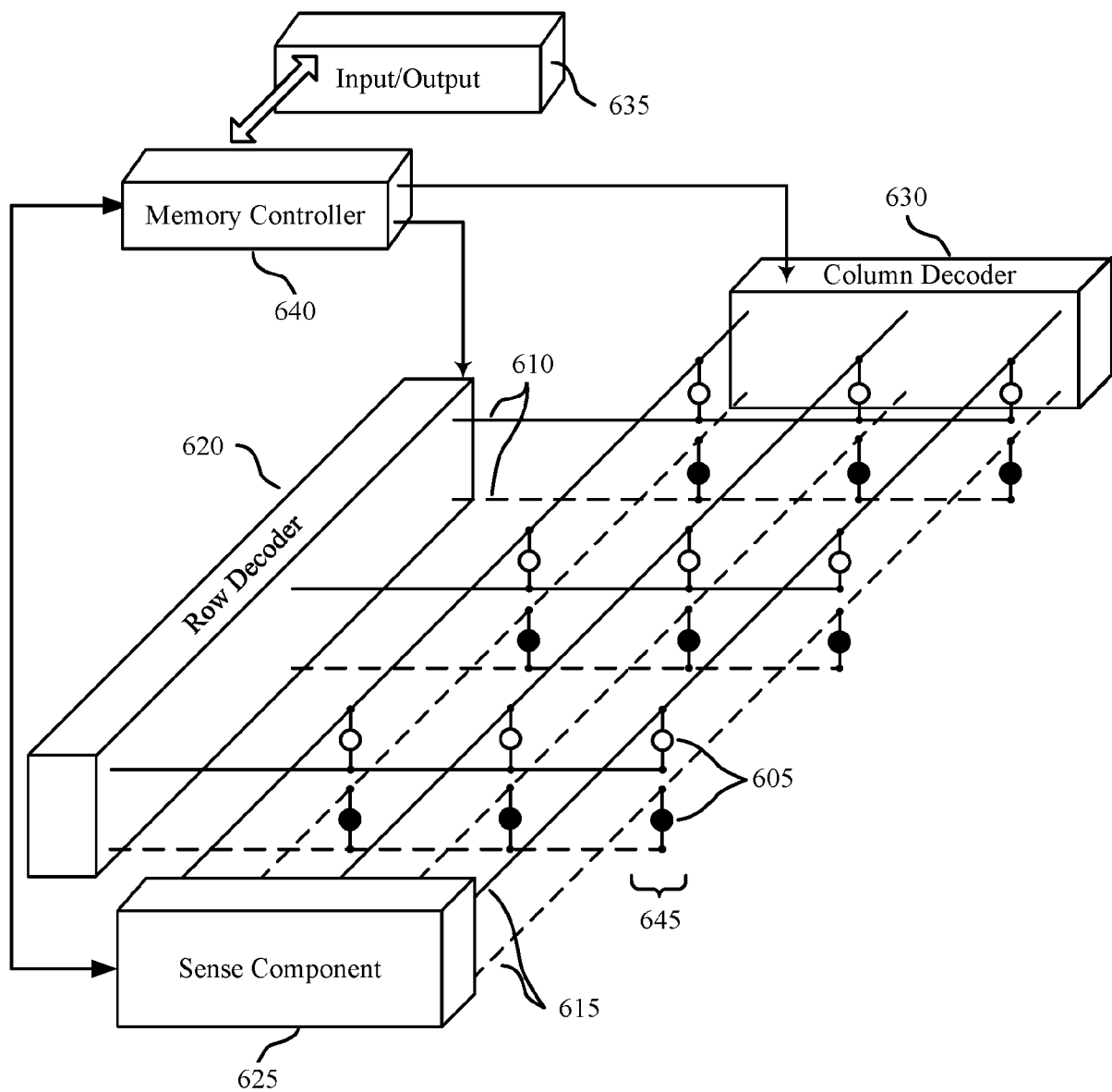


FIG. 6

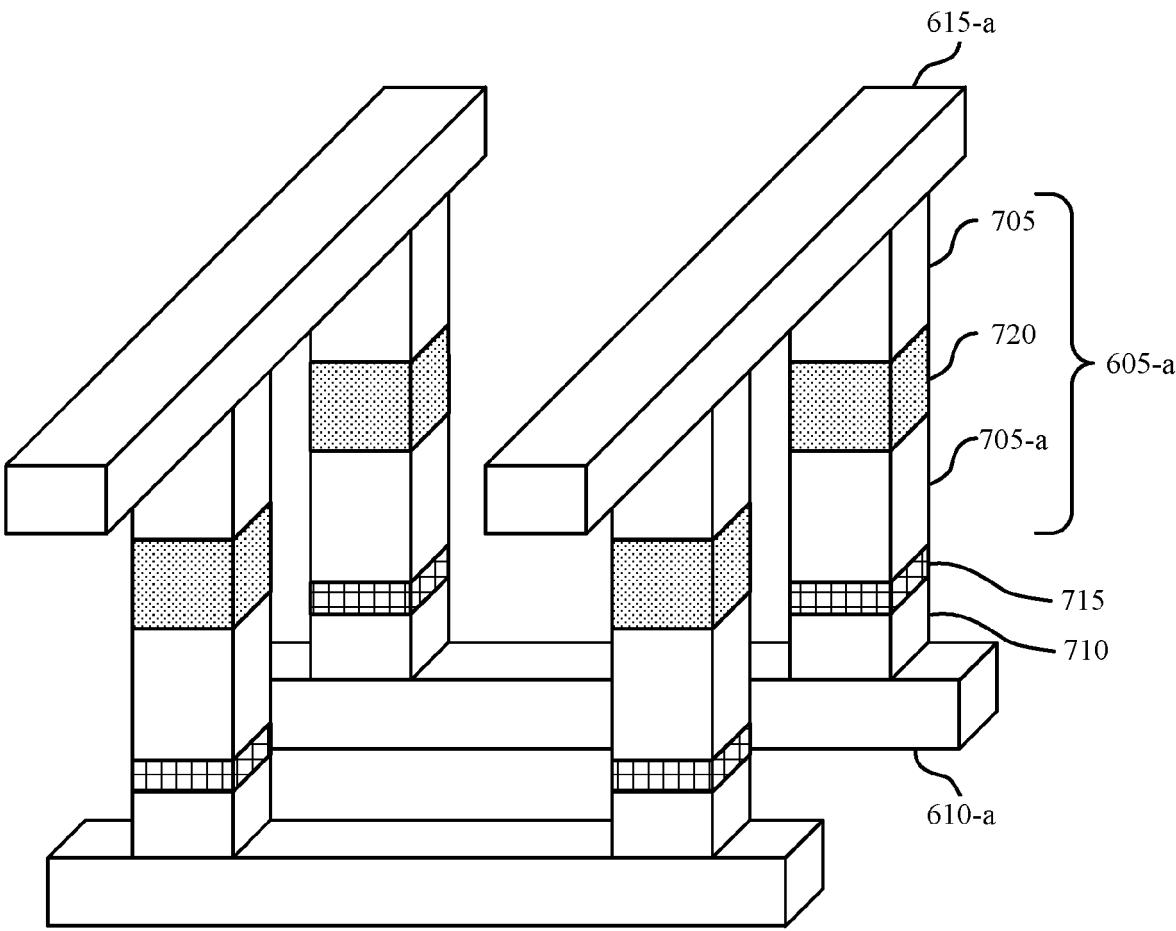


FIG. 7

700

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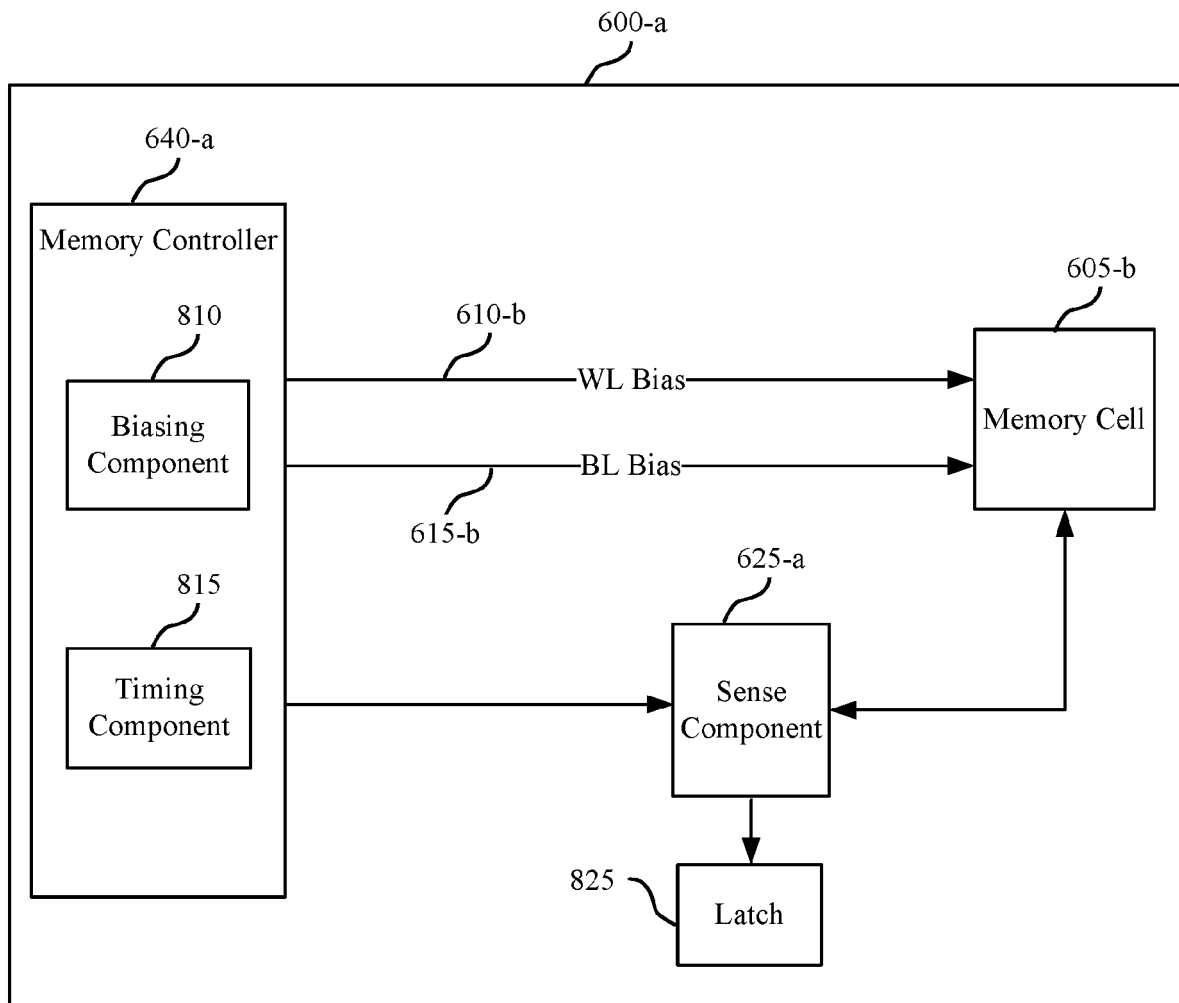


FIG. 8

800

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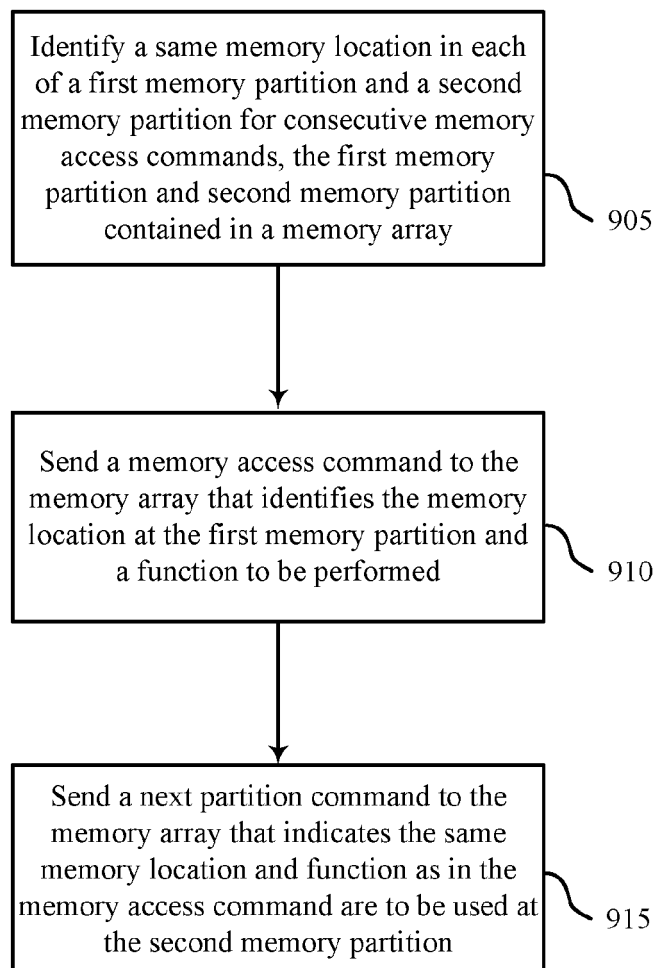


FIG. 9

900

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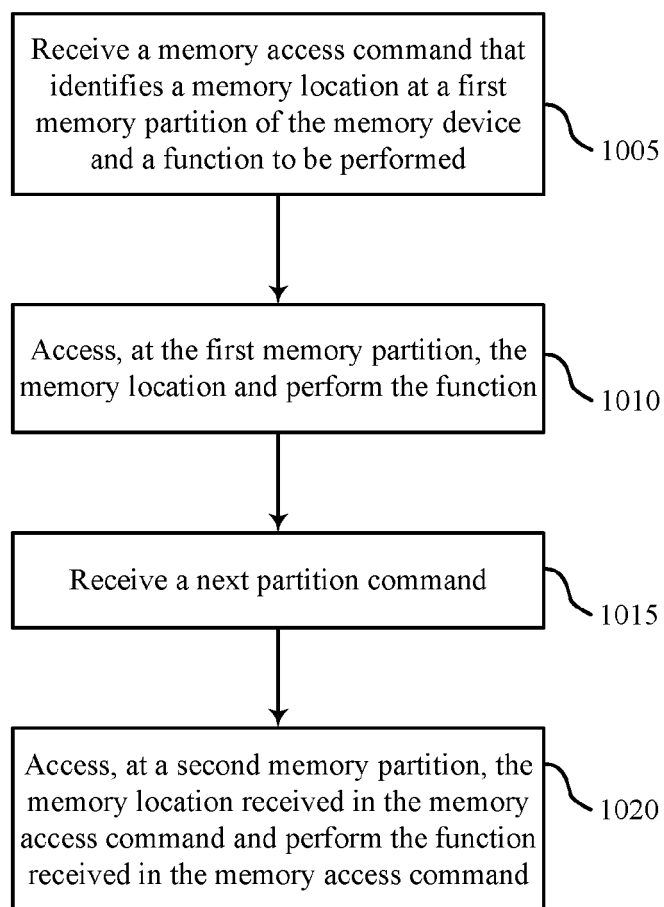


FIG. 10

1000