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(54) Title: SCHEDULING FOR MEMORY

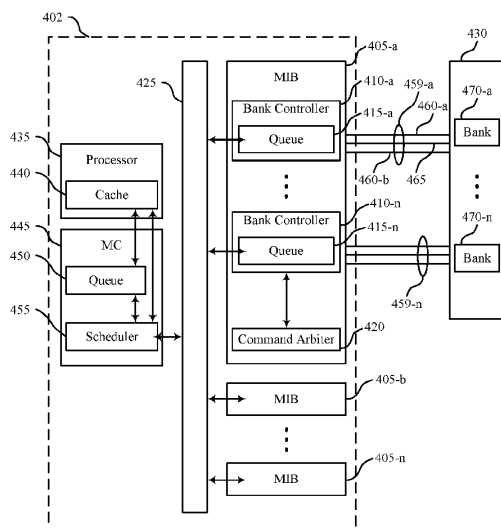


FIG. 4

(57) Abstract: Methods, systems, and devices for schedule memory are described. Specifically, techniques are described for a memory interface between a host system and memory (e.g., a tightly coupled memory). For example, a memory interface block (MIB) between the host system and the memory system may schedule access operations performed by the memory system, schedule and perform error control operations, schedule and perform media management operations, as well as schedule and perform other operations. The use of such a MIB may enable the improvement of the memory system by reducing latency and increasing efficiency of memory accesses, while reducing impacts on the architecture and design of the host system.

[Continued on next page]

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
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