

ABSTRACT

The bus width of the data bus 18 among blocks for transferring data among respective blocks such as the memory control block 15, the error correction block 16, and the host I/F block 17 is 32-bit width, and the bus width of the memory data bus 19 for transferring data between the buffer memory 12 and the memory control block 15 is 64-bit width, whereby an access to the buffer memory 12 is performed by the unit of 64 bits, while respective block processings are performed by the unit of 32 bits out of the 64 bits. Therefore, 32-bit data transferred through the data bus 18 among blocks are always valid data, whereby the access rate from respective blocks in the system to the buffer memory 12 can be increased.