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ADVANCED INTER-LEVEL DIELECTRIC (ILD) LAYER FOR SILICON ULTRA- LARGE SCALE INTEGRATED (ULSI) CIRCUITS

by

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to dielectric layers within integrated circuits. More particularly, the present invention relates to spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions employed in integrated circuits such as silicon ultra-large scale integrated (ULSI) circuits.

2. Description of the Related Art

Integrated circuits are formed upon semiconductor substrates within and upon whose surfaces are formed resistors, transistors, diodes and other electrical circuit elements. The electrical circuit elements are connected internally and externally to the semiconductor substrate upon which they are formed through patterned conductor layers which are separated by dielectric layers.

In the method for forming dielectric layers such as pre-metal dielectric (PMD) layers and, more particularly, inter-level dielectric (ILD) layers within advanced integrated circuits

such as ultra-large scale integrated (ULSI) circuits, it is common in the art to employ a sandwich composite planarizing dielectric layer construction formed from a spin applied spin-on-glass (SOG) planarizing dielectric layer which is sandwiched between a lower lying conformal dielectric layer and an upper lying conformal dielectric layer. Typically, although not exclusively, the lower lying conformal dielectric layer and the upper lying conformal dielectric layer are formed from a silicon oxide dielectric material. Typically, although not exclusively, the silicon oxide dielectric material from which is formed the lower lying conformal dielectric layer and the upper lying conformal dielectric layer is formed through a chemical vapor deposition (CVD) method such as, but not limited to, a plasma enhanced chemical vapor deposition (PECVD) method. In a conventional method for forming such a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction, it is common after forming the spin-on-glass (SOG) planarizing dielectric layer upon the lower lying conformal dielectric layer to further planarize through a reactive ion etch (RIE) etchback method the spin-on-glass (SOG) planarizing dielectric layer prior to forming upon the spin-on-glass (SOG) planarizing dielectric layer the upper lying conformal dielectric layer. The reactive ion etch (RIE) etchback processing of the spin-on-glass (SOG) planarizing dielectric layer is typically preferably undertaken until the uppermost portions of the lower lying conformal dielectric layer are reached and partially etched. There is then formed upon the reactive ion etch (RIE) etchback processed spin-on-glass (SOG) planarizing dielectric layer and the partially etched lower lying conformal dielectric layer the upper lying conformal dielectric layer. The spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction so formed is then typically completely planarized through a chemical-mechanical polish (CMP) planarizing of the upper lying conformal dielectric layer.

By employing such a conventional method where a reactive ion etch (RIE) etchback processing of the spin-on-glass (SOG) planarizing dielectric layer is undertaken until the

uppermost portions of the lower lying conformal dielectric layer are reached and partially etched, there is formed a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction through which there may be formed a via sequentially through the upper lying conformal dielectric layer and the lower lying conformal dielectric layer to a patterned layer, such as a patterned conductor layer, formed beneath the lower lying conformal dielectric layer without passing through the spin-on-glass (SOG) planarizing dielectric layer. It is desirable within advanced integrated circuits to avoid forming vias through spin-on-glass (SOG) planarizing dielectric layers since vias formed through spin-on-glass (SOG) planarizing dielectric layers are often susceptible to moisture sorption and desorption which may yield high resistance connection and interconnection elements formed into those vias formed through those spin-on-glass (SOG) planarizing dielectric layers.

While the conventional method for forming a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction where a via may be formed through only the upper lying conformal dielectric layer and the lower lying conformal dielectric layer within the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction has become common in the art, the method approaches an inherent limitation as the width (ie: pitch) of an aperture formed within a patterned layer upon which is typically formed the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction decreases and the aspect ratio of the aperture within the patterned layer increases. The significance of the width and aspect ratio of the aperture within the patterned layer upon which is formed the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction is illustrated by reference to Fig. 1.

Shown in Fig. 1 is a substrate 10 upon which is formed a pair of patterned layers 12a and 12b. The substrate 10 and the pair of patterned layers 12a and 12b have formed

thereupon a lower lying conformal dielectric layer 14 of a spin-on-glass sandwich composite planarizing dielectric layer construction (the spin-on-glass (SOG) planarizing dielectric layer and the upper lying conformal dielectric layer of the spin-on-glass sandwich composite planarizing dielectric layer construction are not shown). Under conditions where the width $W1$ of the aperture between the patterned layers 12a and 12b decreases while the aspect ratio $H1/W1$ of the aperture between the patterned layers 12a and 12b increases it becomes increasingly prevalent that a void will form within the width $W2$ of the aperture within the lower lying conformal dielectric layer 14 due to bridging of portions of the lower lying conformal dielectric layer 14 from the opposing sidewalls of the patterned conductor layers 12a and 12b. The formation of a void within the width $W2$ of the aperture within the lower lying conformal dielectric layer 14 is undesirable since such a void will preclude subsequent filling of the width $W2$ of the aperture within the lower lying conformal dielectric layer 14 with the subsequently formed spin-on-glass (SOG) planarizing dielectric layer, thus compromising the dielectric characteristics of the integrated circuit into which is formed the patterned layers 12a and 12b.

From a practical perspective, within ultra-large scale integrated (ULSI) circuits where the patterned layers 12a and 12b are typically, although not exclusively, patterned conductor layers and the width $W1$ of the aperture between the patterned layers 12a and 12b is from about 2000 to about 8000 angstroms while the aspect ratio $H/W1$ of the aperture between the patterned layers 12a and 12b is greater than about 2, the lower lying conformal dielectric layer 14 may typically have a thickness T of up to about 3500 angstroms before void formation within the width $W2$ of the aperture within the lower lying conformal dielectric layer 14 becomes prevalent.

Unfortunately, at a thickness T of less than about 2000 angstroms the lower lying

conformal dielectric layer 14 will often be of insufficient thickness to reliably assure that the conventional reactive ion etch (RIE) etchback processing of the spin-on-glass (SOG) planarizing dielectric layer subsequently formed upon the lower lying conformal dielectric layer 14 will reproducibly terminate with only a partial reactive ion etch (RIE) etchback etching of the uppermost portions of the lower lying conformal dielectric layer 14. A complete etching of the uppermost portions of the lower lying conformal dielectric layer 14 through reactive ion etch (RIE) etchback processing of a spin-on-glass (SOG) planarizing dielectric layer formed upon the lower lying conformal dielectric layer 14, as illustrated in Fig. 1, will often damage the patterned layers 12a and 12b and lead to functionality or reliability problems within the integrated circuit within which is formed the patterned layers 12a and 12b, particularly when the patterned layers 12a and 12b are patterned conductor layers.

It is therefore desirable in the art to provide a method through which there may be formed within integrated circuits, such as advanced ultra-large scale integrated (ULSI) circuits, spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions in a fashion such that: (1) patterned layers formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions are not damaged when forming the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions; and (2) apertures or vias may be formed within or through the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions without passing through the spin-on-glass (SOG) planarizing dielectric layers of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions. It is towards these goals that the present invention is generally directed.

Polishing methods and materials through which adjoining layers formed of different materials within integrated circuits may be polished at different rates to produce structures of

desirable dimensions within those integrated circuits are known in the art. For example, Doan et al. in U.S. Patent No. 5,395,801 disclose a polishing method employing either a single polishing slurry or two different polishing slurries having different polishing rates for two insulator layers within an integrated circuit, thus forming an insulator layer structure with preferentially etched characteristics. In addition, B. Tredinnick et al. in "New CMP Polishes for SOG Planarization," Planar 96 - The Dielectrics Conference, January 29, 1996, disclose the use of novel cerium oxide slurries for chemical mechanical polish (CMP) planarizing of various spin-on-glass (SOG) planarizing dielectric layers formed in the presence of silicon oxide dielectric layers formed through a thermal oxidation method employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source material.

Desirable in the art are methods and materials through which spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions may be formed within advanced integrated circuits, such as ultra-large scale integrated (ULSI) circuits, in a fashion such that: (1) patterned layers formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions are not damaged when forming the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions; and (2) apertures or vias may be formed within or through the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions without passing through the spin-on-glass (SOG) planarizing dielectric layers of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions. Particularly desirable are methods and materials which achieve the foregoing two goals while providing a readily manufacturable method of limited process complexity. It is towards these goals that the present invention is specifically directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method through which a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction may be formed within an integrated circuit, where a patterned layer formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction is not damaged when forming the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction.

A second object of the present invention is to provide a method through which a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction may be formed within an integrated circuit, where apertures or vias may be formed within or through the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction without passing through the spin-on-glass (SOG) planarizing dielectric layer of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction.

A third object of the present invention is to provide a method in accord with the first object of the present invention or the second object of the present invention, where the method is readily manufacturable and of limited process complexity.

In accord with the objects of the present invention, there is provided by the present invention a method for forming for use within an integrated circuit, such as an advanced ultra-large scale integrated (ULSI) circuit, a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. To form the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction of the present invention, there is first provided a substrate. There is then formed upon the substrate a patterned layer which has a minimum of one aperture formed at

least partially through the patterned layer. The patterned layer has an upper portion of the patterned layer further from the substrate and the patterned layer also has a lower portion of the patterned layer closer to the substrate. There is then formed upon the patterned layer a first conformal dielectric layer. The first conformal dielectric layer has an upper portion of the first conformal dielectric layer formed upon the upper portion of the patterned layer and a lower portion of the first conformal dielectric layer formed closer to the substrate. There is then formed upon the first conformal dielectric layer a spin-on-glass (SOG) planarizing dielectric layer. The spin-on-glass (SOG) planarizing dielectric layer is formed over both the upper portion of the first conformal dielectric layer and the lower portion of the first conformal dielectric layer. The spin-on-glass (SOG) planarizing dielectric layer has a thickness upon the lower portion of the first conformal dielectric layer greater than the depth of the aperture within the patterned layer. There is then planarized through a chemical mechanical polish (CMP) planarizing method the spin-on-glass (SOG) planarizing dielectric layer and the upper portion of the first conformal dielectric layer to form a planarized spin-on-glass (SOG) planarizing dielectric layer substantially coplanar with a partially planarized first conformal dielectric layer. The planarizing is undertaken without exposing the upper portion of the patterned layer. Finally, there is formed upon the planarized spin-on-glass (SOG) planarizing dielectric layer and partially planarized first conformal dielectric layer a second conformal dielectric layer.

The present invention provides a method through which a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction may be formed within an integrated circuit, where a patterned layer formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction is not damaged when forming the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. Through the method of the present invention, the spin-on-glass (SOG) planarizing dielectric layer and the first conformal dielectric

layer within the spin-on-glass sandwich composite planarizing dielectric layer construction are planarized through a chemical-mechanical polish (CMP) planarizing method to form a planarized spin-on-glass (SOG) planarizing dielectric layer and a partially planarized first conformal dielectric layer without exposing the patterned layer. Thus, since the patterned layer is not reached through the chemical-mechanical polish (CMP) planarizing method of the present invention, the present invention provides a method through which a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction may be formed within an integrated circuit, where a patterned layer formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction is not damaged when forming the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction

The present invention provides a method through which a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction may be formed within an integrated circuit, where apertures or vias may be formed within or through the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction without passing through the spin-on-glass (SOG) planarizing dielectric layer of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. Through the method of the present invention, a second conformal dielectric layer is formed upon a planarized spin-on-glass (SOG) planarizing dielectric layer and a substantially coplanar partially planarized first conformal dielectric layer when forming a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. Through forming an aperture or via within or through the portion of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction where the second conformal dielectric layer is formed upon the partially planarized first conformal dielectric layer, there may be formed an aperture or via within or through the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction without passing through the spin-on-glass (SOG) planarizing

dielectric layer of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction.

The method of the present invention is readily manufacturable and of limited process complexity. The method of the present invention provides for a novel ordering of integrated circuit fabrication methods which are otherwise known in the art of integrated circuit fabrication. Thus, the method of the present invention is readily manufacturable. In comparison with methods as are conventional in the art of forming spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions, the method of the present invention: (1) eliminates a reactive ion etch (RIE) etchback processing of the spin-on-glass (SOG) planarizing dielectric layer prior to forming the second conformal dielectric layer within the spin-on-glass (SOG) sandwich planarizing dielectric layer construction; and (2) replaces a chemical-mechanical polish (CMP) planarizing of the second conformal dielectric layer within the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction with a chemical-mechanical polish (CMP) planarizing of the spin-on-glass (SOG) planarizing dielectric layer and the first conformal dielectric layer within the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. Thus, the method of the present invention has limited process complexity.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

Fig. 1 shows a schematic cross-sectional diagram illustrating the inherent limitation of an aperture width and an aperture aspect ratio within a patterned layer in forming upon the patterned layer a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction through a method conventional in the art.

Fig. 2 to Fig. 6 show a series of schematic cross-sectional diagrams illustrating the results of progressive process stages in forming within an integrated circuit a pair of spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions as inter-level dielectric (ILD) layers within the integrated circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides a method for forming within an integrated circuit, such as an ultra-large scale integrated (ULSI) circuit, a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction in a fashion such that: (1) a patterned layer formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions is not damaged when forming the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction; and (2) an aperture or via may be formed within or through the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction without passing through the spin-on-glass (SOG) planarizing dielectric layer of the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction. In addition, the method through which the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction of the present invention is formed is readily manufacturable and of limited process complexity.

The method of the present invention achieves the foregoing goals through planarizing through a chemical-mechanical polish (CMP) planarizing method a spin-on-glass (SOG) planarizing dielectric layer and a first conformal dielectric layer within the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction to form a planarized spin-on-glass (SOG) planarizing dielectric layer substantially coplanar with a partially planarized first conformal dielectric layer prior to forming upon the planarized spin-on-glass (SOG) planarizing dielectric layer and the partially planarized first conformal dielectric layer a second conformal dielectric layer. The partially planarized first conformal dielectric layer, the planarized spin-on-glass (SOG) planarizing dielectric layer and the second conformal dielectric layer form the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed through the method of the present invention.

The spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed through the method of the present invention may be formed as a dielectric layer within integrated circuits of many types. The spin-on-glass sandwich composite planarizing dielectric layer construction formed through the method of the present invention may be formed within integrated circuits including but not limited to dynamic access memory (DRAM) integrated circuits, static random access memory (SRAM) integrated circuits, application specific integrated circuits (ASICs), integrated circuits having within their fabrications field effect transistors (FETs), integrated circuits having within their fabrications bipolar transistors and integrated circuits having within their fabrications bipolar complementary metal oxide semiconductor (BiCMOS) transistors.

Referring now to Fig. 2 to Fig. 6, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive process stages in forming within an integrated circuit a pair of spin-on-glass (SOG) sandwich composite planarizing dielectric layer

constructions in the locations of a first inter-level dielectric (ILD) layer formed separating a pair of patterned first conductor layers from a pair of patterned second conductor layers and a second inter-level dielectric (ILD) layer formed upon the pair of patterned second conductor layers within the integrated circuit. Although the preferred embodiment of the method of the present invention illustrates a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed separating pairs of patterned conductor layers, the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed through the method of the present invention may also be formed upon patterned layers which are not patterned conductor layers. Shown in Fig. 2 is a schematic cross-sectional diagram of the integrated circuit at an early stage in its formation.

Shown in Fig. 2 is a semiconductor substrate 30 having formed within and upon its surface a pair of isolation regions 32a and 32b which define the active region of the semiconductor substrate 30. Although semiconductor substrates are known in the art with either dopant polarity, many dopant concentrations and various crystallographic orientations, for the preferred embodiment of the method of the present invention, the semiconductor substrate 30 is preferably a (100) silicon semiconductor substrate having an N- or P- doping. Similarly, although it is generally known in the art that isolation regions may be formed within integrated circuits through methods including but not limited to isolation region growth methods and isolation region deposition/patterning methods, for the preferred embodiment of the method of the present invention the pair of isolation regions 32a and 32b is preferably formed through a thermal oxidation isolation region growth method where isolation regions 32a and 32b of silicon oxide are formed within and upon the semiconductor substrate 30 through selective oxidation of portions of the semiconductor substrate 30.

There is also shown within and upon the active region of the semiconductor substrate 30 as defined by the isolation regions 32a and 32b a series of components which form a field effect transistor (FET) upon the active region of the semiconductor substrate 30. The series of components includes: (1) a gate oxide layer 34; (2) a gate electrode 36; and (3) a pair of source/drain regions 38a and 38b. The series of components which forms the field effect transistor (FET) upon the active region of the semiconductor substrate 30 may be formed through any of several methods as are conventional in the art of forming field effect transistors (FETs) within integrated circuits.

For example, gate oxide layers are typically, although not exclusively, formed within field effect transistors (FETs) for use within integrated circuits through patterning through methods as are conventional in the art of blanket gate oxide layers formed within those integrated circuits. The blanket gate oxide layers may be formed within integrated circuits through methods including but not limited to blanket gate oxide layer growth methods and blanket gate oxide layer deposition method through which are formed blanket gate oxide layers typically, although not exclusively, of silicon oxide. Similarly, gate electrodes are typically, although not exclusively, formed within field effect transistors (FETs) for use within integrated circuits through analogous patterning methods, as are known in the art, of blanket layers of gate electrode materials. The blanket layers of gate electrode materials may be formed through methods including but not limited to thermally assisted evaporation methods, chemical vapor deposition (CVD) methods and physical vapor deposition (PVD) methods through which may be formed blanket layers of gate electrode materials formed from materials including but not limited to metals, metal alloys, highly doped polysilicon and polycides (highly doped polysilicon/metal silicide stacks). Finally, the source/drain regions are typically formed within field effect transistors (FETs) for use within integrated circuits through ion implantation methods employing dopant ions of polarity suitable to

the field effect transistors (FETs) desired to be formed.

For the preferred embodiment of the method of the present invention, the gate oxide layer 34 is preferably formed through patterning through methods as are conventional in the art of a blanket gate oxide layer formed through thermal oxidation of the active region of the semiconductor substrate 30 at a temperature of from about 900 to about 1100 degrees centigrade to form a blanket gate oxide layer of typical thickness about 50 to about 100 angstroms. In addition, for the preferred embodiment of the method of the present invention, the gate electrode 36 is preferably formed through patterning through methods as are conventional in the art of a blanket layer of highly doped polysilicon or polycide gate electrode material formed upon the blanket gate oxide layer at a thickness of from about 500 to about 3000 angstroms. Finally, for the preferred embodiment of the method of the present invention, the pair of source/drain regions 38a and 38b is preferably formed through implanting through an ion implantation method as is known in the art a suitable dopant ion into the active region of the semiconductor substrate 30 employing the gate oxide layer 34 and the gate electrode 36 as a mask at an ion implantation dose of from about $1E14$ to about $5E15$ dopant ions per square centimeter and an ion implantation energy of from about 30 to about 100 keV.

There is also shown within Fig. 2 the presence of a blanket planarized pre-metal dielectric (PMD) layer 40. Methods and materials through which planarized pre-metal dielectric (PMD) layers may be formed within integrated circuits are known within the art of integrated circuit fabrication. Planarized pre-metal dielectric (PMD) layers are typically formed within integrated circuits through planarizing through methods as are conventional in the art of conformal pre-metal dielectric (PMD) layers formed within integrated circuits. In turn, conformal pre-metal dielectric (PMD) layers may be formed within integrated circuits through methods

including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods and physical vapor deposition (PVD) sputtering methods through which may be formed conformal pre-metal dielectric (PMD) layers of dielectric materials including but not limited to silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials. For the preferred embodiment of the method of the present invention, the blanket planarized pre-metal dielectric (PMD) layer 40 is preferably formed through planarizing through a reactive ion etch (RIE) etchback planarizing method or chemical-mechanical polish (CMP) planarizing method as is conventional in the art of a blanket conformal pre-metal dielectric (PMD) layer formed of a silicon oxide dielectric material deposited through a plasma enhanced chemical vapor deposition (PECVD) method, as is also common in the art. Preferably, the thickness of the blanket planarized pre-metal dielectric (PMD) layer 40 is from about 5000 to about 15000 angstroms.

As is understood by a person skilled in the art, under certain circumstances it may be desirable to employ the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed through the method of the present invention in place of the above described blanket planarized silicon oxide dielectric layer formed through a plasma enhanced chemical vapor deposition (PECVD) method when forming the blanket planarized pre-metal dielectric (PMD) layer 40. The circumstance under which it may be desirable to employ the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed through the method of the present invention when forming the blanket planarized pre-metal dielectric (PMD) layer 40 will be defined principally but not exclusively by the step-height, aperture width and aspect ratio of the integrated circuit device features formed upon the semiconductor substrate 30. Typically the integrated circuit device features formed upon the semiconductor substrate 30 will not simultaneously possess a sufficiently high step-height, a sufficiently narrow aperture width and a

sufficiently high aspect ratio to warrant employing the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed through the method of the present invention when forming the blanket planarized pre-metal dielectric (PMD) layer 40, although such is not precluded.

Finally, there is shown in Fig. 2 the presence of a pair of patterned first conductor layers 42a and 42b formed upon the blanket planarized pre-metal dielectric (PMD) layer 40. Methods and materials through which patterned conductor layers may be formed within integrated circuits are known in the art of integrated circuit fabrication. Patterned conductor layers are typically, although not exclusively, formed within integrated circuits through patterning through methods as are conventional in the art of blanket conductor layers formed within integrated circuits. Blanket conductor layers may be formed within integrated circuits through methods including but not limited to thermally assisted evaporation methods, electron beam assisted evaporation methods and physical vapor deposition (PVD) sputtering methods through which may be formed blanket conductor layers of conductor materials including but not limited to metals, metal alloys and highly doped polysilicon. For the preferred embodiment of the method of the present invention, the patterned first conductor layers 42a and 42b are preferably formed through patterning through a reactive ion etch (RIE) etch patterning method as is common in the art of a blanket first conductor layer formed at least in part of an aluminum containing conductor alloy, as is also common in the art. Preferably, the patterned first conductor layers 42a and 42b so formed have a thickness H2 of from about 4000 to about 10000 angstroms.

While the method of the present invention provides value in forming a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction with minimal process complexity for any width W3 and aspect ratio H2/W3 of the aperture defined by the patterned

first conductor layers 42a and 42b, the method of the present invention provides particular value in forming a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction when the width $W3$ and the aspect ratio $H2/W3$ of the aperture defined by the patterned first conductor layers 42a and 42b is within the range of the width $W1$ and the aspect ratio $H1/W1$ of the aperture defined by the patterned layers 12a and 12b as shown in Fig. 1 and discussed within the Description of the Related Art. Under these more limited ranges for the width $W3$ and the aspect ratio $H2/W3$ of the aperture defined by the patterned first conductor layers 42a and 42b, the method of the present invention provides particular value since the method of the present invention incorporates a chemical-mechanical polish (CMP) planarizing method where a comparatively thin lower lying conformal dielectric layer may be formed upon the patterned first conductor layers 42a and 42b and partially planarized without exposing the patterned first conductor layers 42a and 42b while serving as a polish stop layer when chemical-mechanical polish (CMP) planarizing a spin-on-glass (SOG) planarizing dielectric layer formed upon the comparatively thin lower lying conformal dielectric layer through the chemical-mechanical polish (CMP) planarizing method.

Referring now to Fig. 3, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 2. Shown in Fig. 3 is the presence of a blanket first conformal dielectric layer 44 formed upon the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 2. Methods and materials through which blanket conformal dielectric layers may be formed within integrated circuits have previously been disclosed herein, within the context of the blanket planarized pre-metal dielectric (PMD) layer 44. Similarly to the blanket planarized pre-metal dielectric (PMD) layer 40, the blanket first conformal dielectric layer 44 is preferably formed of a silicon oxide dielectric material deposited through a plasma enhanced

chemical vapor deposition (PECVD) method, preferably employing a silicon source material such as but not limited to tetra-ethyl-ortho-silicate (TEOS) or silane, although other methods and materials may be employed in forming the blanket first conformal dielectric layer 44. Analogously with the above discussion within the Description of the Related Art, the maximum thickness with which the blanket first conformal dielectric layer 44 may typically be formed void free is determined at least in part by the width W_3 and the aspect ratio H_2/W_3 of the aperture defined by the patterned first conductor layers 42a and 42b. Preferably, the thickness of the blanket first conformal dielectric layer 44 is preferably from about 2000 to about 6000 angstroms.

Also shown in Fig. 3 is the presence of a blanket first spin-on-glass (SOG) planarizing dielectric layer 46 formed upon the blanket first conformal dielectric layer 44. Methods and materials through which blanket spin-on-glass (SOG) planarizing dielectric layers may be formed within integrated circuits are known in the art. Methods through which blanket spin-on-glass (SOG) planarizing dielectric layers may be formed within integrated circuits typically include spin coating and thermal curing methods through which a spin-on-glass (SOG) planarizing composition is spin coated and thermally cured upon an integrated circuit to form a spin-on-glass (SOG) planarizing dielectric layer upon the integrated circuit. Several varieties of spin-on-glass (SOG) planarizing compositions are known in the art, including but not limited to inorganic silicate spin-on-glass (SOG) planarizing compositions, organo-functional siloxane spin-on-glass (SOG) compositions, and fluoro-functional spin-on-glass (SOG) planarizing compositions. Each of the preceding spin-on-glass (SOG) planarizing compositions typically includes solvents and other additives as are appropriate to provide optimal spin-on-glass (SOG) planarizing compositions and spin-on-glass (SOG) planarizing dielectric layers. For the preferred embodiment of the method of the present invention, the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 may be formed of an inorganic silicate spin-on-glass (SOG)

planarizing composition, an organo-functional siloxane spin-on-glass (SOG) planarizing composition or a fluoro-functional spin-on-glass (SOG) planarizing composition provided that a chemical mechanical polish (CMP) selectivity ratio for the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 with respect to the blanket first conformal dielectric layer 44 is within a specified range, as discussed below. Preferably, the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 is formed to a thickness greater than the height H2 of the aperture defined by the patterned first conductor layers 42a and 42b, as illustrated in Fig. 2. Typically, the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 will have a thickness of from about 2000 to about 12000 angstroms.

Referring now to Fig. 4 there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 3. Shown in Fig. 4 is the result of planarizing through a chemical mechanical polish (CMP) planarizing method the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 to form the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c while simultaneously partially planarizing the blanket first conformal dielectric layer 44 to form the blanket first partially planarized conformal dielectric layer 44'. In order for the method of the present invention to provide optimal value in forming a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction when there is employed a comparatively thin blanket first conformal dielectric layer 44 due to a narrow width W3 and high aspect ratio H2/W3 of the aperture defined by the patterned first conductor layers 42a and 42b, it is preferred within the preferred embodiment of the method of the present invention that the blanket first conformal dielectric layer 44 serve as a polish stop layer when chemical-mechanical polish (CMP) planarizing the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 to form the planarized first spin-on-glass (SOG) planarizing dielectric layers

46a, 46b and 46c. Typically and preferably it is desired that the chemical mechanical polish (CMP) planarizing method employed in planarizing the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 to form the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c has a chemical-mechanical polish (CMP) selectivity ratio for the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 with respect to the blanket first conformal dielectric layer 44 of at least about 5:1.

While such a chemical-mechanical polish (CMP) selectivity ratio has not traditionally been achievable with silica based chemical-mechanical polish (CMP) polishing slurries as are conventional in the art, there has recently been disclosed in the art the use of cerium oxide chemical-mechanical polish (CMP) polishing slurries through which such a chemical-mechanical polish (CMP) selectivity ratio may be achieved. See, for example Tredinnick et al., as cited within the Description of the Related Art, as above, where the teachings of Tredinnick et al. are incorporated herein fully by reference. Various parameters of a cerium oxide chemical mechanical polish (CMP) polishing slurry may be varied in order to realize the desired chemical-mechanical polish (CMP) selectivity ratio, the parameters including but not limited to: (1) the pH of the slurry; (2) the weight percent cerium oxide in the slurry; (3) the particle size distribution of the cerium oxide within the slurry; (4) the presence of additives within the slurry; and (5) the hardware parameters employed within the chemical-mechanical polish (CMP) planarizing method employing the slurry.

In accord with the teachings of Tredinnick et al., a prophetic example of a cerium oxide chemical mechanical polish (CMP) polishing slurry applicable within the preferred embodiment of the method of the present invention would include: (1) a comparatively large cerium oxide particle size of about 350 nanometers (nm); (2) a comparatively small cerium oxide

concentration of about 3 weight percent; and (3) a comparatively low pH of about 2.8. Through this prophetic cerium oxide chemical mechanical polish (CMP) polishing slurry there would be polished a blanket spin-on-glass (SOG) planarizing dielectric layer formed from a silsequioxane spin-on-glass (SOG) planarizing composition, such as Allied-Signal No. 418 silsequioxane spin-on-glass (SOG) planarizing composition at a chemical-mechanical polish (CMP) selectivity ratio with respect to a blanket conformal dielectric formed of a silicon oxide deposited through a chemical vapor deposition (CVD) method employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source material of about 5.7:1.

As is shown in Fig. 4, the blanket first spin-on-glass (SOG) planarizing dielectric layer 46 has been planarized to yield the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c, and the blanket first conformal dielectric layer 44 has been partially planarized to yield the blanket first partially planarized conformal dielectric layer 44' to a point such that the upper surfaces of the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c, and the blanket first partially planarized conformal dielectric layer 44' are substantially coplanar. For the purposes of the method of the present invention, the upper surfaces of the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c, and the blanket first partially planarized conformal dielectric layer 44' are substantially coplanar if there may be formed upon those layers a subsequent blanket second conformal dielectric layer without need for additional planarizing of the subsequent blanket second conformal dielectric layer.

Referring now to Fig. 5, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 4. Shown in Fig. 5 is a schematic cross-sectional diagram

of an integrated circuit analogous to the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 4 but upon whose surface is formed a blanket second conformal dielectric layer 48 which needs no additional planarizing. Methods and materials through which is formed the blanket second conformal dielectric layer 48 are preferably equivalent to the methods and materials through which is formed the blanket first conformal dielectric layer 44. However, the blanket second conformal dielectric layer 48 is typically and preferably thicker than the blanket first conformal dielectric layer 44, although the blanket second conformal dielectric layer 48 may be substantially thinner than upper lying conformal dielectric layers formed within spin-on-glass (SOG) sandwich composite planarizing dielectric layer constructions as are conventional in the art since the blanket second conformal dielectric layer 48 needs no additional planarizing. Preferably, the blanket second conformal dielectric layer 48 has a thickness of from about 4000 to about 8000 angstroms.

Upon forming within the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 5 the blanket second conformal dielectric layer 48, there is formed an integrated circuit having formed therein a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed from the blanket first partially planarized conformal dielectric layer 44', the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c, and the blanket second conformal dielectric layer 48. In accord with the objects of the present invention, the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction so formed: (1) may be formed without damaging the patterned first conductor layers 42a and 42b; and (2) may have vias formed through the blanket second conformal dielectric layer 48 and the blanket first partially planarized conformal dielectric layer 44', reaching the patterned first conductor layers 42a and 42b without passing through the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c.

As is understood by a person skilled in the art, the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction as illustrated in Fig. 5 may be formed in locations within an integrated circuit analogous to the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 5 other than upon the patterned first conductor layers. A schematic cross-sectional diagram of such an integrated circuit is illustrated in Fig. 6.

Shown in Fig. 6 is a schematic cross-sectional diagram of an integrated circuit otherwise equivalent to the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 5 but through whose blanket second conformal dielectric layer 48 and blanket first partially planarized conformal dielectric layer 44' is formed, through methods as are conventional in the art, a pair of vias defined by a series of patterned second conformal dielectric layers 48a, 48b and 48c, and a corresponding series of patterned first partially planarized conformal dielectric layers 44a', 44b' and 44c'. The pair of vias has formed therein a pair of conductive interconnection studs 50a and 50b. Methods and materials through which conductive interconnection studs may be formed within integrated circuits are known in the art of integrated circuit fabrication. Conductive interconnection studs may be formed within integrated circuits through methods including but not limited to thermally assisted evaporation methods, electron beam assisted evaporation methods and physical vapor deposition (PVD) sputtering methods through which may be formed conductive interconnection studs of conductive materials including but not limited to metals, metal alloys and highly doped polysilicon. For the preferred embodiment of the method of the present invention, the conductive interconnection studs 50a and 50b are preferably formed at least in part of tungsten metal deposited through a chemical vapor deposition (CVD) method, as is common in the art. The conductive interconnection studs 50a and 50b are preferably formed of a thickness sufficient to reach the upper surfaces of the patterned second conformal dielectric layers 48a, 48b and 48c while simultaneously contacting the

corresponding patterned first conductor layer 42a or 42b.

Finally, there is shown in Fig. 6: (1) a pair of patterned second conductor layers 52a and 52b which contact the pair of conductive interconnection studs 50a and 50b; (2) a blanket third partially planarized conformal dielectric layer 54'; (3) a series of planarized second spin-on-glass (SOG) planarizing dielectric layers 56a, 56b and 56c; and (4) a blanket fourth conformal dielectric layer 58. The pair of patterned second conductor layers 52a and 52b is preferably formed through methods, materials and dimensions equivalent to the methods, materials and dimensions employed in forming the pair of patterned first conductor layers 42a and 42b. Analogously, the blanket third partially planarized conformal dielectric layer 54' is preferably formed through methods, materials and dimensions equivalent to the methods, materials and dimensions employed in forming the blanket first partially planarized conformal dielectric layer 44'. Similarly, the series of planarized second spin-on-glass (SOG) planarizing dielectric layers 56a, 56b and 56c is preferably formed through methods, materials and dimensions equivalent to the methods, materials and dimensions employed in forming the planarized first spin-on-glass (SOG) planarizing dielectric layers 46a, 46b and 46c. Finally, the blanket fourth conformal dielectric layer 58 is preferably formed through methods, materials and dimensions equivalent to the methods, materials and dimensions employed in forming the blanket second conformal dielectric layer 48.

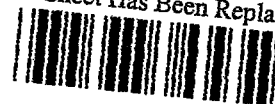
Upon forming the blanket fourth conformal dielectric layer 58, there is formed an integrated circuit having formed therein a second spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction upon a pair of patterned second conductor layers 52a and 52b. The second spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction consists of: (1) the blanket third partially planarized conformal dielectric layer 54';

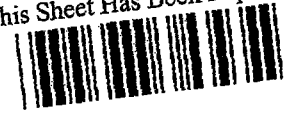
(2) the planarized second spin-on-glass (SOG) planarizing dielectric layers 56a, 56b and 56c; and
(3) the blanket fourth conformal dielectric layer 58. The second spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction exhibits the properties as noted above for the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction formed upon the patterned first conductor layers 42a and 42b.

As is understood by a person skilled in the art, the preferred embodiment of the present invention and the prophetic example of the cerium oxide chemical mechanical polish (CMP) slurry composition employed within the preferred embodiment of the method of the present invention are illustrative of the present invention rather than limiting of the present invention. Modifications may be made to methods, materials, structures, and dimensions through which is provided the preferred embodiment of the present invention and prophetic example of the cerium oxide chemical mechanical polish (CMP) slurry composition employed within the preferred embodiment of the method of the present invention while still providing an embodiment and slurry composition within the spirit and scope of the present invention, as encompassed by the appended claims.

What is claimed is:

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1. A method for forming for use upon a patterned layer within an integrated circuit a spin-on-glass sandwich composite planarizing dielectric layer construction comprising:

providing a substrate;

forming upon the substrate a patterned layer, the patterned layer having a minimum of one aperture formed at least partially through the patterned layer, the patterned layer having an upper portion of the patterned layer further from the substrate, the patterned layer also having a lower portion of the patterned layer closer to the substrate;

forming upon the patterned layer a first conformal dielectric layer, the first conformal dielectric layer having an upper portion of the first conformal dielectric layer formed upon the upper portion of the patterned layer and a lower portion of the first conformal dielectric layer formed closer to the substrate;

forming upon the first conformal dielectric layer a spin-on-glass (SOG) planarizing dielectric layer, the spin-on-glass (SOG) planarizing dielectric layer being formed over both the upper portion of the first conformal dielectric layer and the lower portion of the first conformal dielectric layer, the spin-on-glass (SOG) planarizing dielectric layer having a thickness upon the lower portion of the first conformal dielectric layer greater than the depth of the aperture within the patterned layer;

planarizing through a chemical mechanical polish (CMP) planarizing method the spin-on-glass (SOG) planarizing dielectric layer and the upper portion of the first conformal dielectric layer to form a planarized spin-on-glass (SOG) planarizing dielectric layer substantially coplanar with a partially planarized first conformal dielectric layer, the planarizing being undertaken without exposing the upper portion of the patterned layer; and

forming upon the planarized spin-on-glass (SOG) planarizing dielectric layer and partially planarized first conformal dielectric layer a second conformal dielectric layer.



2. The method of claim 1 wherein the width of the aperture within the patterned layer is from about 2000 to about 8000 angstroms and the aspect ratio of the aperture within the patterned layer is greater than about 2.

3. The method of claim 1 wherein the thickness of the first conformal dielectric layer is from about 2000 to about 6000 angstroms.

4. The method of claim 1 wherein:

the first conformal dielectric layer is formed from a silicon oxide dielectric material deposited through a plasma enhanced chemical vapor deposition (PECVD) method employing a silicon source material chosen from the group of silicon source materials consisting of tetra-ethyl-ortho-silicate and silane; and

the spin-on-glass (SOG) planarizing dielectric layer is formed from a spin-on-glass (SOG) planarizing composition chosen from the group of spin-on-glass (SOG) planarizing compositions consisting of inorganic silicate spin-on-glass (SOG) planarizing compositions, organo-functional siloxane spin-on-glass (SOG) planarizing compositions and fluoro-functional spin-on-glass (SOG) planarizing compositions.

5. The method of claim 4 wherein the chemical mechanical polish (CMP) method employs a cerium oxide (CeO) slurry composition.

6. The method of claim 5 wherein the chemical mechanical polish (CMP) method has a chemical mechanical polish (CMP) selectivity ratio for the spin-on-glass (SOG) planarizing dielectric layer with respect to the first conformal dielectric layer of at least about 5:1.



7. The method of claim 1 further comprising forming a field effect transistor (FET) within and upon the substrate.
8. An integrated circuit having formed therein a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction in accord with the method of claim 1.
9. The integrated circuit of claim 8 wherein the integrated circuit has a field effect transistor (FET) formed therein.
10. A method for forming through a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction within an integrated circuit a via to a patterned conductor layer formed beneath the spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction comprising:
 - providing a substrate;
 - forming upon the substrate a patterned conductor layer, the patterned conductor layer having a minimum of one aperture formed at least partially through the patterned conductor layer, the patterned conductor layer having an upper portion of the patterned conductor layer further from the substrate, the patterned conductor layer also having a lower portion of the patterned conductor layer closer to the substrate;
 - forming upon the patterned conductor layer a first conformal dielectric layer, the first conformal dielectric layer having an upper portion of the first conformal dielectric layer formed upon the upper portion of the patterned conductor layer and a lower portion of the first conformal dielectric layer formed closer to the substrate;
 - forming upon the first conformal dielectric layer a spin-on-glass (SOG) planarizing dielectric layer, the spin-on-glass (SOG) planarizing dielectric layer being formed over



both the upper portion of the first conformal dielectric layer and the lower portion of the first conformal dielectric layer, the spin-on-glass (SOG) planarizing dielectric layer having a thickness upon the lower portion of the first conformal dielectric layer greater than the depth of the aperture within the patterned conductor layer;

planarizing through a chemical mechanical polish (CMP) planarizing method the spin-on-glass (SOG) planarizing dielectric layer and the upper portion of the first conformal dielectric layer to form a planarized spin-on-glass (SOG) planarizing dielectric layer substantially coplanar with a partially planarized first conformal dielectric layer, the planarizing being undertaken without exposing the upper portion of the patterned conductor layer;

forming upon the planarized spin-on-glass (SOG) planarizing dielectric layer and partially planarized first conformal dielectric layer a second conformal dielectric layer; and

forming a via sequentially through the second conformal dielectric layer and the partially planarized first conformal dielectric layer to the patterned conductor layer without passing through the planarized spin-on-glass (SOG) planarizing dielectric layer.

11. The method of claim 10 wherein the width of the aperture within the patterned conductor layer is from about 2000 to about 8000 angstroms and the aspect ratio of the aperture within the patterned conductor layer is greater than about 2.

12. The method of claim 10 wherein the thickness of the first conformal dielectric layer is from about 2000 to about 6000 angstroms.

13. The method of claim 10 wherein:

the first conformal dielectric layer is formed from a silicon oxide dielectric material



deposited through a plasma enhanced chemical vapor deposition (PECVD) method employing a silicon source material chosen from the group of silicon source materials consisting of tetra-ethyl-ortho-silicate and silane; and

the spin-on-glass planarizing dielectric layer is formed from a spin-on-glass planarizing composition chosen from the group of spin-on-glass planarizing compositions consisting of inorganic silicate spin-on-glass (SOG) planarizing compositions, organo-functional siloxane spin-on-glass (SOG) planarizing compositions and fluoro-functional spin-on-glass (SOG) planarizing compositions.

14. The method of claim 13 wherein the chemical mechanical polish (CMP) method employs a cerium oxide (CeO) slurry composition.

15. The method of claim 14 wherein the chemical mechanical polish (CMP) method has a chemical mechanical polish (CMP) selectivity ratio for the spin-on-glass (SOG) planarizing dielectric layer with respect to the first conformal dielectric layer of at least about 5:1.

16. The method of claim 10 further comprising forming a field effect transistor (FET) within and upon the substrate.

17. An integrated circuit having formed therein a spin-on-glass (SOG) sandwich composite planarizing dielectric layer construction having formed therethrough a via in accord with the method of claim 10.

18. The integrated circuit of claim 17 wherein the integrated circuit has a field effect transistor (FET) formed therein.

