ABSTRACT

A METHOD FOR REDUCING MICROLOADING IN AN ETCH BACK OF SPIN-ON-GLASS OR POLYMER

A method for forming a planarized interlevel dielectric layer without degradation due to the microloading effect from spin-on material etchback is described. A patterned first conducting layer is provided over an insulating layer on a semiconductor substrate. An improved interlevel dielectric layer is formed overlying the patterned first conducting layer by the following steps. A first oxide layer is deposited overlying the patterned first conducting layer and the insulating layer. A spin-on material layer is coated overlying the first oxide layer and etched back using O_2 gas added to the CHF_3/CF_4 chemistry until the first oxide layer is exposed overlying the patterned first conducting layer wherein microloading effects from the etching back of the spin-on material layer are lower than microloading effects in a conventional interlevel dielectric layer. A second oxide layer is deposited to complete the interlevel dielectric layer. A second conducting layer is deposited over the interlevel dielectric layer and patterned to complete the fabrication of the integrated circuit device.

(FIGURE 3 IS SUGGESTED FOR PUBLICATION)