What is claimed is:

1. A memory device, comprising:

a peripheral circuit region including a row decoder and a page buffer; and

a cell region including a plurality of wordlines stacked to each other, a plurality of channel structures penetrating the plurality of wordlines, and a plurality of cell contacts connected to the plurality of wordlines, the plurality of cell contacts are disposed in a first cell contact region and a second cell contact region,

wherein the first cell contact region and the second cell contact region are disposed on both sides of the plurality of channel structures, in a first direction,

the cell region and the peripheral circuit region are stacked in a vertical direction in which the plurality of channel structures are extended,

each of the first cell contact region and the second cell contact region has a plurality of first pads and a plurality of second pads,

in the first direction, a length of each of the plurality of first pads is shorter than a length of each of the plurality of second pads, and

an area of at least one of the plurality of second pads included in the first cell contact region is greater than an area of at least one of the plurality of second pads included in the second cell contact region.

2. The memory device of claim 1, wherein a length of the first cell contact is longer than a length of the second cell contact, in the first direction.

3. The memory device of claim 1, wherein the row decoder includes a plurality of first pass elements and a plurality of second pass elements connected to the plurality of wordlines,

a portion of the plurality of wordlines are connected to the plurality of first pass elements and a remainder of the plurality of wordlines are connected to the plurality of second pass elements, and

each of the plurality of first pass elements is connected to one of the portion of the plurality of wordlines and each of the plurality of second pass elements is connected to one of the remainder of the plurality of wordlines.

4. The memory device of claim 3, wherein the plurality of second pass elements are disposed between the plurality of first pass elements, in the first direction.

5. The memory device of claim 3, wherein the number of the portion of the plurality of wordlines is greater than the number of the remainder of the plurality of wordlines.

6. The memory device of claim 3, wherein the cell region includes a first cell region and a second cell region adjacent to each other, in the first direction, and

at least one of the plurality of second pass elements is disposed between the first cell region and the second cell region, in the first direction.

7. The memory device of claim 3, wherein the cell region includes a first cell region and a second cell region adjacent to each other, in the first direction, and

at least one of the plurality of second pass elements is disposed under a boundary region between the first cell region and the second cell region in the first direction.

8. The memory device of claim 7, wherein the plurality of wordlines are not disposed over the at least one of the plurality of second pass element, in the vertical direction.

9. The memory device of claim 7, wherein the at least one of the plurality of second pass element is connected to two or more of the remainder of the plurality of wordlines, by at least one vertical via extending in the vertical direction, and

in the vertical direction, a length of the at least one vertical via is longer than a length of each of the plurality of cell contacts.

10. The memory device of claim 9, wherein, in the vertical direction, the length of the at least one vertical via is longer than a length of each of the plurality of channel structures.

11. The memory device of claim 1, wherein the number of the plurality of second pads included in the first cell contact region is greater than the number of the plurality of second pads included in the second cell contact region.

12. A memory device, comprising:

a plurality of cell regions, each of the plurality of cell regions including a plurality of wordlines stacked in a vertical direction and extending in a first direction and a plurality of channel structures extending in the vertical direction and penetrating the plurality of wordlines; and

a peripheral circuit region including a plurality of pass elements, and disposed under the plurality of cell regions in the vertical direction,

wherein each of the plurality of cell regions includes a first cell region and a second cell region arranged in the first direction,

at least one pass element of the plurality of pass elements is disposed in a boundary region between the first cell region and the second cell region, and is connected to at least one vertical via crossing a boundary between the peripheral circuit region and the plurality of cell regions, and

the at least one vertical via is commonly connected to at least one of the plurality of wordlines included in the first cell region and at least one of the plurality of wordlines included in the second cell region,

wherein each of the first cell region and the second cell region includes a cell array region in which the plurality of channel structures are disposed and a first cell contact region and a second cell contact region are disposed on both sides of the cell array region in the first direction,

each of the first cell contact region and the second cell contact region has a plurality of first pads and a plurality of second pads,

in the first direction, a length of each of the plurality of first pads is shorter than a length of each of the plurality of second pads, and

an area of at least one of the plurality of second pads included in the first cell contact region is greater than an area of at least one of the plurality of second pads included in the second cell contact region.

13. The memory device of claim 12, wherein the at least one of the plurality of wordlines included in the first cell region and the at least one of the plurality of wordlines included in the second cell region are disposed at the same height, in the vertical direction.

14. The memory device of claim 12, wherein the first cell region and the second cell region have a symmetrical structure, with respect to the boundary region.

15. The memory device of claim 12, wherein in the first direction, the boundary region is disposed between the second cell contact region of the first cell region and the second cell contact region of the second cell region.

16. The memory device of claim 15, wherein a length of the second cell contact region is shorter than a length of the first cell contact region, in the first direction.

17. The memory device of claim 15, wherein each the at least one of the plurality of wordlines included in the first cell region and the at least one of the plurality of wordlines included in the second cell region is commonly connected to the at least one vertical via by cell contacts disposed in the second cell contact region.