

TITLE**PROCESS FOR PREVENTING FORMATION OF PHOTORESIST SCUM****BACKGROUND OF THE INVENTION****1. Field of the Invention:**

5 The present invention relates to a semiconductor process, and more particularly to a process for preventing formation of photoresist scum in order to improve etching profile and prevent clogging of via holes, thus improving subsequent metallization.

10 **2. Description of the Prior Art:**

 In current semiconductor integrated circuit process, photolithography technique is a very critical procedure, in which accurate transfer of the circuit design to the semiconductor substrate determines the product properties. Generally, photolithography technique includes coating, exposure, development, and photoresist stripping. In recent years, with the continuous miniaturization of the device size, photolithography technique needs more improvement and plays a critical role in device quality, yield, and cost.

20 In the dual damascene photolithography process, nitrogen (N) reacts with and contaminates the photoresist. Thus, during the development procedure, amine (NH_x) photoresist scum remains, in turn forming
25 inaccurate pattern and seriously affecting electrical properties of the device. The nitrogen source is from silicon oxynitride (SiON) material of the anti-reflective layer (ARL) and silicon nitride or silicon

carbon nitride (SiCN) material of the etching stop layer. In order to further understand the background of the present invention, the conventional process for forming a dual damascene structure is explained accompanied by
5 FIGS. 1a to 1e.

First, referring to FIG. 1a, an etching stop layer 102 such as silicon nitride or silicon carbon nitride, a dielectric layer 104, an anti-reflective layer 106 such as silicon oxynitride, and a photoresist layer 108 are
10 formed in sequence on a substrate 100.

Subsequently, referring to FIG. 1b, a photoresist pattern layer 108a is formed using exposure and wet development. Since the photoresist layer 108 is contaminated by nitrogen, the photochemical reaction is
15 not complete during exposure. Thus, during wet development, photoresist scum 108b remains on the sidewalls of the photoresist pattern layer 108a. Therefore, when etching is performed on form a via hole 104a, the etching profile is inferior and the critical
20 dimension (CD) is changed as shown in FIG. 1c, seriously affecting electrical properties of the device.

Subsequently, referring to FIG. 1d, after the photoresist pattern layer 108a is removed, a photoresist layer 110 is formed on the anti-reflective layer 106 and
25 in the via hole 104a. Next, referring to FIG. 1e, a photoresist pattern layer 110a is formed by exposure and development. Next, etching is performed to form a trench 104b, making up a dual damascene structure. In the same way, due to nitrogen contamination during the exposure
30 and development processes, photoresist scum 110b clogs

in the via hole 104a. Photoresist scum 110b, detrimental to subsequent metallization and causing device failure, is very difficult to remove even by photoresist stripping.

5 In order to solve the above-mentioned problem, plasma descumming with oxygen plasma is performed on photoresist pattern layers suffering formation of photoresist scum. However, after plasma descumming, the photoresist pattern layer thins and has decreased
10 etching resistance. Also, the resulting pattern will be larger than the original design, which in turn changes electrical properties of the device and does not meet the original device requirements.

 In addition, some researchers have developed
15 special photoresists or developers to prevent formation of photoresist scum. Although the photoresist scum problem is solved, the production cost increases.

SUMMARY OF THE INVENTION

 An object of the present invention is to provide a
20 process for preventing formation of photoresist scum by means of using silicon oxide (SiO_x) or hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) as the anti-reflective layer to prevent nitrogen from contaminating the photoresist. Moreover, a barrier layer is
25 additionally formed on the etching stop layer and another barrier layer is additionally formed below the anti-reflective layer. These two barrier layers can be silicon oxide or hydrocarbon-containing silicon oxide to prevent nitrogen from diffusing into the dielectric

layer, which in turn prevents formation of photoresist scum without causing unfavorable effects on the subsequent process or changing electrical properties of the devices.

5 Another object of the present invention is to provide a process of preventing formation of photoresist scum using a non-amine anti-reflective layer. During the photolithography process, the photoresist scum is prevented by nitrogen contamination.

10 A further object of the present invention is to provide a process of preventing formation of photoresist scum by formation of a barrier layer both below the anti-reflective layer and on the etching stop layer, in order to prevent nitrogen diffusion into the dielectric layer.

15 To achieve the above objects, the present inventive process for preventing formation of photoresist scum includes the following steps. A substrate on which a dielectric layer is formed is provided. Next, a non-amine anti-reflective layer is formed on the dielectric layer. Next, a photoresist pattern layer is formed on the non-amine anti-reflective layer. During the formation of the photoresist pattern layer, the non-amine anti-reflective layer does not react with the photoresist pattern layer, thus not forming photoresist scum. The non-amine anti-reflective layer can be silicon oxide (SiO_x) or hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$).

25 The present invention also provides a process for preventing formation of photoresist scum suitable for

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use in a dual damascene process and the process for preventing formation of photoresist scum includes the following steps. A substrate on which an etching stop layer, a dielectric layer, a first barrier layer, and an anti-reflective layer are formed is provided. The first barrier layer blocks a first dopant in the anti-reflective layer from diffusing into the dielectric layer. Next, the anti-reflective layer and the dielectric layer are etched to form a via hole. Next, a photoresist pattern layer is formed on the anti-reflective layer. The first barrier layer blocks the first dopant in order to prevent photoresist scum forming in the via hole. Finally, the anti-reflective layer and the dielectric layer are etched using the photoresist pattern layer as a mask to form a trench above the via hole, thus forming a dual damascene structure. The process can further include forming a second barrier layer between the etching stop layer and the dielectric layer in order to block a second dopant in the etching stop layer from diffusing into the dielectric layer. The first and second barrier layers can be silicon oxide (SiO_x) or hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) and have a thickness of 50 to 1000 Å. The first and second dopants can be nitrogen.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way

of illustration only and thus not intended to be
limitative of the present invention.

FIGS. 1a to 1e are cross-sections illustrating the
conventional process flow of forming a dual damascene
5 structure.

FIGS. 2a to 2e are cross-sections illustrating the
process flow of forming a dual damascene structure
according to a first embodiment of the present invention.

FIGS. 3a to 3e are cross-sections illustrating the
process flow of forming a dual damascene structure
10 according to a second embodiment of the present
invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 2a to 2e are cross-sections illustrating the
process flow of preventing formation of photoresist scum
15 according to a first embodiment of the present invention.

First, referring to FIG. 2a, a substrate 200 such
as a silicon wafer is provided. Although there are
semiconductor devices formed on the substrate 200, a flat
20 substrate is depicted for simplicity. Next, an etching
stop layer 202, a barrier layer 203, and a dielectric
layer 204 are formed on the substrate 200. The material
of the etching stop layer 202 can constitute silicon
nitride or silicon carbon nitride. The barrier layer 203
25 can comprise silicon oxide (SiO_x) or hydrocarbon-
containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) having a thickness of
50 to 1000 Å to block the dopant such as nitrogen in the
etching stop layer 202 from diffusing into the dielectric
layer 204. In addition, in the present embodiment, the

etching stop layer 202 can also use material containing no nitrogen, such as silicon oxide (SiO_x) or hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$). In this way, there is no need to form the above-mentioned barrier layer 203. Next, a non-amine anti-reflective layer 206 and a photoresist layer 208 are formed on the dielectric layer 204. The non-amine anti-reflective layer 206 can be silicon oxide (SiO_x) or hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$).

Subsequently, referring to FIG. 2b, a photoresist pattern layer 208a is formed using conventional exposure and wet development procedures. Since the non-amine anti-reflective layer 206 contains no nitrogen, the photoresist layer 208 does not react with nitrogen during the photolithography process. That is, during wet development, no photoresist scum remains on the sidewalls of the photoresist pattern layer 208a.

Subsequently, referring to FIG. 2c, the non-amine anti-reflective layer 206, the dielectric layer 204, and the barrier layer 203 are etched in sequence using the photoresist pattern layer 208a as an etching mask, thus exposing the etching stop layer 202 surface and forming a via hole 204a. Since there is no photoresist scum, the via hole 204a has a better profile. In addition, since no plasma descumming is required, the critical dimension (CD) does not change.

Subsequently, referring to FIG. 2d, the photoresist pattern layer 208a is removed to expose the surface of the non-amine anti-reflective layer 206. Next, a

photoresist layer 210 is formed on the non-amine anti-reflective layer 206 and in the via hole 204a.

5 Finally, referring to FIG. 2e, a photoresist pattern layer 210a is formed using the exposure and development procedures, forming a trench. In the same way, the photoresist pattern layer 210a does not react with the non-amine anti-reflective layer 206 to form residual scum. On the other side, although the etching stop layer 202 contains nitrogen, nitrogen cannot
10 diffuse into the dielectric layer 204 because of the blocking of the barrier layer 203. Thus, the photoresist layer 210 in the via hole 204a will not be contaminated, and no photoresist scum forms in the via hole 204a.

15 FIGS. 3a to 3e are cross-sections illustrating the process flow of preventing formation of photoresist scum according to a second embodiment of the present invention.

First, referring to FIG. 3a, in the same way, a substrate 300 such as a silicon wafer is provided. Next,
20 an etching stop layer 302, a second barrier layer 303, a dielectric layer 304, a first barrier layer 305, an anti-reflective layer 306, and a photoresist layer 308 are formed on the substrate 300. The etching stop layer 302 can comprise silicon nitride or silicon carbon
25 nitride. The anti-reflective layer 306 can be silicon oxynitride. The first and second barrier layers 305 and 303 can comprise silicon oxide (SiO_x) or hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) having a thickness of 50 to 1000 Å to block the dopant such as nitrogen in the

etching stop layer 302 and in the anti-reflective layer 306 from diffusing into the dielectric layer 304.

Subsequently, referring to FIG. 3b, a photoresist pattern layer 308a is formed using conventional exposure and wet development procedures. Next, referring to FIG. 3c, the anti-reflective layer 306, the first barrier layer 305, the dielectric layer 304, and the second barrier layer 303 are etched in sequence using the photoresist pattern layer 308a as an etching mask, thus exposing the surface of the etching stop layer 302 and forming the via hole 304a.

Subsequently, referring to FIG. 3d, the photoresist pattern layer 308a is removed to expose the surface of the anti-reflective layer 306. Next, a photoresist layer 310 is formed on the anti-reflective layer 306 and in the via hole 304a.

Finally, referring to FIG. 3e, a photoresist pattern layer 310a is formed using the exposure and development procedures. In the same way, during the photolithography process, although the anti-reflective layer 306 and the etching stop layer 302 contain nitrogen, nitrogen cannot diffuse into the dielectric layer 304 because of the blocking of the first and second barrier layers 305 and 303 respectively. Thus, the photoresist layer 310 in the via hole 304a will not be contaminated, and there is no photoresist clogging of the via hole 304a, thus improving the subsequent metallization.

According to the inventive process, photoresist scum is effectively prevented by the use of the non-amine

material as the anti-reflective layer, the etching stop layer, or the barrier layer. In addition, since no plasma descumming is required and no special photoresist or developer is used, the critical dimension does not change
5 and the production cost is decreased.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are possible in light of the
10 above teaching. The embodiments chosen and described provide an excellent illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as
15 are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.

What is claimed is:

1. A process for preventing formation of photoresist scum, comprising the following steps:

providing a substrate on which a dielectric layer is
5 formed;

forming a non-amine anti-reflective layer on the
dielectric layer, said non-amine anti-reflective
layer being a hydrocarbon-containing silicon
oxide ($\text{SiO}_x\text{C}_y\text{H}$) layer; and

10 forming a photoresist pattern layer on the non-amine
anti-reflective layer, wherein during the
formation of the photoresist pattern layer, the
non-amine anti-reflective layer does not react
with the photoresist pattern layer, said non-
15 amine anti-reflective layer being a hydrocarbon-
containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) layer, thus
not forming photoresist scum.

2. The process as claimed in claim 1, further
comprising forming an etching stop layer containing no
20 nitrogen between the substrate and the dielectric layer.

3. A process for preventing formation of photoresist
scum, comprising the following steps:

providing a substrate on which a dielectric layer is
formed;

25 forming a non-amine anti-reflective layer on the
dielectric layer;

forming a first photoresist pattern layer on the non-
amine anti-reflective layer, wherein during the

formation of the first photoresist pattern layer, the non-amine anti-reflective layer does not react with the first photoresist pattern layer, thus not forming photoresist scum;

5 etching the non-amine anti-reflective layer and the dielectric layer using the first photoresist pattern layer as a mask to form a via hole; removing the first photoresist pattern layer to expose the non-amine anti-reflective layer surface; and
10 forming a second photoresist pattern layer on the non-amine anti-reflective layer, wherein during the formation of the second photoresist pattern layer, the non-amine anti-reflective layer does not react with the second photoresist pattern layer, thus
15 not forming photoresist scum.

4. The process as claimed in claim 3, further comprising forming an etching stop layer between the substrate and the dielectric layer.

20 5. The process as claimed in claim 4, further comprising forming a barrier layer between the etching stop layer and the dielectric layer to block a dopant in the etching stop layer from diffusing into the dielectric layer.

25 6. The process as claimed in claim 3, wherein the non-amine anti-reflective layer is a silicon oxide (SiO_x) layer.

7. The process as claimed in claim 3, wherein the non-amine anti-reflective layer is a hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) layer.

8. The process as claimed in claim 5, wherein the barrier layer has a silicon oxide (SiO_x) layer.

9. The process as claimed in claim 5, wherein the barrier layer is a hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{H}$) layer.

10. The process as claimed in claim 5, wherein the barrier layer has a thickness of 50 to 1000 Å.

11. The process as claimed in claim 5, wherein the dopant is nitrogen.

12. A process for preventing formation of photoresist scum suitable for use in a dual damascene process, comprising the following steps:

providing a substrate on which an etching stop layer, a dielectric layer, a first barrier layer, and an anti-reflective layer are formed, wherein the first barrier layer blocks a first dopant in the anti-reflective layer from diffusing into the dielectric layer;

etching the anti-reflective layer and the dielectric layer to form a via hole;

forming a photoresist pattern layer on the anti-reflective layer, wherein the first barrier layer blocks the first dopant in order to prevent forming photoresist scum in the via hole; and

etching the anti-reflective layer and the dielectric layer using the photoresist pattern layer as a mask to form a trench above the via hole, thus forming a dual damascene structure.

5 13. The process as claimed in claim 12, wherein the first barrier layer is a silicon oxide (SiO_x) layer.

14. The process as claimed in claim 12, wherein the first barrier layer is a hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{:H}$) layer.

10 15. The process as claimed in claim 12, wherein the first barrier layer has a thickness of 50 to 1000 Å.

16. The process as claimed in claim 12, wherein the first dopant is nitrogen.

15 17. The process as claimed in claim 12, further comprising forming a second barrier layer between the etching stop layer and the dielectric layer, wherein the second barrier layer blocks a second dopant in the etching stop layer from diffusing into the dielectric layer.

20 18. The process as claimed in claim 17, wherein the second barrier layer is a silicon oxide (SiO_x) layer.

19. The process as claimed in claim 17, wherein the second barrier layer is a hydrocarbon-containing silicon oxide ($\text{SiO}_x\text{C}_y\text{:H}$) layer.

25 20. The process as claimed in claim 17, wherein the second barrier layer has a thickness of 50 to 1000 Å.

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21. The process as claimed in claim 17, wherein the second dopant is nitrogen.