SPACER AND PROCESS TO ENHANCE THE STRAIN IN THE CHANNEL WITH STRESS LINER

DESCRIPTION

Field of the Invention

[0001] The present invention relates to a spacer used to make the stress liner close to the gate.

Background Description

[0002] Mechanical stresses within a semiconductor device substrate can modulate device performance. That is, stresses within a semiconductor device are known to enhance semiconductor device characteristics. Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses are created in the channel of the NFETs and/or PFETs.

[0003] It is known, for example, to provide a patterned and oxidized silicon liner in isolation regions, or spacers on gate sidewalls, to selectively induce the appropriate strain in the channels of the FET devices. By providing patterned oxidized spacers, the appropriate stress is applied closer to the device than the stress applied as a result of the trench isolation fill technique.

[0004] While these methods provide structures applying stresses to the devices, they

may require additional materials and/or more complex processing, and thus, result in higher cost. In addition, in the methods described above, for example, the stresses in the channel are relatively moderate, which provide only moderate benefit in device performance.

[0005] Further, nitride stress liners have been used to improve device performance with enhanced carrier mobility in the channel. The strain induced in the channel by the liner, e.g., nitride, is sensitive to the distance between stress liner and the gate, which is separated by a spacer. However, in an effort to arrange the nitride close to the gate, the spacer is removed.

[0006] Further, it is known in the art to utilize two spacers, e.g., a first oxide spacer and a second nitride spacer, and to remove only the second nitride spacer. However, this still disadvantageously results in an oxide spacer of 10 - 20 nm remaining between the gate and nitride liner. Moreover, another thin oxide layer is below the nitride cover layer which can relax the strain in the channel.

SUMMARY OF THE INVENTION

[0007] A first aspect of the invention is directed to a process for enhancing strain in a channel with a stress liner. The process includes applying a first spacer composed of an first oxide and first nitride layer to a gate electrode on a substrate, applying a second spacer composed of a second oxide and second nitride layer, performing an extension/halo implantation before the applying of the second spacer, deep implanting source and drain in the substrate, removing the second nitnde, second oxide, and first nitride layers to form an L-shaped oxide spacer adjacent the gate electrode; and depositing a stress contact liner over the gate and the L-shaped spacer.

[0008] According to a feature of the present invention, the gate electrode may be formed by a poly gate etch. Moreover, the first oxide layer can be formed by gate reoxidation, and the first oxide layer can have a thickness of 1- 5 nm. The first nitride layer may have a thickness of 10 - 15 nm.

[0009] In accordance with another feature of the invention, the removing of the first and second nitride layers and the second oxide iayer can form an L-shaped oxide spacer adjacent the gate electrode spacer, and the process may further include depositing a stress contact liner over the gate and the L-shaped spacer.

[0010] According to a further feature of the present invention, the process can include forming silicide (on the gate electrode and the source/drain region) before the removal of the first and second nitride layers and the second oxide layer. Alternatively, the process can include forming silicide after the removal of the first and second nitride layers and the second oxide layer. Further, the removing of the first and second nitride layers and the second oxide layer can include one of a wet etch or a reactive ion etch.

[0011] Embodiments of the invention are directed to a spacer for enhancing stain in a channel. The spacer includes a first spacer composed of an first oxide couplable to a gate electrode and first nitride iayer coupled to the first oxide layer, and a second spacer composed of a second oxide coupled to the first oxide layer and a second nitride layer coupled to the second oxide layer. The first and second nitride layers and the second oxide layer are removable to form an L-shaped oxide spacer.

[0012] A second aspect of the present invention is directed to a process for forming an integrated circuit. The process includes forming a gate electrode on a substrate, forming an L-shaped oxide spacer adjacent the gate electrode, and depositing a stress liner over the gate electrode and the L-shaped spacer, wherein the forming of the L-shaped spacer comprises forming a first oxide/nitride spacer, performing an extension/halo implantation, forming a second oxide/nitride spacer, and removing the second oxide/nitride spacer and the nitride of the first oxide/nitride spacer.

[0013] According to a feature of the present invention, a vertical extent of the L-shaped oxide spacer can have a thickness between 1-5 nm. Further, the L-shaped spacer can be formed by a first oxide/nitride spacer and a second oxide/nitride spacer, in which the second oxide/nitride spacer and the nitride of the first oxide/nitride spacer are removed.

[0014] In accordance with the process, the forming of the L-shaped oxide layer may include forming an oxide layer over the gate electrode by reoxidation, depositing a first nitride layer over the oxide layer, forming a first spacer by reactive ion etching (RIE) and then performing an extension/halo implantation. The process also includes depositing a second oxide layer over the first nitride layer, depositing a second nitride layer over the second oxide layer, forming a second spacer by RIE, and removing the second nitride, second oxide, and first nitride layers. Moreover, prior to removing the second oxide and the first and second nitride layers, the process can include deep implanting source and drain in the substrate. The process can also include forming silicide on the gate electrode after the removal of the first and second nitride layers and the second oxide layer, or, alternatively, forming silicide before the removal of the first and second nitride

layers and the second oxide layer. The removing of the first and second nitride layers and the second oxide layer can include one of a wet etch or a reactive ion etch.

[0015] In accordance with another feature of the invention, the gate electrode may be formed by a poly gate etch.

[0016] Embodiments of the present invention are directed to an integrated circuit having a gate electrode formed on a substrate, an L-shaped oxide spacer arranged adjacent the gate electrode, and a stress liner deposited over the gate electrode and the L-shaped spacer.

[0017] According to a feature of the invention, a vertical extent of the L-shaped oxide spacer can have a thickness between 1 - 5 nm. The L-shaped spacer can be formed by a first oxide/nitride spacer and a second oxide/nitride spacer, in which the second oxide/nitride spacer and the nitride of the first oxide/nitride spacer are removed. Further, the L-shaped oxide layer can be formed by removing nitride from an oxide/nitride spacer. A source and drain may be formed through deep implantation in the substrate. Further, silicide can be formed on the gate electrode and source/drain after removing nitride from an oxide/nitride spacer, or silicide can be formed before removing nitride from an oxide/nitride spacer. Moreover, the gate electrode may be formed by a poly gate etch.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Figs. 1 - 9 schematically illustrate process according to a first embodiment of

the invention for forming the structure of the present invention;

[0019] Figs. 10 – 12 schematically illustrate a process according to a second embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

[0020] A first oxide/nitride spacer is utilized before the halo/extension implant. The oxide layer is formed by reoxidation and can be as thin as 1 – 5 nm, preferably 1 – 2 nm. The nitride layer can be removed with a second spacer and before nitride cover layer deposition. In this manner, maximum stain can be induced in the channel to improve device performance.

[0021] Strain in the channel of MOSFET is sensitive to the proximity of nitride to the gate. The present invention is directed to a disposable spacer to make the stress liner close the gate, which includes a first spacer, e.g., oxide/nitride, of which the nitride layer is subsequently removed. As a result, the nitride stress liner may only be a few nanometers from the gate, which can increase the strain in the channel.

[0022] A first embodiment of the invention, illustrated in Figs. 1 – 9, enhances strain in the channel with a stress liner. As shown in Fig. 1, a gate 10, e.g., a poly gate, is formed on a substrate 20, e.g., silicon or other suitable material, through a poly gate etch. An insulating layer 15 is formed between gate 10 and substrate 20. In Fig. 2, an oxide layer 30 is formed over gate 10 and substrate 20 to protect gate 10. Preferably, oxide layer 30 has a thickness that generally corresponds to the thickness of insulating layer 15 between gate 10 and substrate 20. Oxide layer 30, e.g., 1 – 5 nm, can be

formed by gate reoxidation. It is noted that, in the prior art, oxide layers protecting the gate have a thickness of 10-20 nm. Subsequently, a nitride layer 40, e.g., 10-15 nm, is deposited over the oxide layer by nitride deposition in Fig. 3. In Fig. 4, portions of the nitride and oxide layers are etched, e.g., via reactive ion etching (RIE) to form first spacers 50 on the sides of gate 10. In this regard, the oxide layer beneath the nitride is etched to extend, e.g., 10 - 20 nm from gate insulator 15 along substrate 20.

[0023] Extension/halo implantation is performed, as is schematically illustrated in Fig. 5, after formation of first spacer 50. After implantation, as illustrated in Fig. 6, a second oxide layer 70 is deposited over first nitride layer 40, and a second nitride layer 80 is deposited over second oxide layer 70. A second spacer 60 is formed by RIE.

[0024] As illustrated in Fig. 7, a deep source/drain implant is performed, as well as a silicide formation 90 in gate 10 and the source/drain region, in Fig. 8, a nitride/oxide/nitride removal, e.g., via wet etch or RSE, is performed. Thus, as shown in g. 8, an L-shaped spacer (oxide layer) 30' is formed at the edges of gate 10. In accordance with the invention, L-shaped spacer 30' is significantly thinner than that in the prior art without loss of performance.

[0025] As shown in Fig. 9, a stress liner 100, e.g., a nitride CA (contact) liner, is deposited over gate 10, L-shaped spacer 30', and substrate 20. Because of the significantly thinner construction of L-shaped spacer 30', as compared to the prior art oxide spacer, stress liner 100 is arranged only a few nanometers from gate 10, which increases the strain in the channel.

[0026] In a second embodiment of the invention, the formation process in accordance with Figs. 1 – 6 is performed. Subsequently, as shown in Fig. 10, a deep source/drain implant is performed. However, in contrast to the previous embodiment, silicide formation does not yet occur. In Fig. 11, a nitride/oxide/nitride removal, e.g., via wet etch or RIE, is performed. Thus, as shown in Fig. 11, an L-shaped spacer 30' is formed at the edges of gate 10. Fig. 12 shows a silicide formation 90 on gate 10 and the source/drain region. Thereafter, the process proceeds in accordance with Fig. 9, such that a stress liner 100, e.g., a nitride CA (contact) liner, is deposited over gate 10, L-shaped spacer 30', and substrate 20, whereby stain in the channel is enhanced due to the thin construction of L-shaped spacer 30' separating gate 10 and stress liner 100.

[0027] The circuit as described above is part of the design for an integrated circuit chip. The chip design is created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer transmits the resulting design by physical means (e.g., by providing a copy of the storage medium storing the design) or electronically (e.g., through the Internet) to such entities, directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which typically include multiple copies of the chip design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

[0028] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.

WHAT IS CLAIMED:

1. A process for enhancing strain in a channel with a stress liner, comprising:

applying a first spacer composed of an first oxide and first nitride layer to a gate electrode on a substrate;

applying a second spacer composed of a second oxide and second nitride layer;

performing an extension/halo implantation before the applying of the second spacer;

deep implanting source and drain in the substrate;

removing the second nitride, second oxide, and first nitride layers to form an L-shaped oxide spacer adjacent the gate electrode; and

depositing a stress contact liner over the gate and the L-shaped spacer.

2. The process in accordance with claim 1, wherein the gate electrode is formed by a poly gate etch.

3. The process in accordance with claim 1, wherein the first oxide layer is formed by gate reoxidation.

4. The process in accordance with claim 3, wherein the first oxide layer has a thickness of 1 - 5 nm.

5. The process in accordance with claim 1, wherein the first nitride layer has a thickness of 10 - 15 nm.

6. The process in accordance with claim 1, further comprising forming silicide on the gate electrode and a source/drain region before the removal of the first and second nitride layers and the second oxide layer.

7. The process in accordance with claim 1, further comprising forming silicide on the gate electrode and a source/drain region after the removal of the first and second nitride layers and the second oxide layer.

8. The process in accordance with claim 1, wherein the removing of the first and second nitride layers and the second oxide layer comprises one of a wet etch or a reactive ion etch.

9. A process for forming an integrated circuit, comprising:

forming a gate electrode on a substrate;

forming an L-shaped oxide spacer adjacent the gate electrode; and depositing a stress liner over the gate electrode and the L-shaped spacer

wherein the forming of the L-shaped spacer comprises forming a first oxide/nitride spacer, performing an extension/halo implantation, forming a second oxide/nitride spacer, and removing the second oxide/nitride spacer and the nitride of the first oxide/nitride spacer.

10. The process in accordance with claim 9, wherein a vertical extent of the L-shaped oxide spacer has a thickness between 1-5 nm.

11. The process in accordance with claim 9, wherein the

first oxide layer is formed over the gate electrode by reoxidation,

the first nitride layer is deposited over the oxide layer,

the second oxide layer is deposited over the first nitride layer after the extension/halo implantation, and

the second nitride layer is deposited over the second oxide layer

12. The process in accordance with claim 11, wherein prior to removing the second oxide and the first and second nitride layers, the process further comprises deep implanting source and drain in the substrate.

13. The process in accordance with claim 11, further comprising forming silicide after the removal of the first and second nitride layers and the second oxide layer.

14. The process in accordance with claim 11, further comprising forming silicide before the removal of the first and second nitride layers and the second oxide layer.

15. The process in accordance with claim 11, wherein the removing of the first and second nitride layers and the second oxide layer comprises one of a wet etch or a reactive ion etch.

16. The process in accordance with claim 9, wherein the gate electrode is formed by a poly gate etch.