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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

The diagram illustrates a pixel circuit and its control logic. The pixel circuit, labeled 100, consists of a Ramp Generator (106) connected to a capacitor C1. The other end of C1 is connected to a switch S4. The other end of S4 is connected to a Column Line (98). The Column Line (98) is also connected to a switch S3, which is controlled by a signal Cpxl (96). The other end of S3 is connected to a common source terminal (94) of a PMOS transistor (90). The gate of transistor 90 is connected to a signal Vpch (91). The drain of transistor 90 is connected to the Column Line (98). The Column Line (98) is also connected to a switch S5, which is controlled by a signal CLOCK (102). The other end of S5 is connected to a Counter (104). The Counter (104) is also connected to an Arithmetic unit (108) and a Latches unit (110). The Latches unit (110) is connected to a Synchronizer (112). The Synchronizer (112) is connected to a CLOCK signal (114).

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