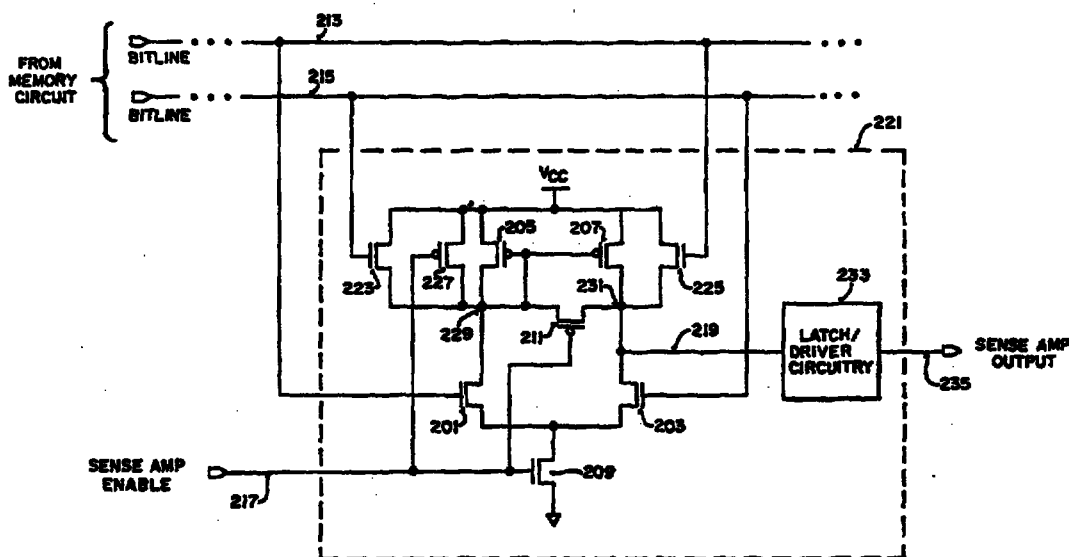




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(54) Title: BITLINE LEVEL INSENSITIVE SENSE AMPLIFIER



(57) Abstract

A sense amplifier (221) for detecting the difference in voltage between two bitlines (113, 115) of a memory circuit. The sense amplifier is comprised of a differential amplifier (201, 203) which is coupled to the two bitlines (113, 115) and generates an output signal based on voltage levels sensed in the bitlines (113, 115). The differential amplifier (201, 203) is coupled to Vcc and ground through an active load (205, 207) and a current source (209) respectively. To address the problem of increased common mode voltage levels found in the bitlines (113, 115), a pair of transistors (223, 225) are connected in parallel across the active load (205, 207) to Vcc and the differential amplifier (202, 203). The gate of one of the transistors is coupled to one of the bitlines (113, 115) and the gate of the other one of the transistors is coupled to the other one of the bitlines (113, 115). With these two transistors (223, 225) coupled in parallel across the load (205, 207) as described, the differential amplifier (201, 203) has increased immunity to elevated common mode levels found in the bitlines (113, 115).