1. A system comprising:

a computer bus;

a host computer to execute test flows; and

instrument modules, an instrument module comprising:

resources; and

a processing device;

wherein resources operated on by a test flow define a domain;

wherein the host computer is configured to output commands including a sync command in the test flow to the instrument modules, the sync command for causing the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules in the domain are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated; and

wherein the processing device is configured to resume executing commands based on the information.

2. The system of claim 1, wherein the information is distributed after all instrument modules in the domain have encountered a sync command.

3. The system of claim 1, wherein the host computer is programmed to send the commands to the instrument modules via a communication bus that is different from the computer bus.

4. The system of claim 1, wherein aggregating the status and distributing the information are performed independent of the host computer.

5. The system of claim 1, wherein at least some of the commands instruct resources in the domain to perform operations.

6. The system of claim 1, wherein the instrument module comprises an endpoint device to provide status to the computer bus;

wherein the endpoint device comprises a contributing endpoint device; and

wherein the contributing endpoint device is configured to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

7. The system of claim 1, wherein the instrument module comprises an endpoint device; and

wherein the endpoint device comprises a non-contributing endpoint device to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

8. The system of claim 1, wherein the host computer is programmed to execute a test program that includes multiple, separate instruction flows, the multiple, separate instruction flows including the test flow.

9. The system of claim 8, wherein the instrument module comprises an endpoint device; and

wherein the endpoint device is configured to subscribe to one or more of the multiple, separate flows.

10. The system of claim 1, wherein the instrument module comprises an endpoint device; and

wherein the endpoint device is configured to generate a signal to provide to resources in the domain.

11. The system of claim 10, wherein the signal is to trigger the resource to perform an action for which the resource has been previously armed.

12. The system of claim 10, wherein an offset may be added to the signal to control signal timing relative to receipt of the information.

13. The system of claim 1, wherein the instrument module comprises an endpoint device; and

wherein the endpoint device comprises a transmitter to implement output to the computer bus, and a receiver to implement receiving from the computer bus.

14. The system of claim 1, wherein the status comprises a pass or fail status of a test performed by the processor.

15. The system of claim 1, wherein the status comprises bits that are encoded in time-division-multiple-access fashion onto the computer bus using a periodic frame comprised of multiple bits.

16. The system of claim 15, wherein the periodic frame is characterized by one or more of headers, trailers, cyclic redundancy checks, or 8b/10b encoding.

17. The system of claim 1, wherein at least some of the bits of the information represent a system time alignment signal to set system clock counters on the instruments to at least one of a specified value or a specified time that is in a payload on the bus.

18. The system of claim 1, wherein the computer bus comprises at least one of a wired-OR bus; point-to-point connections and logic gates; non-contact, wireless or optical signaling; or a combination of one or more of: a wired-OR bus; point-to-point connections and logic gates; non-contact, and wireless or optical signaling.

19. The system of claim 1, wherein the information is received over the computer bus.

20. The system of claim 1, wherein the information is received over a communication bus that is different than the computer bus.

21. The system of claim 1, wherein the sync command in the test flow immediately precedes, in the test flow, a command requiring action or measurement vis-à-vis a device under test by the test flow.

22. The system of claim 1, wherein at least part of the test flow is controllable not to be synchronized.

23. A system comprising:

a computer bus;

instrument modules, an instrument module comprising:

resources; and

a processing device to execute commands from a queue;

wherein the processing device is configured, in response to encountering at least one sync command in the queue, to cause the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated; and

wherein the processing device is configured to resume executing commands based on the information.

24. The test system of claim 23, further comprising:

a host computer; and

a communication bus;

wherein the host computer is configured to output the commands to the instrument module via the communication bus.

25. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller.

26. The test system of claim 25, wherein the synchronization mechanism is configured to:

enable each processing unit to transmit status data indicating whether the processing unit has completed a portion of the test program;

to receive and to aggregate status data across all processing units; and

to transmit one or more aggregated status bits back to all processing units.

27. The test system of claim 26, wherein the processing unit is configured to perform operations comprising: when the processing unit has completed a portion of the test program, the processing unit indicates, on a synchronization bus, that the processing unit has completed the portion of the test program and, before proceeding to a next portion of the test program, the processing unit receives the one or more aggregated status bits indicating that all other processing units in the test system have completed portions of the test program.

28. The test system of claim 26, wherein the synchronization mechanism has a defined timing relative to system clocks so that multiple instruments can receive the one or more aggregated status bits and be triggered to perform an action, a measurement, or both an action and a measurement with predictable and repeatable timing alignment among multiple instruments.

29. The test system of claim 26, wherein the synchronization mechanism is configured to support status data comprising multiple status bits that are transmittable by each processing unit, and that can be aggregated to produce the one or more

aggregated status bits, the one or more aggregated status bits being transmitted to all of the processing units.

30. The test system of claim 26, wherein the one or more aggregated status bits are usable to synchronize all instruments in the test system to synchronize a sequence of actions, a sequence of measurements, or a sequence of actions and measurements.

31. The test system of claim 26, wherein the status data comprises at least one bit to transmit pass or fail status of a test program.

32. The test system of claim 26, wherein the status data comprises one or more status bits that are encoded in time-division-multiple-access fashion onto a serial data bus using a periodic frame.

33. The test system of claim 32, wherein the periodic frame is characterized by one or more of headers, trailers, cyclic redundancy checks, or 8b/10b encoding.

34. The test system of claim 32, wherein the periodic frame is configurable to transmit information other than the one or more status bits.

35. The test system of claim 26, wherein one or more bit transmitted to the processing units represent a system time alignment signal to set system clock counters on the instruments to a specified value.

36. The test system of claim 26, wherein the one or more aggregated status bits comprises a single status bit to synchronize all instruments in the test system to synchronize a sequence of actions, a sequence of measurements, or a sequence of actions and measurements.

37. The test system of claim 26, wherein the synchronization mechanism comprises at least one of a wired-OR bus; point-to-point connections and logic gates;

non-contact, wireless or optical signaling; or a combination of one or more of: a wired-OR bus; point-to-point connections and logic gates; non-contact, and wireless or optical signaling.

38. The test system of claim 26, wherein at least part of the synchronization mechanism is controllable to be disabled either automatically or manually.

39. The test system of claim 26, wherein at least part of the synchronization mechanism is controllable to operate on only part of the test program.

1. A system comprising:

a computer bus;

a host computer to execute test flows; and

instrument modules, an instrument module comprising:

resources; and

a processing device;

wherein resources operated on by a test flow define a domain;

wherein the host computer is configured to output commands including a sync command in the test flow to the instrument modules, the sync command for causing the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules in the domain are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information;

wherein the instrument module comprises an endpoint device to provide status to the computer bus;

wherein the endpoint device comprises a contributing endpoint device; and

wherein the contributing endpoint device is configured to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

2. A system comprising:

a computer bus;

a host computer to execute test flows; and

instrument modules, an instrument module comprising:

resources; and

a processing device;

wherein resources operated on by a test flow define a domain;

wherein the host computer is configured to output commands including a sync command in the test flow to the instrument modules, the sync command for causing the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules in the domain are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information;

wherein the instrument module comprises an endpoint device; and

wherein the endpoint device comprises a non-contributing endpoint device to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

3. The system of claim 1 or 2, wherein the host computer is programmed to output the commands to the instrument modules via a communication bus that is different from the computer bus.

4. The system of claim 1 or 2, wherein aggregating the status and distributing the information are performed independent of the host computer.

5. The system of claim 1 or 2, wherein at least some of the commands instruct resources in the domain to perform operations.

6. The system of claim 1 or 2, wherein the signal is to trigger a resource to perform an action for which the resource has been previously armed.

7. The system of claim 1, wherein an offset may be added to the signal to control signal timing relative to receipt of the information.

8. The system of claim 1 or 2, wherein the endpoint device comprises a transmitter to implement output to the computer bus, and a receiver to implement receiving from the computer bus.

9. The system of claim 1 or 2, further comprising a processor to perform a test; wherein the status comprises a pass or fail status of the test performed by the processor.

10. The system of claim 1 or 2, wherein the computer bus comprises at least one of a wired-OR bus; point-to-point connections and logic gates; non-contact, wireless or optical signaling; or a combination of one or more of: a wired-OR bus; point-to-point connections and logic gates; non-contact, and wireless or optical signaling.

11. The system of claim 1 or 2, wherein the information is received over the computer bus.

12. The system of claim 1 or 2, wherein the information is received over a communication bus that is different than the computer bus.

13. The system of claim 1 or 2, wherein the sync command in the test flow immediately precedes, in the test flow, a command requiring action or measurement vis-a-vis a device under test by the test flow.

14. The system of claim 1 or 2, wherein at least part of the test flow is controllable not to be synchronized.

15. The system of claim 1 or 2, wherein the information is distributed after all instrument modules in the domain have encountered a sync command.

16. A system comprising:
a computer bus;
a host computer to execute test flows; and
instrument modules, an instrument module comprising:
resources; and
a processing device;
wherein resources operated on by a test flow define a domain;
wherein the host computer is configured to output commands including a sync command in the test flow to the instrument modules, the sync command for causing the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules in the domain are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information;

wherein the host computer is programmed to execute a test program that includes multiple, separate instruction flows, the multiple, separate instruction flows including the test flow;

wherein the instrument module comprises an endpoint device; and

wherein the endpoint device is configured to subscribe to one or more of the multiple, separate instruction flows.

17. A system comprising:

a computer bus;

a host computer to execute test flows; and

instrument modules, an instrument module comprising:

resources; and

a processing device;

wherein resources operated on by a test flow define a domain;

wherein the host computer is configured to output commands including a sync command in the test flow to the instrument modules, the sync command for causing the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules in the domain are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information; and

wherein the status comprises bits that are encoded in time-division-multiple-access fashion onto the computer bus using a periodic frame comprised of multiple bits.

18. The system of claim 17, wherein the periodic frame is characterized by one or more of headers, trailers, cyclic redundancy checks, or 8b/10b encoding.

19. A system comprising:

a computer bus;

a host computer to execute test flows; and

instrument modules, an instrument module comprising:

resources; and

a processing device;

wherein resources operated on by a test flow define a domain;

wherein the host computer is configured to output commands including a sync command in the test flow to the instrument modules, the sync command for causing the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules in the domain are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information; and

wherein at least some bits of the information represent a system time alignment signal to set system clock counters on the instrument modules to at least one of a specified value or a specified time that is in a payload on the computer bus.

20. A system comprising:

a computer bus;

instrument modules, an instrument module comprising:

resources; and

a processing device to execute commands from a queue;

wherein the processing device is configured, in response to encountering at least one sync command in the queue, to cause the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information;

wherein the instrument module comprises an endpoint device to provide status to the computer bus;

wherein the endpoint device comprises a contributing endpoint device; and

wherein the contributing endpoint device is configured to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

21. The system of claim 20, further comprising:

a host computer; and

a communication bus;

wherein the host computer is configured to output the commands to the instrument module via the communication bus.

22. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller;

wherein the synchronization mechanism is configured to:

enable each processing unit to transmit status data in response to a synch command, the status data indicating whether the processing unit has completed a portion of the test program;

receive and to aggregate status data across all processing units; and

transmit one or more aggregated status bits back to all processing units; and

wherein a processing unit among the at least some processing units is configured to resume execution based on the aggregated status bits.

23. The test system of claim 22, wherein the one or more aggregated status bits are usable to synchronize all instruments in the test system to synchronize a sequence

of actions, a sequence of measurements, or a sequence of actions and measurements.

24. The test system of claim 22, wherein the status data comprises at least one bit to transmit pass or fail status of a test program.

25. The test system of claim 22, wherein the synchronization mechanism comprises at least one of a wired-OR bus; point-to-point connections and logic gates; non-contact, wireless or optical signaling; or a combination of one or more of: a wired-OR bus; point-to-point connections and logic gates; non-contact, and wireless or optical signaling.

26. The test system of claim 22, wherein at least part of the synchronization mechanism is controllable to be disabled either automatically or manually.

27. The test system of claim 22, wherein at least part of the synchronization mechanism is controllable to operate on only part of the test program.

28. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller;

wherein the synchronization mechanism is configured to:

enable each processing unit to transmit status data indicating whether the processing unit has completed a portion of the test program;

receive and to aggregate status data across all processing units; and

transmit one or more aggregated status bits back to all processing units; and

wherein a processing unit is configured to perform operations comprising: when the processing unit has completed a portion of the test program, the processing unit indicates, on a synchronization bus, that the processing unit has

completed the portion of the test program and, before proceeding to a next portion of the test program, the processing unit receives the one or more aggregated status bits indicating that all other processing units in the test system have completed portions of the test program.

29. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller;

wherein the synchronization mechanism is configured to:

enable each processing unit to transmit status data indicating whether the processing unit has completed a portion of the test program;

receive and to aggregate status data across all processing units; and

transmit one or more aggregated status bits back to all processing units; and

wherein the synchronization mechanism has a defined timing relative to system clocks so that multiple instruments can receive the one or more aggregated status bits and be triggered to perform an action, a measurement, or both an action and a measurement with predictable and repeatable timing alignment among multiple instruments.

30. The test system of claim 29, wherein the synchronization mechanism is configured to support status data comprising multiple status bits that are transmittable by each processing unit, and that can be aggregated to produce the one or more aggregated status bits, the one or more aggregated status bits being transmitted to all of the processing units.

31. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller;

wherein the synchronization mechanism is configured to:

enable each processing unit to transmit status data indicating whether the processing unit has completed a portion of the test program;

receive and to aggregate status data across all processing units; and

transmit one or more aggregated status bits back to all processing units; and

wherein the status data comprises one or more status bits that are encoded in time-division-multiple-access fashion onto a serial data bus using a periodic frame.

32. The test system of claim 31, wherein the periodic frame is characterized by one or more of headers, trailers, cyclic redundancy checks, or 8b/10b encoding.

33. The test system of claim 31, wherein the periodic frame is configurable to transmit information other than the one or more status bits.

34. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller;

wherein the synchronization mechanism is configured to:

enable each processing unit to transmit status data indicating whether the processing unit has completed a portion of the test program;

receive and to aggregate status data across all processing units; and

transmit one or more aggregated status bits back to all processing units; and

wherein at least some of the one or more aggregated status bits transmitted to the processing units represent a system time alignment signal to set system clock counters on the instruments to a specified value.

35. The test system of claim 34, wherein the one or more aggregated status bits comprises a single status bit to synchronize all instruments in the test system to synchronize a sequence of actions, a sequence of measurements, or a sequence of actions and measurements.

36. A system comprising:

a computer bus;

instrument modules, an instrument module comprising:

resources; and

a processing device to execute commands from a queue;

wherein the processing device is configured, in response to encountering at least one sync command in the queue, to cause the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information;

wherein the instrument module comprises an endpoint device; and

wherein the endpoint device comprises a non-contributing endpoint device to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

37. A system comprising:

a computer bus;

instrument modules, an instrument module comprising:

resources; and

a processing device to execute commands from a queue;

wherein the processing device is configured, in response to encountering at least one sync command in the queue, to cause the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information; and

wherein the status comprises bits that are encoded in time-division-multiple-access fashion onto the computer bus using a periodic frame comprised of multiple bits.

38. A system comprising:

a computer bus;

instrument modules, an instrument module comprising:

resources; and

a processing device to execute commands from a queue;

wherein the processing device is configured, in response to encountering at least one sync command in the queue, to cause the instrument module to provide a status to the computer bus and to pause the processing device;

wherein statuses from the instrument modules are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated;

wherein the processing device is configured to resume executing commands based on the information; and

wherein at least some bits of the information represent a system time alignment signal to set system clock counters on the instrument modules to at least one of a specified value or a specified time that is in a payload on the computer bus.