METHOD TO CONTROL SOURCE/DRAIN STRESSOR PROFILES FOR STRESS ENGINEERING

Abstract

An example embodiment of a strained channel transistor structure comprises the following: a strained channel region comprising a first semiconductor material with a first natural lattice constant; a gate dielectric layer overlying the strained channel region; a gate electrode overlying the gate dielectric layer; and a source region and drain region oppositely adjacent to the strained channel region, one or both of the source region and drain region are comprised of a stressor region comprised of a second semiconductor material with a second natural lattice constant different from the first natural lattice constant; the stressor region has a graded concentration of a dopant impurity and/or of a stress inducing molecule. Another example embodiment is a process to form the graded impurity or stress inducing molecule stressor embedded S/D region, whereby the location/profile of the S/D stressor is not defined by the recess depth/profile.

Figure 5