A METHOD FOR A SHORT CHANNEL CMOS TRANSISTOR WITH SMALL OVERLAY CAPACITANCE USING IN-SITU DOPED SPACERS WITH A LOW DIELECTRIC CONSTANT

Abstract

The method for a transistor using a replacement gate process that has a doped low-K dielectric spacer that lowers the junction capacitance. A dummy gate is formed over a substrate. Ions are implanted into the substrate using the dummy gate as an implant mask to form source and drain regions. A masking layer is formed on the substrate over the source and drain regions. We remove the dummy gate. Doped low k spacers are formed on the sidewalls of the masking layer. The doped spacers are heated to diffuse dopant into the substrate to form lightly doped drain (LDD regions). We form a high k gate dielectric layer over the masking layer. A gate layer is formed over the high K dielectric layer. The gate layer is chemical-mechanical polished (CMP) to form a gate over the high k dielectric layer and to remove the gate layer over the masking layer.

Fig. 7