ENHANCED PASSIVATION PROCESS TO PROTECT SILICON PRIOR TO HIGH DOSE IMPLANT STRIP

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This applications claims benefit under 34 USC §119(e) to U.S. Provisional Patent Application No. 61/285,918, filed December 11, 2009, which is incorporated by reference herein.

FIELD OF INVENTION

[002] The present invention pertains to methods and apparatuses to remove or strip photoresist material and removing related residues from a work piece surface. In certain embodiments, this application relates to methods and apparatus for stripping resist after ion implant or plasma assisting doping implant (low dose or high-dose implanted resist).

BACKGROUND

[003] Photoresist is a light sensitive material used in certain fabrication processes to form a patterned coating on a work piece, e.g., a semiconductor wafer, during processing. After exposing the photoresist coated surface to a pattern of high energy radiation, a portion of the photoresist is removed to reveal the surface below, leaving the rest of the surface protected. Semiconductor processes such as etching, depositing, and ion implanting are performed on the uncovered surface and the remaining photoresist. After performing one or more semiconductor processes, the remaining photoresist is removed in a strip operation.

SUMMARY OF THE INVENTION

[004] Improved methods and apparatus for stripping photoresist and removing ion implant related residues from a work piece surface are provided. According to various embodiments, the workpiece is exposed to a passivation plasma, allowed to cool for a period of time, and then exposed to an oxygen-based or hydrogen-based plasma to remove the photoresist and ion implant related residues. Aspects of the invention include reducing silicon loss, leaving little or no residue while maintaining an acceptable strip rate. In

certain embodiments, methods and apparatus remove photoresist material after high-dose ion implantation processes.

[005] One aspect of the invention relates to a method of removing material from a work piece surface in a reaction chamber, and involves exposing the work piece to a plasma generated from forming gas; after exposing the work piece to the forming gas plasma, allowing the wafer to sit in a non-plasma environment for a time period of at least 30 seconds; and after allowing the wafer to sit, exposing the wafer to an oxygen- or hydrogen-based plasma to remove the material.

[006] According to various embodiments, the work piece is allowed to sit for at least about 100 seconds, at least about 150 seconds, at least about 200 seconds, or at least about 220 seconds.

[007] In certain embodiments, at least one of the oxygen- or hydrogen-based plasma includes fluorine species; in other embodiments, neither do. The material removed from the work piece surface may be a high-dose implanted resist. In certain embodiments, the forming gas plasma is remotely generated. In certain embodiments, a protective film forms on exposed silicon portions of the workpiece after exposure to the forming gas plasma. The protective film may be a Si_xN_y film.

[008] Another aspect of the invention relates to an apparatus for removing material from a work piece surface including a reaction chamber including a plasma source, a showerhead positioned downstream of the plasma source, and a work piece support downstream of the showerhead, said work piece support comprising a pedestal and temperature-controlling mechanism to control a temperature of a work piece supported on the work piece support; and a controller for executing a set of instructions, said set of instruction including instructions for exposing the work piece to a plasma generated from forming gas; after exposing the work piece to the forming gas plasma, allowing the wafer to sit in a non-plasma environment for a time period of at least 30 seconds; and after allowing the wafer to sit, exposing the wafer to an oxygen- or hydrogen-based plasma to remove the material.

[009] These and other features and advantages of the present invention will be described in more detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figures 1A – 1D depict various stages of semiconductor device fabrication before and after ion implantation and stripping operations.

[0011] Figure 2 is a process flow diagram illustrating operations in accordance with certain embodiments of the present invention.

[0012] Figure 3 is a graph showing silicon loss as a function of post-passivation wait time.

[0013] Figure 4 is a schematic illustration showing an apparatus suitable for implementing aspects of the present invention.

[0014] Figure 5 shows a multi-station sequential architecture suitable for implementing aspects of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

INTRODUCTION

[0015] In the following detailed description of the present invention, numerous specific embodiments are set forth in order to provide a thorough understanding of the invention. However, as will be apparent to those skilled in the art, the present invention may be practiced without these specific details or by using alternate elements or processes. In other instances well-known processes, procedures and components have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

[0016] In this application, the terms "work piece", "semiconductor wafer", "wafer" and "partially fabricated integrated circuit" will be used interchangeably. One skilled in the art would understand that the term "partially fabricated integrated circuit" can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. The following detailed description assumes the invention is implemented on a wafer.

However, the invention is not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of this invention include various articles such as displays, printed circuit boards, and the like.

[0017] Photoresist is a light sensitive material used in certain fabrication processes to form a patterned coating on a work piece, e.g., a semiconductor wafer, during processing. After exposing the photoresist coated surface to a pattern of high energy radiation, a portion of the photoresist is removed to reveal the surface below, leaving the rest of the surface protected. Semiconductor processes such as etching, depositing, and ion implanting are performed on the uncovered surface and the remaining photoresist. After performing one or more semiconductor processes, the remaining photoresist is removed in a strip operation.

[0018] During ion implantation, dopant ions, e.g., ions of boron, boron difluoride, indium, gallium, thallium, phosphorous, arsenic, antimony, bismuth, or germanium, are accelerated toward a work piece target. The ions implant in exposed regions of the work piece as well as in the remaining photoresist surface. The process may form well regions (source/drain) and lightly doped drain (LDD) and doubled diffused drain (DDD) regions. The ion implant impregnates the resist with the implant species and depletes the surface of hydrogen. The outer layer or crust of the resist forms a carbonized layer that may be much denser than the underlying bulk resist layer. These two layers have different thermal expansion rates and react to stripping processes at different rates.

[0019] The difference between the outer layer and bulk layer is quite pronounced in post high-dose ion implant resist. In high-dose implantation, the ion dose may be greater than 1 x 1015 ions/cm2 and the energy may be from 10Kev to greater than 100 keV. Traditional high dose implantation strip (HDIS) processes employ oxygen chemistries where monatomic oxygen plasma is formed away from the process chamber and then directed at the work piece surface. The reactive oxygen combines with the photoresist to form gaseous by-products which is removed with a vacuum pump. For HDIS, additional gases are needed to remove the implanted dopants with oxygen.

[0020] Primary HDIS considerations include strip rate, amount of residue, and film loss of the exposed and underlying film layer. Residues are commonly found on the substrate surface after HDIS and stripping. They may result from sputtering during the high-energy implant, incomplete removal of crust, and/or oxidation of implant atoms in the resist. After stripping, the surface should be residue free or substantially residue free to ensure high yield and eliminate the need for additional residue removal processing. Residues may be removed by overstripping, i.e., a continuation of the strip process past the point nominally required to remove all photoresist. Unfortunately, in conventional HDIS operations, overstripping sometimes removes some of the underlying functional device structure. At the device layer, even very little silicon loss from the transistor source/drain regions may adversely affect device performance and yield, especially for ultra shallow junction devices fabricated at the <32nm design rule or below.

[0021] As mentioned previously, the methods and apparatus of the invention may be used to efficiently and effectively to remove photoresist materials after high-dose ion implantation. The invention is not limited to high-dose implant strip (HDIS). The invention is also not limited to any particular category of dopants implanted. For instance, described methods and apparatus may be effectively used with stripping after medium or low dose implant. Although specific dopant ions such as boron, arsenic, and phosphorous are discussed, the described methods and apparatus may be effectively used to strip resist impregnated with other dopants, such as nitrogen, oxygen, carbon, germanium, and aluminum.

[0022] The methods and apparatus of the present invention use passivation plasmas that are produced from forming gas. The methods and apparatus also use photoresist stripping and ion removal plasmas that are generated from plasmas gases that contain oxygen and/or hydrogen. In certain embodiments, the gases also contain a fluorine-containing gas, a weak oxidizing agent and one or more additional components. One skilled in the art will recognize that the actual species present in the plasma may be a mixture of different ions, radicals, and molecules derived from the particular gases used to generate the plasmas described herein. For example, it is noted that other species may be present in the reaction chamber, such as small hydrocarbons, carbon dioxide, water vapor and other volatile components as the plasma reacts with and breaks down the organic photoresist and other

residues. One of skill in the art will also recognize that the initial gas/gases introduced into the plasma is/are often different from the gas/gases that exist in the plasma as well as the gas/gases contact the work piece surface during strip.

[0023] Figure 1A to 1D depicts various stages of semiconductor fabrication before and after ion implantation and stripping operations. Figure 1A shows a semiconductor substrate 101 coated with photoresist material 103. The substrate 101 may include one or more layers of deposited film, e.g., oxide film, silicide contact, and/or polysilicon film, or may be a bare silicon substrate, including for example a silicon-on-insulator type substrate. Initially, the photoresist material coats the entire substrate surface. The photoresist is then exposed to patterned radiation generated through a mask and developed to remove a portion of the material, e.g., the opening 104 shown in Figure 1A between the remaining photoresist materials 103.

[0024] The substrate is then exposed to an ion implant process. During ion implant, the surface of the work piece or wafer is implanted with dopant ions. The process may be, for example, a plasma-immersion ion implantation (PIII) or ion beam implantation. The ions bombard the substrate surface, including the exposed silicon layer 101 and the photoresist 103. With high energy ion implantation, small amounts of the underlying material 107 may be sputtered to the photoresist sidewalls. See Figure 1B. This material may include some of the implant species, other material in the plasma or ion beam, and by-products of the implantation. They include silicon, aluminum, carbon, fluorine, titanium, other contact materials such as cobalt, and oxygen in both elemental and compound form. The actual species depend on the composition of the substrate before ion implant, the photoresist, and the implanted species.

[0025] At the exposed silicon layer 101, a doped region 109 is created. The ion energy or intensity of the bombardment determines the depth or thickness of the doped region. The density of the ion flux determines the extent of doping.

[0026] The ions also impregnate the photoresist surface creating a crust layer 105. The crust layer 105 may be carbonized and highly cross-linked polymer chains. The crust is usually depleted of hydrogen and impregnated with the implant species. The crust layer

105 is denser than the bulk resist layer 103. The relative density depends on the ion flux while the thickness of the crust layer depends on the ion energy.

[0027] This crust layer 105 is harder to strip than the bulk photoresist 103 below. Removal rates of the crust layer may be 50% or 75% slower than the underlying bulk Enhanced Passivation process to protect Silicon prior to High Dose Implant Enhanced Passivation process to protect Silicon prior to High Dose Implant photoresist. The bulk photoresist contains relatively high levels of chemically bonded nitrogen and some of its original casting solvent. At elevated wafer temperature, e.g., above 150 to above 200oC, the bulk resist can outgas and expand relative to the crust layer. The entire photoresist can then "pop" as the underlying bulk photoresist builds up pressure under the crust. Photoresist popping is a source of particles and process defects because the residues are especially hard to clean from the wafer surface and chamber internal parts. With high-dose ion implantation, the density difference between the crust and underlying bulk photoresist layer is even higher. The crust may also be thicker.

[0028] Figure 1C shows the substrate after a strip that fails to completely remove the photoresist 103 and the sidewall sputter residue 107. The sidewall sputter residue 107 may include particles that do not form a volatile compound under conventional strip chemistries. These particles may remain after a conventional strip operation. The residue may also include oxides of implanted species formed with the reactive oxygen used in oxygen-based strip chemistries, such as boron oxide and arsenic oxide. Portions of the crust 105 may also remain on the substrate. Crust sidewalls and corners at the bottom of photoresist vias may be hard to strip because of geometries. These residue particles may be removed by overstripping in some cases, using fluorinated chemistry, or wet cleaning the wafer.

[0029] Silicon loss is a function of resist thickness, crust thickness, and percent overstrip. Longer and more aggressive stripping to remove thicker resist can also remove more silicon. For resist with thicker crust, the difference between the crust layer and bulk resist layer is even more pronounced. The thicker crust sidewalls and corners are even harder to strip. Thus, strip processes designed to remove thick crust also tends to remove more silicon. Overstrip may be used to address resist uniformity and geometries in addition to

residue removal. Overstrip is a continuation of the strip process past the point nominally required to remove all photoresist. If the photoresist is totally removed in some areas of the wafer but not others, continuation of the strip process would cause additional material, typically silicon and silicon oxide, to be removed from areas that are already stripped.

[0030] Figure 1D shows the substrate after all residue has been removed. According to various embodiments, the residue is removed without additional silicon loss or oxidation and with minimum delay. In certain embodiments, the strip process leaves no residue and thus reduces the number of process steps.

[0031] Provided herein are methods to reduce silicon loss for high dose implant strip (HDIS) processes, although as noted above, the methods may be effectively used with stripping after medium or low dose implant or other photoresist stripping processes. The methods described herein provide a passivation layer to prevent silicon loss prior to stripping and are not limited to a particular stripping chemistry.

[0032] Figure 2 is a process flow diagram 200 illustrating operations in a method according to certain embodiments. First, a wafer having photoresist and implant residue material is provided in an operation 201. The wafer may be provided to a chamber capable of containing a plasma. Although not depicted, the wafer is optionally pre-heated (prior to, during, or after operation 201) to a set temperature low enough to prevent popping, but high enough to provide energy for formation of a passivation layer and an acceptable etch rate in further operations. The wafer is then exposed to a plasma generated from forming gas an operation 203. The forming gas comprises hydrogen and an inert dilutant, such as, for example, nitrogen, helium, or the like, or a combination thereof. In an exemplary embodiment of the invention, the forming gas is about 0.5 to about 10 molar percent (%) hydrogen. In a particular embodiment of the invention, the forming gas is about 3 to about 6 % hydrogen, e.g., 4% hydrogen. In certain embodiments, pure nitrogen gas with essentially no hydrogen is used. It has been found that pure nitrogen can provide as similar passivation effect as forming gas.

[0033] The wafer is exposed to the forming gas plasma for a period of time, e.g., on the order of about 10 to 90 seconds, e.g., about 20 to 40 seconds. In many embodiments, the

plasma is a remotely-generated plasma, though it may be an in-situ plasma. In certain embodiments, the plasma is generated from a gas consisting essentially of forming gas. In other embodiments, other species may be added. In certain embodiments, substantially no oxygen or fluorine is present in the gases inlet to the plasma generator.

[0034] Then in an operation 205, the plasma is extinguished and the wafer sits for a period of time. In certain embodiments, the wafer is allowed to cool during this operation, for example to about 35 C. Without being bound by a particular theory, it is believed that a protective surface forms on the exposed silicon to slow prevent oxidation or etching from subsequent oxygen-based or hydrogen-based stripping chemistries that may include fluorine species. The protective surface may be a SixNy film.

[0035] It was unexpectedly found that the wait time between operation 203 and the subsequent stripping operations is critical to reducing silicon loss. Figure 3 is a graph showing silicon loss (Angstroms) as a function of wait time (seconds) between exposure to the forming gas plasma, and a subsequent stripping process using a hydrogen-based chemistry containing fluorine. The silicon loss decreases sharply as the wait time increases, eventually leveling off around 220 seconds. According to various embodiments, the wait time is at least about 30 seconds, at least about 60 seconds, at least about 100 seconds, at least about 120 seconds, at least about 140 seconds, at least about 160 seconds, at least about 180 seconds, at least about 200 seconds, at least about 220 seconds, at least about 240, at least about 260 seconds, or at least about 280 seconds. The effect observed in Figure 3 is unexpected as the chemical kinetics of the reaction to form a SixNy film would be expected to be much faster.

[0036] Once the waiting period is finished, a stripping process is performed in an operation 207. The stripping process may use one or more oxygen-based or hydrogen-based plasmas. In certain embodiments, the stripping chemistry additionally contains fluorine species in one or more operations. Fluorine compounds that may be fed to the plasma generator to generate such species include nitrogen trifluoride (NF3), sulfur hexafluoride (SF6), hexafluoroethane (C2F6), tetrafluoromethane (CF4), trifluoromethane (CHF3), difluoromethane (CH2F2), octofluoropropane (C3F8), octofluorocyclobutane

(C4F8), octofluoro[1-]butane (C4F8), octofluoro[2-]butane (C4F8), octofluoroisobutylene (C4F8), fluorine (F2), and the like.

[0037] While the methods described herein are not limited to any particular strip chemistries, examples plasmas to remove photoresist and HDI residue include plasmas generated from the following:

O2/NF3

O2/CF4

O2/N2

H2/CO2/NF3

H2/CO2/CF4

H2/CO2/NF3/CF4

H2/CO2

H2/N2

[0038] In many embodiments, multiple operations having different chemistries are performed to fully remove the photoresist and residue. In certain embodiments, forming gas is added to one or more of these HDI strip operations. For example, in certain embodiments, forming gas is added to all non-fluorine containing plasma operations. It has been found that using forming gas or pure nitrogen in the fluorine-containing stations can adversely affect silicon loss. Without being bound by a particular theory, it is believed that this may be due to nitrogen in the forming gas facilitating the disassociation of the NF3, releasing more F- ions. Typically, no significant wait time is imposed after these operations, though in certain embodiments, it may be. Examples are:

O2/FG with forming gas supplying about 14-25% by volume;

H2/CO2/FG with forming gas supplying about 40-60% by volume;

[0039] It should be noted that the passivation process described in operations 203 and 205 may be performed or repeated at other stages in the process, e.g., between one or more strip operations. In certain embodiments, only operation 203 is inserted between these operations.

Plasma Generation

[0040] Various types of plasma sources may be used in accordance with the invention, including RF, DC, and microwave based plasma sources. In a preferred embodiment, a downstream RF plasma source is used. Typically, the RF plasma power for a 300 mm wafer ranges between about 300 Watts to about 10 Kilowatts. In some embodiments, the RF plasma power is between about 2000 Watts and 5000 Watts, e.g., 3500 W.

Showerhead Assembly

[0041] According to various embodiments of the present invention the plasma gas is distributed to the work surface via a showerhead assembly. The showerhead assembly may be grounded or have an applied voltage to attract some charge species while not affecting the flow of neutral species to the wafer, e.g., 0-1000 watt bias. Many of the electrically charged species in the plasma recombine at the showerhead. The assembly includes the showerhead itself which may be a metal plate having holes to direct the plasma and inert gas mixture into the reaction chamber. The showerhead redistributes the active hydrogen from the plasma source over a larger area, allowing a smaller plasma source to be used. The number and arrangement of the showerhead holes may be set to optimize strip rate and strip rate uniformity. If the plasma source is centrally located over the wafer, the showerhead holes are preferably smaller and fewer in the center of the showerhead in order to push the active gases toward the outer regions. The showerhead may have at least 100 holes. Suitable showerhead include the Gamma xPR showerhead or the GxT drop-in showerhead available from Novellus Systems, Inc. of San Jose, CA. In embodiments in which there is no showerhead assembly, the plasma enters the process chamber directly.

Process Chamber

[0042] The process chamber may be any suitable reaction chamber for the strip operation being performed. It may be one chamber of a multi-chambered apparatus or it may simply be a single chamber apparatus. The chamber may also include multiple stations where different wafers are processed simultaneously. The process chamber may be the same chamber where the implant, etch, or other resist-mediated process takes place. In other embodiments, a separate chamber is reserved for the strip. Process chamber pressure may range from about 600 mTorr to 2 Torr. In certain embodiments, the pressure ranges from about 0.9 Torr to 1.5 Torr.

[0043] The process chamber includes one or more processing stations on which strip operations are performed. In certain embodiments, the one or more processing stations includes a preheat station, at least one strip station, and an over-ash station. The wafer support is configured to support the wafer during processing. The wafer support may also transfer heat to and from the wafer during processing to adjust the wafer temperature as necessary. In certain embodiments, the wafer is supported on a plurality of minimum contacts and does not physically contact the wafer support surface plane. A spindle picks up the wafer and transfers the wafer from one station to another.

[0044] Figure 4 is a schematic illustration showing aspects of a downstream plasma apparatus 400 suitable for practicing the present invention on wafers. This apparatus may be used both for passivation and strip operations. Apparatus 400 has a plasma producing portion 411 and an exposure chamber 401 separated by a showerhead assembly 417. Inside exposure chamber 401, a wafer 403 rests on a platen (or stage) 405. Platen 405 is fitted with a heating/cooling element. In some embodiments, platen 405 is also configured for applying a bias to wafer 403. Low pressure is attained in exposure chamber 401 via vacuum pump via conduit 407. Sources of gaseous hydrogen (with or without dilution/carrier gas) and carbon dioxide (or other weak oxidizing agent) provide a flow of gas via inlet 409 into plasma producing portion 411 of the apparatus. Plasma producing portion 411 is surrounded in part by induction coils 413, which are in turn connected to a power source 415. During operation, gas mixtures are introduced into plasma producing portion 411, induction coils 413 are energized and a plasma is generated in plasma

producing portion 411. Showerhead assembly 417 may have an applied voltage or be grounded directs the flow of species into exposure chamber 401. As mentioned, wafer 403 may be temperature controlled and/or a RF bias may be applied. Various configurations and geometries of the plasma source 411 and induction coils 413 may be used. For example, induction coils 413 may loop around the plasma source 411 in an interlaced pattern. In another example, the plasma source 411 may be shaped as a dome instead of a cylinder. A controller 450 may be connected to components of the process chamber, and control process gas composition, pressure, temperature and wafer indexing of the stripping operations. Machine-readable media may be coupled to the controller and contain instructions for controlling process conditions for these operations.

[0045] Suitable plasma chambers and systems include the Gamma 2100, 2130 I2CP (Interlaced Inductively Coupled Plasma), G400, and GxT offered by Novellus Systems, Inc. of San Jose, CA. Other systems include the Fusion line from Axcelis Technologies Inc. of Rockville, Maryland, TERA21 from PSK Tech Inc. in Korea, and the Aspen from Mattson Technology Inc. in Fremont, CA. Additionally, various strip chambers may be configured onto cluster tools. For example, a strip chamber may be added to a Centura cluster tool available from Applied Materials of Santa Clara, CA.

Work piece

[0046] In preferred embodiments, the work piece used in accordance with the methods and apparatus of the invention is a semiconductor wafer. Any size wafer may be used. Most modern wafer fabrication facilities use either 200 mm or 300 mm wafers. As disclosed above, the process and apparatus disclosed herein strips photoresist after a processing operation such as etching, ion implant, or deposition. The present invention is suitable for wafers having very small features or critical dimensions, e.g., sub 100 nm, at 65 nm, or at or less than 45 nm. The low silicon loss feature of the HDIS as disclosed is particularly suitable for very shallow junctions of advanced logic devices. The present invention is also specifically suitable for wafers undergoing front end of the line (FEOL) ion implantation, especially high-dose ion implantation.

[0047] The plasma-activated species reacts with the photoresist and sputter residue on the wafer. At the wafer, the reactive gas may include a number of plasma activated species,

radicals, charged species, and gas by-products. For hydrogen-based plasmas, the volume concentration of various hydrogen species may be about 20-80% of the gas at the wafer, typically over 50%. For oxygen-based plasmas, the volume concentration of various oxygen species may be about 20-80% of the gas at the wafer, typically over 50%. The volume concentration of various fluorine species may be 0.01% to about 2% or less than 1%. The volume concentration of various species from the weak oxidizing agent may be 0.05 to about 5% or about 1.2%. These species may include H2*, H2+, H+, H*, e-, OH, O*, CO, CO2, H2O, HF, F*, F-, CF, CF2, and CF3.

[0048] Process conditions may vary depending upon the wafer size. In some embodiments of the invention, it is desired to keep the work piece at a particular temperature during the application of plasmas to its surface. Wafer temperatures can range between about 110 degrees and about 500 degrees Celsius. To reduce the likelihood of photoresist popping described above, wafer temperature is preferably increased slowly until enough crust has been removed and photoresist popping ceases to be a concern. Initial station temperature may be about 110 degrees to about 260 degrees Celsius, for example, about 240 degrees Celsius. Later stations can use higher temperatures such as 285 degrees Celsius and about 350 degrees Celsius successfully with good strip rates. In certain embodiments, the temperature is lowered during NF3 spikes to reduce Si loss associated with these spikes.

EXAMPLE PROCESSES

[0049] As indicated above, in certain embodiments, a multi-station strip apparatus is employed to perform the photoresist and residue stripping processes described herein. Figure 5 is a simplified schematic showing a top view of such an apparatus including stations 1, 2, 3, 4, 5 and 6. Wafers enter the apparatus at station 1 via chamber 501, are transferred to each station in sequence for a processing operation at that station and exit from station 6 via chamber 502 after the process is complete. The architecture permits pausing or cooling the wafer after the passivation process to protect against silicon erosion by HDIS strip chemistries.

Example process 1

Station	Chemistry	Time	Temperature (C)
1 – Preheat	No gas	18 seconds	240
2 – FG passivation – plasma exposure	FG	18 seconds	240
2 – post-passivation wait	FG (plasma off)	220 seconds	240
3 – 4	H2/CO2/NF3	18 seconds per station	285
5 – 6	H2/CO2/FG	18 seconds per station	350

Example process 2

Station	Chemistry	Time	Temperature (C)
1 – FG passivation – plasma exposure	FG	18 seconds	240
1 – post-passivation wait	FG (plasma off)	220 seconds	
2 – 4	H2/CO2/NF3	18 seconds per station	285
5 – 6	H2/CO2/FG	18 seconds per station	350

[0050] In another example process, a first pass on 6 stations is performed to provide the forming gas passivation, followed by pre-heat in station 1 and strip operations in stations 2-6 in a second pass. The waiting operation may take place outside the chamber, in a non-oxidative environment.

[0051] The disclosed methods and apparatus may be implemented in systems including lithography and/or patterning hardware for semiconductor fabrication. Further, the disclosed methods may be implemented in a process with lithography and/or patterning processes preceding or following the disclosed methods.

Experimental

[0052] Various experiments were conducted comparing Si loss when the forming gas passivation in station 1 preceded F-containing strip operations in stations 2-6 to Si loss when no passivation process was performed. Silicon loss was reduced by 54% -82%.

[0053] While this invention has been described in terms of a few preferred embodiments, it should not be limited to the specifics presented above. Many variations on the above-described preferred embodiments may be employed. Therefore, the invention should be broadly interpreted with reference to the following claims.

CLAIMS

What is claimed is:

1. A method of removing material from a work piece surface in a reaction chamber, the method comprising:

exposing the work piece to a plasma generated from forming gas;

after exposing the work piece to the forming gas plasma, allowing the wafer to sit in a non-plasma environment for a time period of at least 30 seconds;

and after allowing the wafer to sit, exposing the wafer to an oxygen- or hydrogen-based plasma to remove the material.

2. The method of claim 1, wherein the work piece is allowed to sit for at least 100 seconds.

3. The method of claim 1, wherein the work piece is allowed to sit for at least 150 seconds.

4. The method of claim 1, wherein the work piece is allowed to sit for at least 200 seconds.

5. The method of claim 1, wherein the work piece is allowed to sit for at least 220 seconds.

6. The method of any of claims 1-5 wherein the oxygen- or hydrogen-based plasma comprises fluorine species.

7. The method of any of claims 1-6, wherein the material removed from the work piece surface comprises a high-dose implanted resist.

8. The method of any of claims 1-7, wherein the forming gas plasma is remotely generated.

9. The method of any of claims 1-8, wherein a protective film forms on exposed silicon portions of the workpiece after exposure to the forming gas plasma.

10. The method of claim 9 wherein the protective film is a Si_xN_y film.

11. The method of claim 1 wherein exposing the work piece is performed after a lithography operation.

12. An apparatus for removing material from a work piece surface comprising:

a reaction chamber comprising:

a plasma source,

a showerhead positioned downstream of the plasma source, and

a work piece support downstream of the showerhead, said work piece support comprising a pedestal and temperature-controlling mechanism to control a temperature of a work piece supported on the work piece support; and

a controller for executing a set of instructions, said set of instruction comprising instructions for exposing the work piece to a plasma generated from forming gas, after exposing the work piece to the forming gas plasma, allowing the work piece to sit in a non-plasma environment for a time period of at least 30 seconds; and after allowing the work piece to sit, exposing the wafer to an oxygen- or hydrogen-based plasma to remove the material.

13. The apparatus of claim 12 wherein the controller instructions comprises instructions for allowing the work piece to sit for at least 100 seconds.

14. The apparatus of claim 12 wherein the controller instructions comprises instructions for allowing the work piece to sit for at least 100 seconds.

15. The apparatus of claim 12 wherein the controller instructions comprises instructions for allowing the work piece to sit for at least 150 seconds.

16. The apparatus of claim 12 wherein the controller instructions comprises instructions for allowing the work piece to sit for at least 200 seconds.

17. The apparatus of claim 12 wherein the controller instructions comprises instructions for allowing the work piece to sit for at least 220 seconds.