

FINAL VERSION

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IPOS P/1071-290

REPLACED SHEETS SG

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CAPACITORS

~~LAYERED LC COMPONENTS~~

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

The present invention relates generally to
5 layered ~~LC components~~^{capacitors} and, more particularly, to multi-
terminal layered ~~LC components~~^{capacitors} and noise-absorbing
layered ceramic ~~LC components~~^{capacitors} which are used for reducing
or eliminating electrical noise in electronic apparatus,
for instance.

10 2. Description of the Related Art

Two-terminal and four-terminal, layered
capacitors are commonly used for reducing or eliminating
electrical noise in various electronic apparatus. As
shown in FIG. 8, a conventional four-terminal, layered
15 capacitor 51 comprises dielectric sheets 52 carrying
internal ground electrodes 53 on their surfaces,
dielectric sheets 52 carrying internal capacitor
electrodes 54 on their surfaces, and outermost protective
dielectric sheets 52.

20 The individual dielectric sheets 52 are stacked
one on top of another and calcined as a whole to form the
capacitor 51 shown in FIG. 9. An external input terminal
56 and external output terminal 57 are formed at opposite
end faces of the capacitor 51 while a pair of external
25 ground terminals 58 and 59 are formed at its front and
rear end faces, respectively, as illustrated in FIG. 9.
FIG. 10 is an equivalent circuit of the capacitor 51. A
four-terminal, layered capacitor 51 of this kind has a
higher resonant frequency than conventional two-terminal,
30 layered capacitors of the type having a plurality of

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internal electrodes on respective dielectric layers which are connected alternately to respective input and output electrodes. Also, in general they provide high attenuation in a high-frequency range.

5 Although the conventional four-terminal, layered capacitors 51 generally offer high attenuation factors at high frequencies, the amount of attenuation they achieve is lower than that of two-terminal, layered
10 capacitors around the resonant frequencies of the two-terminal, layered capacitors.

SUMMARY OF THE INVENTION

capacitors The invention provides multi-terminal, layered
~~IC components~~ *IC components* having excellent, improved attenuation characteristics even at resonant frequencies of the known
15 two-terminal, layered capacitors while maintaining a high attenuation capability in high-frequency ranges.

capacitor To achieve this, a multi-terminal, layered ~~IC~~
~~component~~ *component* according to an aspect of the invention
20 comprises a first internal capacitor electrode electrically connected to an external input terminal, a second internal capacitor electrode electrically connected to an external output terminal, an internal ground electrode electrically connected to an external
25 ground terminal to produce a capacitance between the first internal capacitor electrode and the internal ground electrode and another capacitance between the second internal capacitor electrode and the internal ground electrode, and an internal inductor electrode electrically connected between the external input
30 terminal and the external output terminal.

Provided with the internal inductor electrode, first and second internal capacitor electrodes and

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internal ground electrode, the aforementioned multi-
terminal, layered ^{capacitor} ~~LC component~~ of the invention forms a
circuit configured with two separate capacitor elements
and an inductor element. The layered ^{capacitor} ~~LC component~~ thus
constructed provides a lower resonant frequency than the
conventional four-terminal, layered capacitors while
maintaining a high-frequency attenuation capability
comparable to the latter. As a result, it becomes
possible to produce a four-terminal, layered ^{capacitor} ~~LC component~~
featuring excellent attenuation characteristics over a
wide frequency range.

A noise-absorbing, ceramic layered ^{capacitor} ~~LC component~~
according to a second aspect of the invention comprises a
plurality of internal electrodes embedded in a ceramic
body, the internal electrodes including capacitor element
patterns arranged in such a way that a plurality of
capacitor elements are formed and inductor element
patterns forming inductor elements, whereby a circuit in
which the capacitor elements are connected in parallel
with one another by the inductor elements in a plurality
of stages is formed.

Preferably the plurality of capacitor elements
provide different values of capacitance in the above
noise-absorbing, ceramic layered ^{capacitor} ~~LC component~~ of the
invention. Thus, it is possible to absorb electrical
noise in specific frequency bands corresponding to the
respective values of capacitance of the capacitor
elements. It is therefore apparent that this noise-
absorbing, ceramic layered ^{capacitor} ~~LC component~~ provides desired
noise-absorbing performance even when the electrical
noise is present in a plurality of frequency bands.

Furthermore, the necessary noise-absorbing
performance is obtainable without increasing the number

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of components since the individual capacitor elements and inductor elements of the noise-absorbing, ceramic layered ~~LC component~~^{capacitor} of the invention are integrally stacked into a one-piece structure. ✓

5 Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

10 FIG. 1 is an exploded perspective view of a four-terminal, layered ~~LC component~~^{capacitor} according to a first embodiment of the invention; ✓

15 FIG. 2 is a perspective view showing the external appearance of the four-terminal, layered ~~LC component~~^{capacitor} shown in FIG. 1; ✓

FIG. 3 is an equivalent circuit of the four-terminal, layered ~~LC component~~^{capacitor} shown in FIG. 2; ✓

20 FIG. 4 is a graph representing attenuation characteristics of the four-terminal, layered ~~LC component~~^{capacitor} of FIG. 2; ✓

FIG. 5 is an exploded perspective view of a four-terminal, layered ~~LC component~~^{capacitor} according to a second embodiment of the invention; ✓

25 FIG. 6 is a perspective view showing the external appearance of the four-terminal, layered ~~LC component~~^{capacitor} shown in FIG. 5; ✓

FIG. 7 is an equivalent circuit of the four-terminal, layered ~~LC component~~^{capacitor} shown in FIG. 6; ✓

30 FIG. 8 is an exploded perspective view of a conventional four-terminal, layered capacitor;

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FIG. 9 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 8;

FIG. 10 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 9;

FIG. 11 is an exploded perspective view of a ceramic layered ~~LC-component~~^{capacitor} according to a third embodiment of the invention;

FIG. 12 is a perspective view showing the external appearance of the ceramic layered ~~LC-component~~^{capacitor} of the third embodiment;

FIG. 13 is a cross-sectional diagram showing an internal electrode arrangement of the ceramic layered ~~LC-component~~^{capacitor} of the third embodiment;

FIG. 14 is an equivalent circuit of the ceramic layered ~~LC-component~~^{capacitor} of the third embodiment;

FIG. 15 is a graph representing noise-absorbing characteristics of the ceramic layered ~~LC-component~~^{capacitor} of the third embodiment; and

FIG. 16 is a perspective view of an internal ground electrode which is used in a four-terminal, ceramic layered ~~LC-component~~^{capacitor} according to a variation of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Multi-terminal, layered ~~LC-components~~^{capacitors} according to embodiments of the invention are now described in detail with reference to the accompanying drawings, in which like elements and assemblies are designated by like reference numbers.

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FIRST EMBODIMENT

capacitor As shown in FIG. 1, a four-terminal, layered ~~is~~ ✓
component 1 of a first embodiment comprises a dielectric ✓
sheet 2 carrying an internal inductor electrode 3 on its
surface, dielectric sheets 2 carrying internal ground
electrodes 4 on their surfaces, dielectric sheets 2
carrying internal capacitor electrodes 5 and 6 on their
surfaces, and outermost protective dielectric sheets 2.
Each dielectric sheet 2 is made of a ceramic material,
for example.

The internal inductor electrode 3 is generally
patterned to form a sinuous shape with its extreme left
segment 3a and extreme right segment 3b exposed at left
and right edges of the dielectric sheet 2, respectively.
The internal capacitor electrodes 5 are located on the
left side of the individual dielectric sheets 2 with
extreme left ends 5a of the internal capacitor electrodes
5 exposed at left edges of the dielectric sheets 2,
while the internal capacitor electrodes 6 are located on
the right side of the individual dielectric sheets 2 with
extreme right ends 6a of the internal capacitor
electrodes 6 exposed at right edges of the dielectric
sheets 2. The electrodes 3 to 6 are layers of silver
(Ag), silver-palladium alloy (Ag-Pd) or Nickel (Ni), for
example, formed by using a technique such as printing,
sputtering or vacuum evaporation.

All the dielectric sheets 2 are stacked in the
order shown in FIG. 1, and calcined to form a single
laminated body. As illustrated in FIG. 2, an external
input terminal 10 and external output terminal 11 are
formed at left and right end faces of the laminated body
while a pair of external ground terminals 12 and 13 are
formed at front and rear end faces, respectively. The

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external input terminal 10 is electrically connected to the extreme left segment 3a of the internal inductor electrode 3 as well as to the extreme left end 5a of each internal capacitor electrode 5, while the external output terminal 11 is electrically connected to the extreme right segment 3b of the internal inductor electrode 3 as well as to the extreme right end 6a of each internal capacitor electrode 6. Further, the external ground terminals 12 and 13 are electrically connected to outer ends 4a and 4b of each internal ground electrode 4, respectively.

The four-terminal, layered ^{capacitor} ~~LC-component~~ 1 having the above-described structure can be regarded, with reference to its equivalent circuit shown in FIG. 3, as being constructed by separating a single capacitor of the conventional structure (shown in FIG. 10) into a pair of capacitors, that is, a capacitor C1 formed by the internal capacitor electrodes 5 and the internal ground electrodes 4 and a capacitor C2 formed by the internal capacitor electrodes 6 and the internal ground electrodes 4, and then connecting the capacitors C1 and C2 together by means of the internal inductor electrode 3.

A curve (solid line 21) shown in FIG. 4 represents measured attenuation characteristics of the four-terminal, layered ^{capacitor} ~~LC-component~~ 1, of which the capacitance is 0.15 μ F in this embodiment. FIG. 4 also shows, for comparison, attenuation characteristics of a conventional two-terminal, layered capacitor (dotted line 22) and of a conventional four-terminal, layered capacitor (dotted line 23), both having the same value of capacitance as the four-terminal, layered ^{capacitor} ~~LC-component~~ 1 of the first embodiment. As can be seen from FIG. 4, the four-terminal, layered ~~LC-component~~ capacitor 1 of the

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first embodiment has a lower resonant frequency than the conventional four-terminal, layered capacitor due to the inductance of the internal inductor electrode 3, and has greater attenuation over a wider frequency range due to the capacitors C1 and C2.

SECOND EMBODIMENT

As shown in FIG. 5, a four-terminal, layered capacitor component 31 of a second embodiment of the invention is the same as the capacitor 1 of the first embodiment except for the structure of an internal inductor electrode 32 which is made up of a series of segments 32a-32e which are formed in series with a pair of internal capacitor electrodes 33 and 34. The internal inductor electrode 32 includes curved segments 32a, 32b and 32c with extreme outer segments 32d and 32e exposed at left and right edges of the dielectric sheet 2, respectively. The internal capacitor electrode 33 is electrically connected between the curved segments 32a and 32b while the internal capacitor electrode 34 is electrically connected between the curved segments 32b and 32c.

The individual dielectric sheets 2 are stacked in the order shown in FIG. 5, and calcined to form a single laminated body. An external input terminal 36 and external output terminal 37 are formed at left and right end faces of the laminated body while a pair of external ground terminals 38 and 39 are formed at front and rear end faces, respectively, as illustrated in FIG. 6. The external input terminal 36 is electrically connected to the extreme left segment 32d of the internal inductor electrode 3 as well as to the extreme left end 5a of each internal capacitor electrode 5, while the external output

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terminal 37 is electrically connected to the extreme right segment 32e of the internal inductor electrode 3 as well as to the extreme right end 6a of each internal capacitor electrode 6. Further, the external ground terminals 38 and 39 are electrically connected to outer ends 4a and 4b of each internal ground electrode 4, respectively.

The four-terminal, layered ^{capacitor} ~~LC-component~~ 31 having the above-described structure can be regarded, with reference to its equivalent circuit shown in FIG. 7, as being constructed by separating the single capacitor of the conventional structure (shown in FIG. 10) into a pair of capacitors, that is, a capacitor C1 formed by the internal capacitor electrodes 5 and the internal ground electrodes 4 and a capacitor C2 formed by the internal capacitor electrodes 6 and the internal ground electrodes 4, and then connecting the capacitors C1 and C2 by an LC circuit made up of inductors 32a-32c formed by the internal inductor electrode 32 and capacitors C3 and C4 formed by the internal capacitor electrodes 33, 34 and 4. An advantage of this four-terminal, layered ^{capacitor} ~~LC-component~~ 31 is that its resonant frequency is even lower than that of the four-terminal, layered ^{capacitor} ~~LC-component~~ 1 of the first embodiment.

Additional features of the invention are described in further detail with reference to the following third embodiment, in which three distinct capacitor elements are formed in a noise-absorbing, ceramic layered ^{capacitor} ~~LC-component~~ (hereinafter referred to simply as a ceramic layered ^{capacitor} ~~LC-component~~).

THIRD EMBODIMENT

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FIG. 11 is an exploded perspective view showing
the construction of a ceramic layered ^{capacitor} ~~LC-component~~ 101 ✓
according to a third embodiment of the invention; FIG. 12
is a perspective view showing the external appearance of
the ceramic layered ^{capacitor} ~~LC-component~~ 101; FIG. 13 is a cross- ✓
sectional diagram showing an internal electrode
arrangement including capacitor and inductor element
patterns of the ceramic layered ^{capacitor} ~~LC-component~~ 101; and ✓
FIG. 14 is an equivalent circuit of the ceramic layered
^{capacitor} ~~LC-component~~ 101. To facilitate understanding of the ✓
internal electrode arrangement, each layer (plane)
containing capacitor and/or inductor element patterns is
regarded as a distinct ceramic sheet.

As shown in FIGS. 11 and 12, the ceramic
layered ^{capacitor} ~~LC-component~~ 101 comprises a laminated ceramic ✓
body 102 formed by stacking a plurality of ceramic sheets
102a to 102f and four external terminals 103a to 103d
fitted to outer surfaces of the laminated ceramic body
102. Additional ceramic sheets carrying no electrodes
(not shown) are laminated on the top and bottom of the
laminated ceramic body 102.

The ceramic layered ^{capacitor} ~~LC-component~~ 101 contains ✓
capacitor element patterns 104a to 104d provided on the
ceramic sheets 102a, 102b, 102e and 102f, respectively,
to form a capacitor element 104, capacitor element
patterns 105a to 105d provided on the same ceramic sheets
102a, 102b, 102e and 102f, respectively, to form a
capacitor element 105, and capacitor element patterns
106a and 106b provided on the ceramic sheets 102c and
102d, respectively, to form a capacitor element 106. The
individual capacitor element patterns 104a-104d, 105a-
105d, 106a and 106b are so arranged that the capacitor
elements 104 and 105 have the same value of capacitance

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and the capacitor element 106 has a smaller value of capacitance compared to the capacitor elements 104 and 105.

capacitor
The ceramic layered ~~LC-component~~ 101 further
contains inductor element patterns 107a to 110a provided
on the ceramic sheets 102c and 102d to form four inductor
elements 107 to 110 which interconnect the capacitor
elements 104, 105 and 106. The individual inductor
element patterns 107a to 110a are so arranged that all
the inductor elements 107 to 110 have the same
inductance.

As can be seen from the equivalent circuit of
the ceramic layered ~~LC-component~~ ^{capacitor} 101 shown in FIG. 14,
the capacitor element 106 is connected to the capacitor
element 104 by the inductor elements 107 and 108, and the
capacitor element 105 is connected to the capacitor
element 106 by the inductor elements 109 and 110 to form
together a network in which the individual capacitor
elements 104 to 106 are connected in parallel with one
another by the inductor elements 107 to 110. The
external terminals 103a and 103b are connected to both
leads of the capacitor element 104 while the external
terminals 103c and 103d are connected to both leads of
the capacitor element 105 to complete the four-terminal,
ceramic layered ~~LC-component~~ ^{capacitor} 101.

capacitor
The ceramic layered ~~LC-component~~ 101 is
bidirectional in operation because it has a bilaterally
symmetric configuration with the capacitor elements 104
and 105 having the same capacitance located at both ends
of the device. More specifically, the ceramic layered
~~LC-component~~ ^{capacitor} 101 may be connected so that the external
terminals 103a and 103b act as input terminals and the
external terminals 103c and 103d act as output terminals,

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or the external terminals 103c and 103d act as input terminals and the external terminals 103a and 103b act as output terminals.

FIG. 15 is a graph representing noise-absorbing characteristics of the ceramic layered ^{capacitor} ~~LC-component~~ 101 showing a relationship between frequency and attenuation factor. A solid line G1 in the graph shows noise-absorbing characteristics of the whole ceramic layered ^{capacitor} ~~LC-component~~ 101, an alternate long and short dashed line G2 shows noise-absorbing characteristics of each of the capacitor elements 104 and 105 only, and another alternate long and short dashed line G3 shows noise-absorbing characteristics of the capacitor element 106 only.

It can be seen from FIG. 15 that the ceramic layered ^{capacitor} ~~LC-component~~ 101 has two prominent attenuation bands F1 and F2. This indicates that the noise-absorbing characteristics of the individual capacitor elements 104, 105 and 106 remain effective in the ceramic layered ^{capacitor} ~~LC-component~~ 101. According to this embodiment, a single ceramic layered ^{capacitor} ~~LC-component~~ provides the necessary noise-absorbing performance even when electrical noise is present in two separate frequency ranges.

VARIATIONS OF THE EMBODIMENTS

While the invention has been described in conjunction with embodiments thereof, details of the construction of the above-described multi-terminal, layered ^{capacitors} ~~LC-components~~ can be varied in various ways.

As an example, a dielectric sheet which acts as a spacer may be inserted between each internal inductor electrode and internal ground electrode in the

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aforementioned embodiments to eliminate or reduce stray capacitance appearing between the two electrodes.

In another variation, at least one set of internal inductor electrodes and internal ground electrodes is provided at a specific point in the vertical, or stacking, direction of a multi-terminal, layered ~~LC-component~~^{capacitor} for achieving symmetry in electrode arrangement or for adjusting the inductance component of the layered ~~LC-component~~^{capacitor}.

The foregoing discussion of the embodiments is based on the assumption that each multi-terminal, layered ~~LC-component~~^{capacitor} is manufactured singly. In the case of mass production, a plurality of multi-terminal, layered ~~LC-components~~^{capacitors} can be produced at once by making a large substrate having the layer structure as described above and then cutting it into chips of a desired size.

Although the capacitors of the aforementioned embodiments are made by stacking a plurality of dielectric sheets and calcining the stack, the invention is not limited to this construction. In one alternative, the individual dielectric sheets may be calcined before stacking. In another alternative, the layer structure of dielectric sheets and electrodes of each capacitor may be produced by alternately applying and drying pasty dielectric and conductive materials by using a printing technique, for instance.

In the first and second embodiments, each of the internal ground electrodes 4 need not necessarily be made of a single electrode element but may be divided into two separate parts as shown in FIG. 16.

Although there are produced three capacitor elements 104, 105 and 106 in the third embodiment described above, the embodiment may be modified to form

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two capacitor elements, or four or more capacitor elements, interconnected by as many inductor elements as necessary, within the scope of the invention.

5 The invention is not limited to the
aforementioned preferred embodiments and the variations
thereof in other respects as well. Shapes and
arrangements of the individual capacitor element
patterns, inductor element patterns and external
terminals may be altered or modified without departing
10 from the spirit and scope of the invention.

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WHAT IS CLAIMED IS:

Capacitor with a plurality of dielectric sheets, said dielectric sheets

1. A multi-terminal, layered ~~LC~~ component comprising:

- an external input terminal;
- an external output terminal;
- an external ground terminal;
- a first internal capacitor electrode

electrically connected to said external input terminal;

- a second internal capacitor electrode

electrically connected to said external output terminal;

an internal ground electrode electrically connected to said external ground terminal, said internal ground electrode producing a capacitance between said first internal capacitor electrode and said internal ground electrode and another capacitance between said second internal capacitor electrode and said internal ground electrode; and

an internal inductor electrode electrically connected between said external input terminal and said external output terminal, wherein said plurality of dielectric sheets are stacked integrally.

2. A four-terminal, layered ~~LC~~ component comprising:

- an external input terminal;
- an external output terminal;
- a pair of external ground terminals;
- a first internal capacitor electrode

electrically connected to said external input terminal;

- a second internal capacitor electrode

electrically connected to said external output terminal;

an internal ground electrode electrically connected to said pair of external ground terminals, said

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Capacitor with a plurality of dielectric sheets, said dielectric sheets



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internal ground electrode producing a capacitance between
said first internal capacitor electrode and said internal
ground electrode and another capacitance between said
second internal capacitor electrode and said internal
ground electrode; and

an internal inductor electrode electrically
connected between said external input terminal and said
external output terminal,

*wherein said plurality of dielectric sheets
are stacked integrally.*

3. A four-terminal layered ~~LC~~-component
according to claim 2, wherein said internal ground
electrode comprises a pair of internal ground electrode
members each connected to a respective one of said
external ground terminals.

capacitor

4. A four-terminal, layered ~~LC~~-component
according to claim 2, wherein said internal inductor
electrode has a curved segment and a third internal
capacitor electrode which forms a third capacitance with
said internal ground electrode.

capacitor 5. A noise-absorbing, ceramic layered ~~LC~~-
~~component~~ comprising a plurality of internal electrodes
embedded in a ceramic body, said internal electrodes
including:

capacitor element patterns arranged to form a
plurality of capacitor elements having different values
of capacitance; and

inductor element patterns forming inductor
elements which interconnect said capacitor elements in
parallel with one another via said inductor elements in a
plurality of stages,

*wherein said ceramic body is formed by
stacking a plurality of dielectric sheets.*

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capacitor 6. A noise-absorbing, ceramic layered ~~is~~
~~component~~ according to claim 5, further comprising a
plurality of external terminals connected respectively
to said capacitor elements. ✓

capacitor 7. A noise-absorbing, ceramic layered ~~is~~
~~component~~ according to claim 6, wherein said capacitor
element patterns are arranged in such a way that one of
said capacitor elements has a smaller value of
5 capacitance than the remainder thereof. ✓

capacitor 8. A noise-absorbing, ceramic layered ~~is~~
~~component~~ according to claim 5, wherein said capacitor
element patterns are arranged in such a way that one of
said capacitor elements has a smaller value of
5 capacitance than the remainder thereof. ✓

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LAYERED

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LAYER-BUILT CAPACITORS

ABSTRACT OF THE DISCLOSURE

capacitors

Multi-terminal, layered ~~LC~~ components having
excellent attenuation characteristics over a wide
frequency range. A four-terminal, layered ~~LC~~ ^{capacitor} component
has a dielectric sheet with an internal inductor
electrode connecting an external input terminal to an
external output terminal, dielectric sheets with internal
capacitor electrodes connected to the external input
terminal, and internal capacitor electrodes connected to
the external output terminal, and dielectric sheets with
internal ground electrodes connected to external ground
terminals. All these dielectric sheets are integrally
stacked and calcined to form a one-piece structure.

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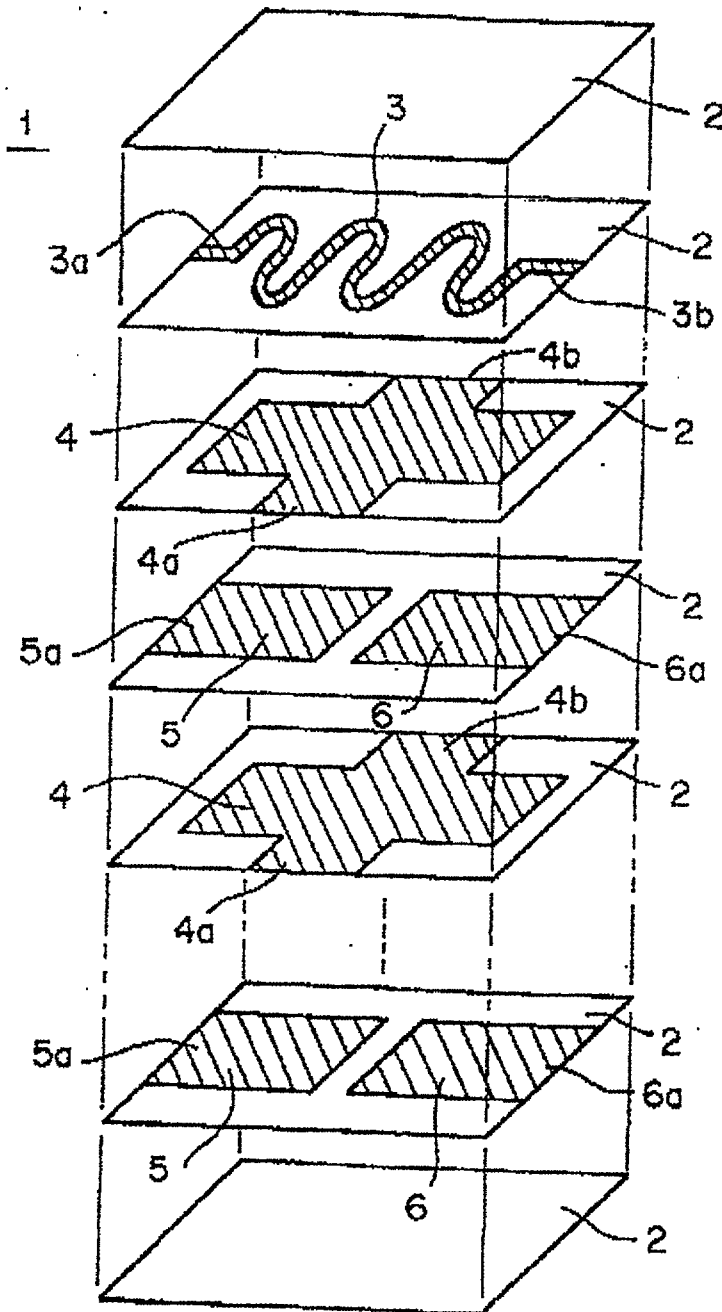


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【図1】 FIG.1



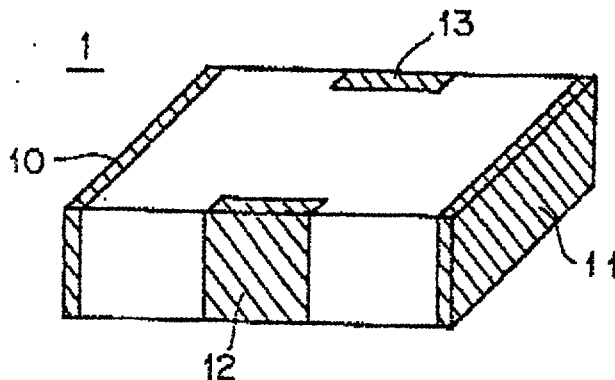
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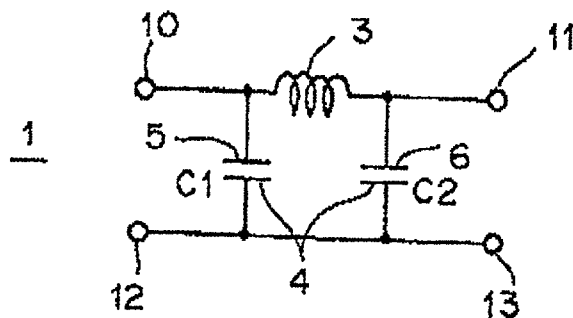
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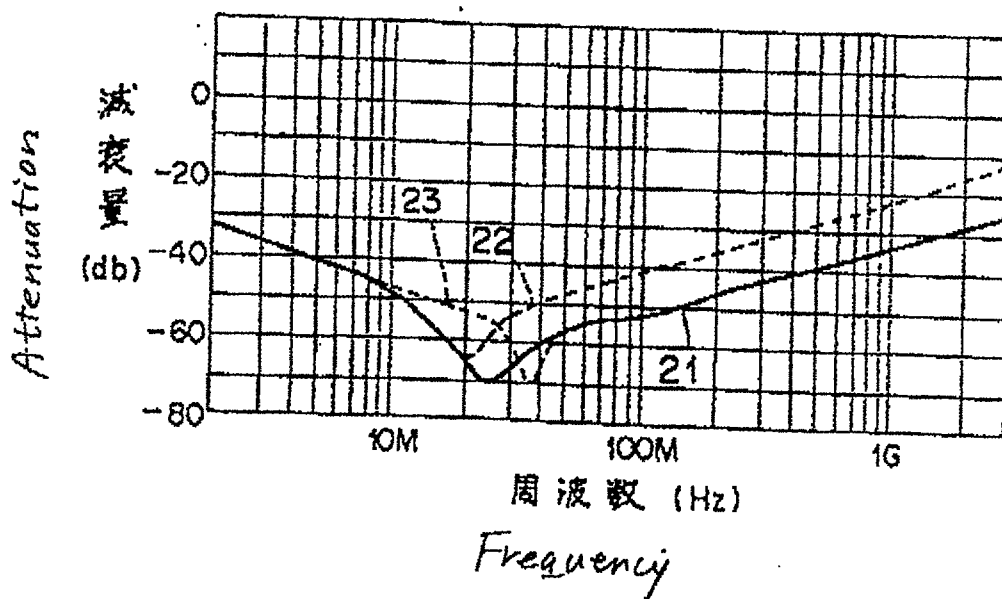
【図2】 FIG.2



【図3】 FIG.3



【図4】 FIG. 4

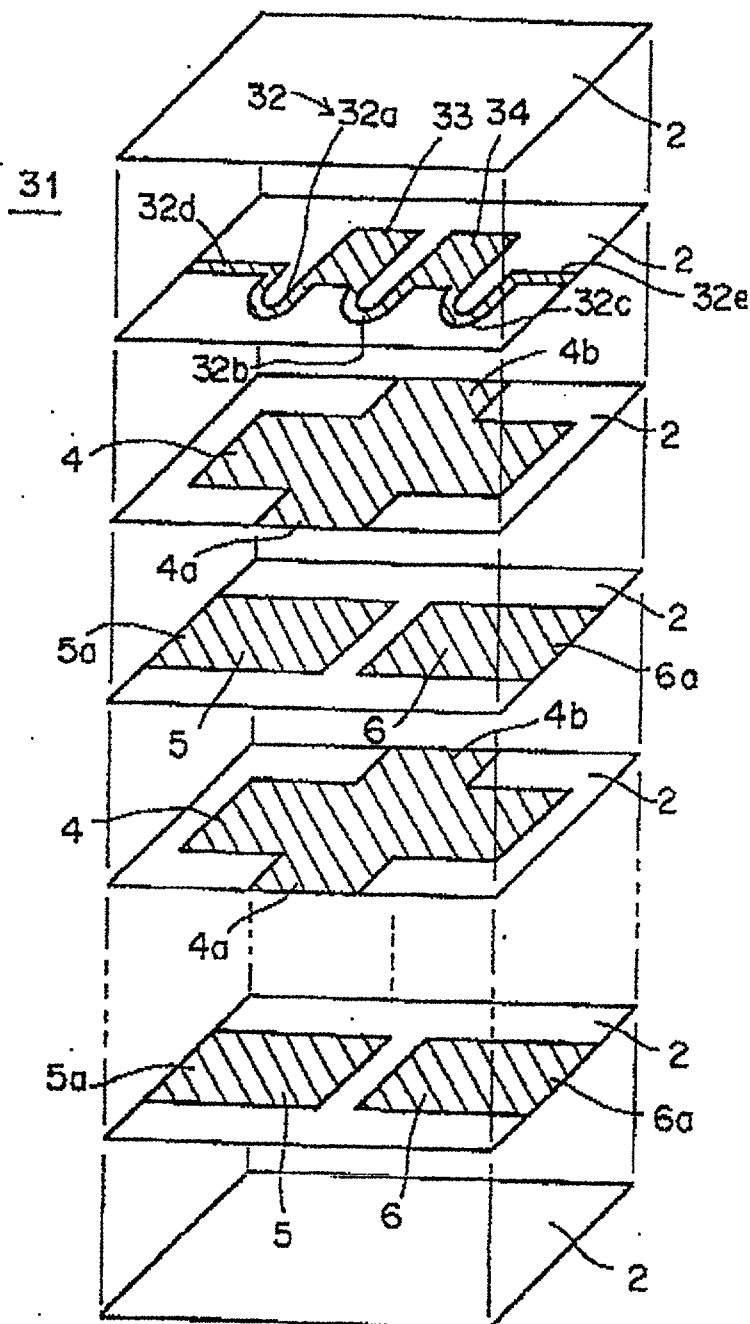


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【図5】 Fig. 5



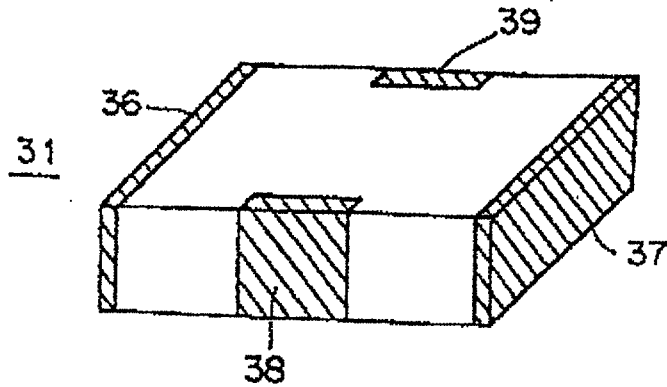
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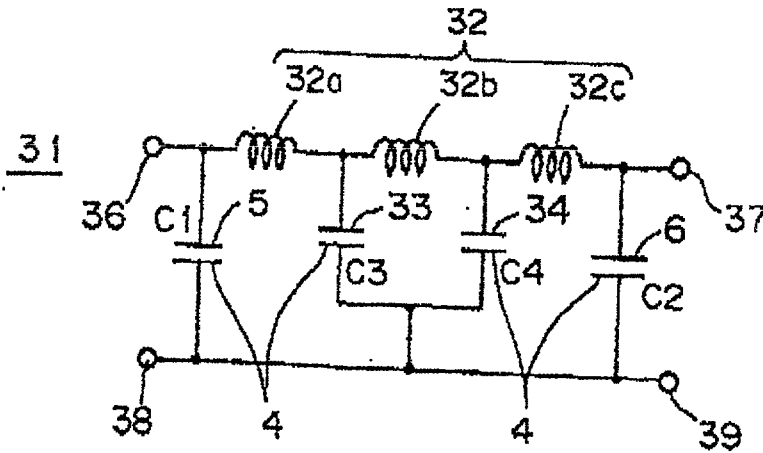
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【図6】 FIG. 6



【図7】 FIG. 7



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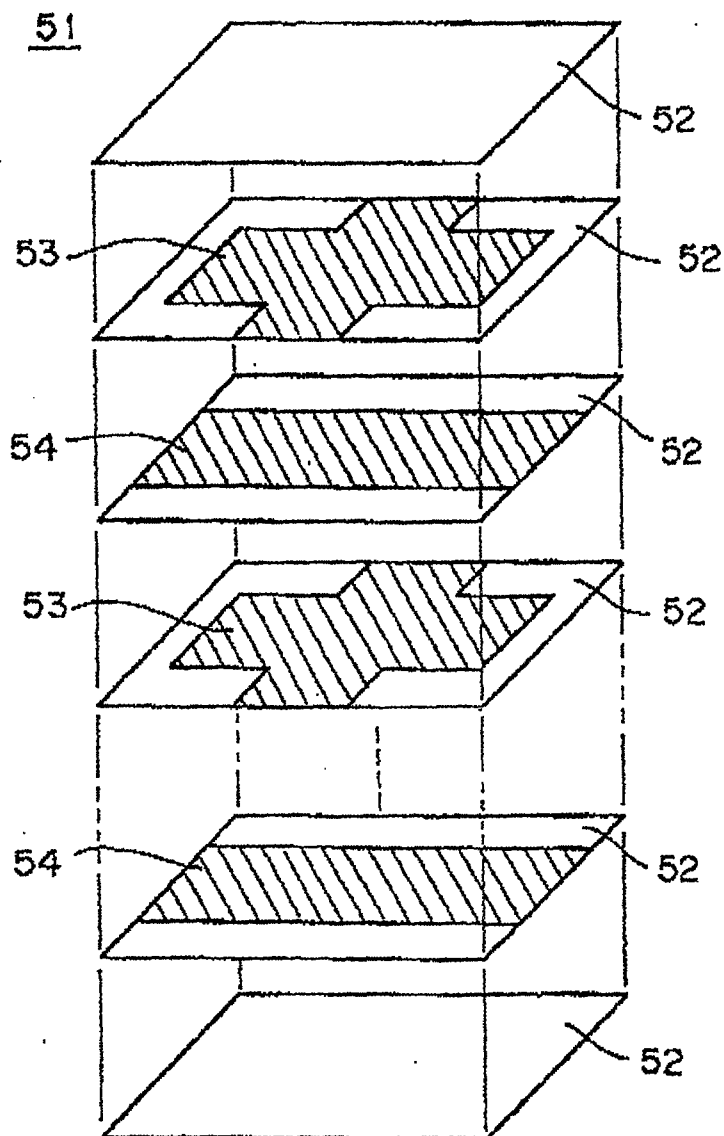


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【図8】 FIG. 8



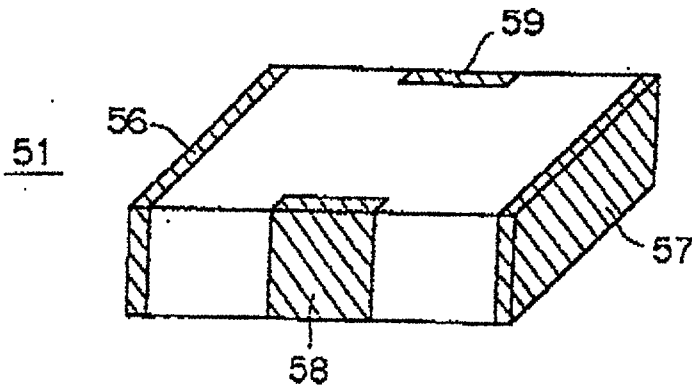
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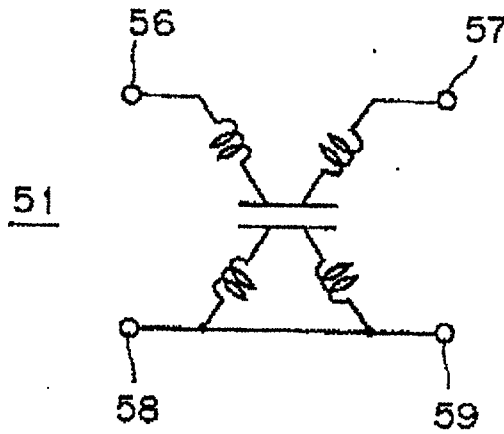
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【図9】 FIG.9



【図10】 FIG.10



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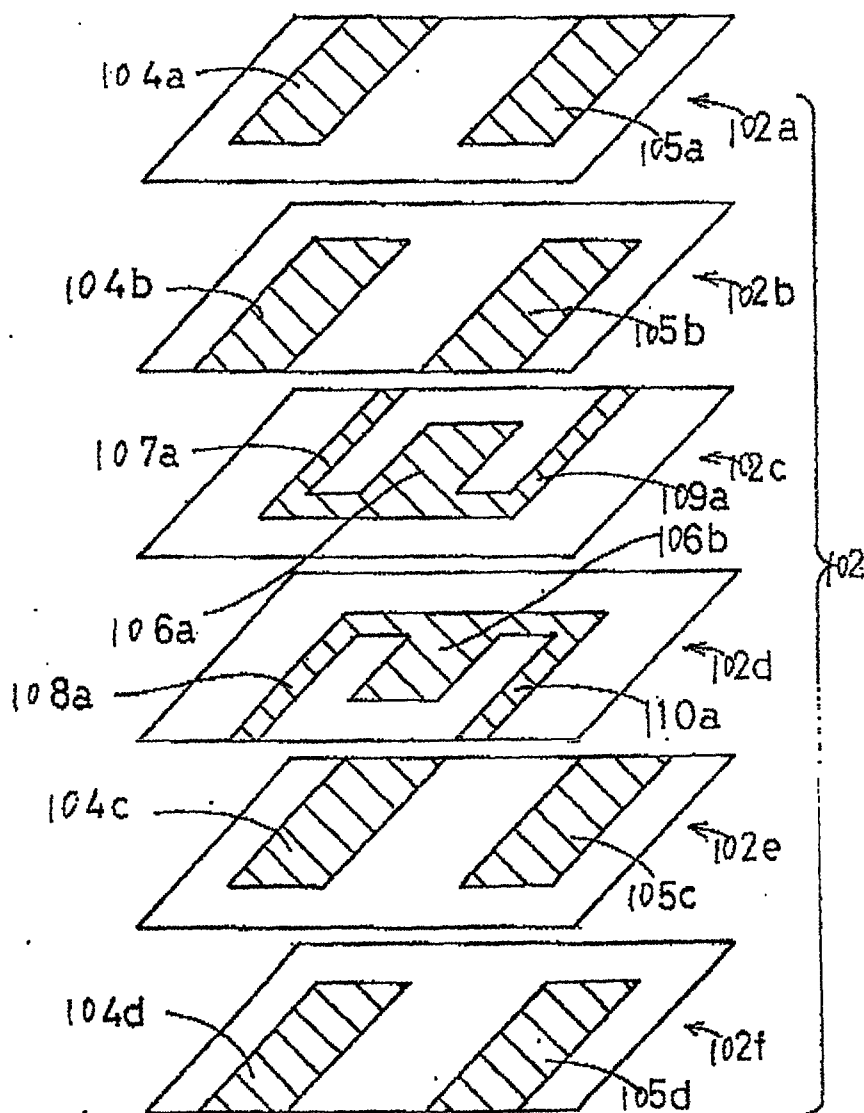
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FIG. 11

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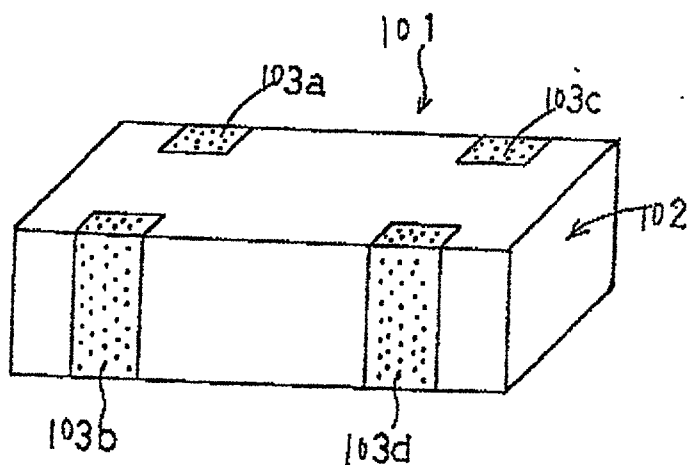


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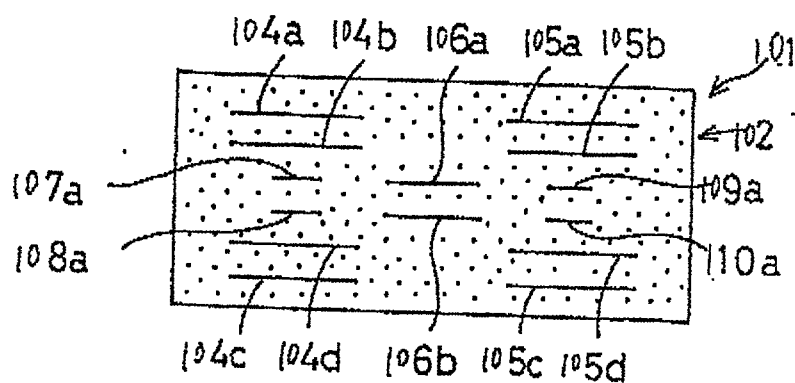
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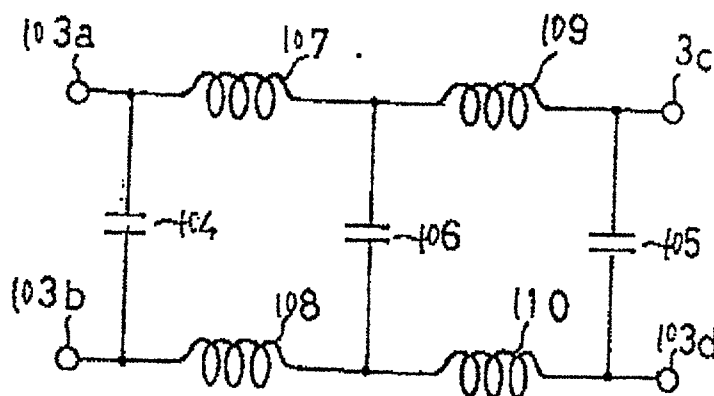
【図12】 FIG. 12



【図13】 FIG. 13



【図14】 FIG. 14

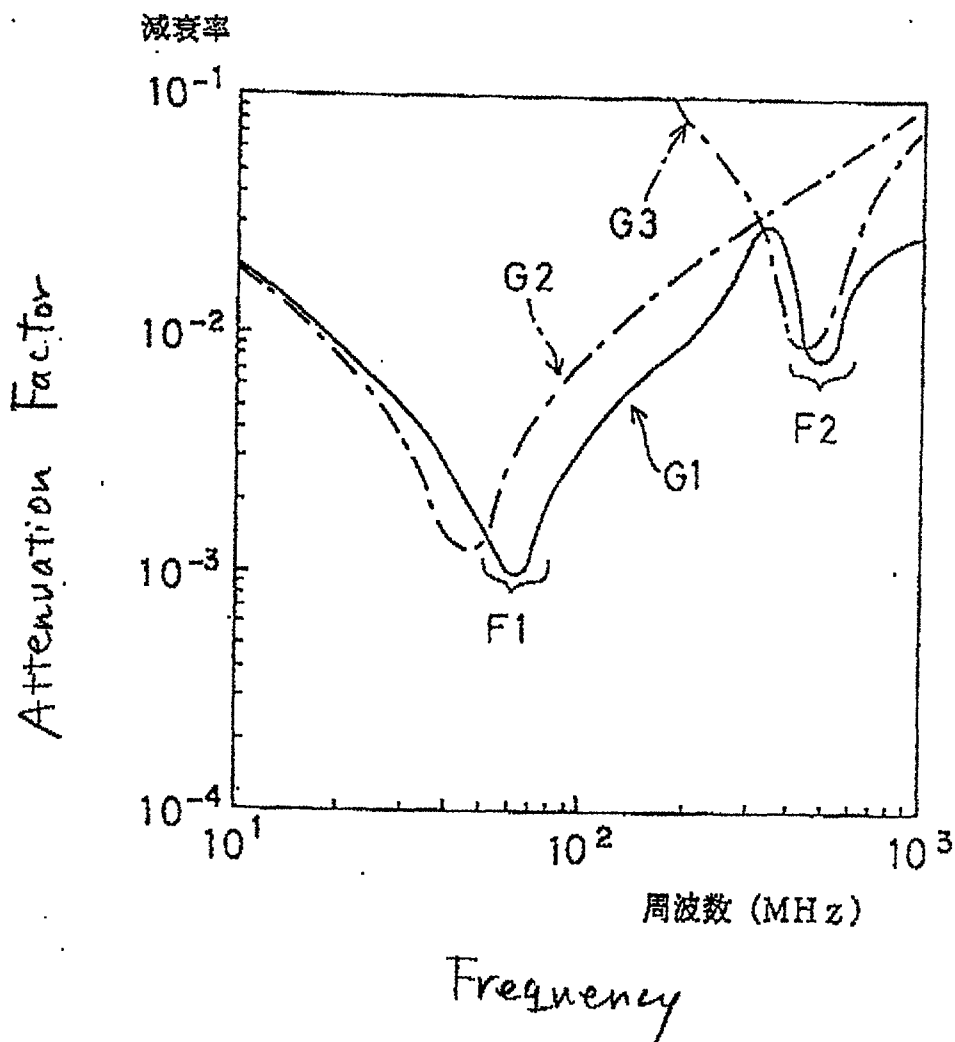


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【図】
 15 FIG. 15

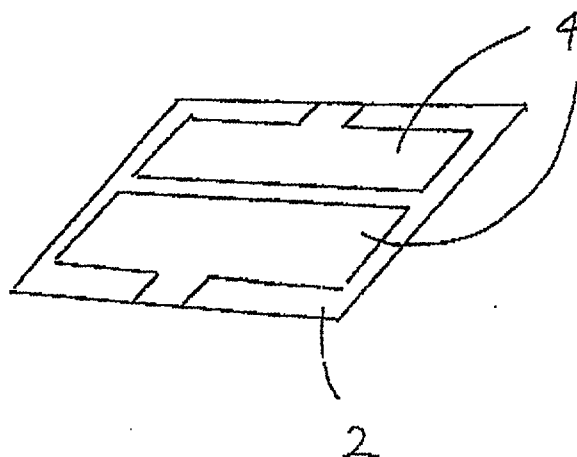


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[図 16] FIG. 16



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☒	Abstract : paged 24 to paged 10	
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REPLACED SHEETS		SG
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LAYERED CAPACITORS

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

The present invention relates generally to layered capacitors and, more particularly, to multi-terminal, layered capacitors and noise-absorbing, ceramic layered capacitors which are used for reducing or eliminating electrical noise in electronic apparatus, for instance.

2. Description of the Related Art

Two-terminal and four-terminal, layered capacitors are commonly used for reducing or eliminating electrical noise in various electronic apparatus. As shown in FIG. 8, a conventional four-terminal, layered capacitor 51 comprises dielectric sheets 52 carrying internal ground electrodes 53 on their surfaces, dielectric sheets 52 carrying internal capacitor electrodes 54 on their surfaces, and outermost protective dielectric sheets 52.

The individual dielectric sheets 52 are stacked one on top of another and calcined as a whole to form the capacitor

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51 shown in FIG. 9. An external input terminal 56 and external output terminal 57 are formed at opposite end faces of the capacitor 51 while a pair of external ground terminals 58 and 59 are formed at its front and rear end faces, respectively, as illustrated in FIG. 9. FIG. 10 is an equivalent circuit of the capacitor 51. The four-terminal, layered capacitor 51 of this kind has a higher resonant frequency than conventional two-terminal, layered capacitors of the type having a plurality of internal electrodes on respective dielectric layers which are connected alternately to respective input and output end electrodes. Also, in general they provide high attenuation in a high-frequency range.

Although the conventional four-terminal, layered capacitors 51 generally offer high attenuation factors at high frequencies, the amount of attenuation they achieve is lower than that of two-terminal, layered capacitors around the resonant frequencies of the two-terminal, layered capacitors.

SUMMARY OF THE INVENTION

The invention provides multi-terminal, layered capacitors having excellent, improved attenuation

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characteristics even at resonant frequencies of the known two-terminal, layered capacitors while maintaining a high attenuation capability in high-frequency ranges.

To achieve this, a multi-terminal, layered capacitor according to an aspect of the invention comprises a first internal capacitor electrode electrically connected to an external input terminal, a second internal capacitor electrode electrically connected to an external output terminal, an internal ground electrode electrically connected to an external ground terminal to produce a capacitance between the first internal capacitor electrode and the internal ground electrode and another capacitance between the second internal capacitor electrode and the internal ground electrode, and an internal inductor electrode electrically connected between the external input terminal and the external output terminal.

Provided with the internal inductor electrode, first and second internal capacitor electrodes and internal ground electrode, the aforementioned multi-terminal, layered capacitor of the invention forms a circuit configured with two separate capacitor elements and an inductor element. The layered capacitor thus constructed provides a lower resonant

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frequency than the conventional four-terminal, layered capacitors while maintaining a high-frequency attenuation capability comparable to the latter. As a result, it becomes possible to produce a four-terminal, layered capacitor featuring excellent attenuation characteristics over a wide frequency range.

A noise-absorbing, ceramic layered capacitor according to a second aspect of the invention comprises a plurality of internal electrodes embedded in a ceramic body, the internal electrodes including capacitor element patterns arranged in such a way that a plurality of capacitor elements are formed and inductor element patterns forming inductor elements, whereby a circuit in which the capacitor elements are connected in parallel with one another by the inductor elements in a plurality of stages is formed.

Preferably the plurality of capacitor elements provide different values of capacitance in the above noise-absorbing, ceramic layered capacitor of the invention. Thus, it is possible to absorb electrical noise in specific frequency bands corresponding to the respective values of capacitance of the capacitor elements. It is therefore apparent that this noise-absorbing, ceramic layered capacitor provides

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desired noise-absorbing performance even when the electrical noise is present in a plurality of frequency bands.

Furthermore, the necessary noise-absorbing performance is obtainable without increasing the number of components since the individual capacitor elements and inductor elements of the noise-absorbing, ceramic layered capacitor of the invention are integrally stacked into a one-piece structure.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an exploded perspective view of a four-terminal, layered capacitor according to a first embodiment of the invention;

FIG. 2 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 1;

FIG. 3 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 2;

FIG. 4 is a graph representing attenuation characteristics of the four-terminal, layered capacitor of

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FIG. 2;

FIG. 5 is an exploded perspective view of a four-terminal, layered capacitor according to a second embodiment of the invention;

FIG. 6 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 5;

FIG. 7 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 6;

FIG. 8 is an exploded perspective view of a conventional four-terminal, layered capacitor;

FIG. 9 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 8;

FIG. 10 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 9;

FIG. 11 is an exploded perspective view of a ceramic layered capacitor according to a third embodiment of the invention;

FIG. 12 is a perspective view showing the external appearance of the ceramic layered capacitor of the third embodiment;



FIG. 13 is a cross-sectional diagram showing an internal electrode arrangement of the ceramic layered capacitor of the third embodiment;

FIG. 14 is an equivalent circuit of the ceramic layered capacitor of the third embodiment;

FIG. 15 is a graph representing noise-absorbing characteristics of the ceramic layered capacitor of the third embodiment; and

FIG. 16 is a perspective view of an internal ground electrode which is used in a four-terminal, ceramic layered capacitor according to a variation of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Multi-terminal, layered capacitors according to embodiments of the invention are now described in detail with reference to the accompanying drawings, in which like elements and assemblies are designated by like reference numbers.

FIRST EMBODIMENT

As shown in FIG. 1, a four-terminal, layered capacitor 1 of a first embodiment comprises a dielectric sheet 2 carrying an internal inductor electrode 3 on its surface, dielectric sheets 2 carrying internal ground electrodes 4 on

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their surfaces, dielectric sheets 2 carrying internal capacitor electrodes 5 and 6 on their surfaces, and outermost protective dielectric sheets 2. Each dielectric sheet 2 is made of a ceramic material, for example.

The internal inductor electrode 3 is generally patterned to form a sinuous shape with its extreme left segment 3a and extreme right segment 3b exposed at left and right edges of the dielectric sheet 2, respectively. The internal capacitor electrodes 5 are located on the left side of the individual dielectric sheets 2 with extreme left ends 5a of the internal capacitor electrodes 5 exposed at left edges of the dielectric sheets 2, while the internal capacitor electrodes 6 are located on the right side of the individual dielectric sheets 2 with extreme right ends 6a of the internal capacitor electrodes 6 exposed at right edges of the dielectric sheets 2. The electrodes 3 to 6 are layers of silver (Ag), silver-palladium alloy (Ag-Pd) or Nickel (Ni), for example, formed by using a technique such as printing, sputtering or vacuum evaporation.

All the dielectric sheets 2 are stacked in the order shown in FIG. 1, and calcined to form a single laminated body. As illustrated in FIG. 2, an external input terminal

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10 and external output terminal 11 are formed at left and right end faces of the laminated body while a pair of external ground terminals 12 and 13 are formed at front and rear end faces, respectively. The external input terminal 10 is electrically connected to the extreme left segment 3a of the internal inductor electrode 3 as well as to the extreme left end 5a of each internal capacitor electrode 5, while the external output terminal 11 is electrically connected to the extreme right segment 3b of the internal inductor electrode 3 as well as to the extreme right end 6a of each internal capacitor electrode 6. Further, the external ground terminals 12 and 13 are electrically connected to outer ends 4a and 4b of each internal ground electrode 4, respectively.

The four-terminal, layered capacitor 1 having the above-described structure can be regarded, with reference to its equivalent circuit shown in FIG. 3, as being constructed by separating a single capacitor of the conventional structure (shown in FIG. 10) into a pair of capacitors, that is, a capacitor C1 formed by the internal capacitor electrodes 5 and the internal ground electrodes 4 and a capacitor C2 formed by the internal capacitor electrodes 6 and the internal ground electrodes 4, and then connecting the



capacitors C1 and C2 by means of the internal inductor electrode 3.

A curve (solid line 21) shown in FIG. 4 represents measured attenuation characteristics of the four-terminal, layered capacitor 1, of which capacitance is $0.15 \mu\text{F}$ in this embodiment. FIG. 4 also shows for comparison attenuation characteristics of a conventional two-terminal, layered capacitor (dotted line 22) and of a conventional four-terminal, layered capacitor (dotted line 23), both having the same value of capacitance as the four-terminal, layered capacitor 1 of the first embodiment. As can be seen from FIG. 4, the four-terminal, layered capacitor 1 of the first embodiment has a lower resonant frequency than the conventional four-terminal, layered capacitor due to the inductance of the internal inductor electrode 3, and has greater attenuation over a wider frequency range due to the capacitors C1 and C2.

SECOND EMBODIMENT

As shown in FIG. 5, a four-terminal, layered capacitor 31 of a second embodiment of the invention is the same as the capacitor 1 of the first embodiment except for the structure of an internal inductor electrode 32 which is made up of a

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series of segments 32a-32e which are formed in series with a pair of internal capacitor electrodes 33 and 34. The internal inductor electrode 32 includes curved segments 32a, 32b and 32c with extreme outer segments 32d and 32e exposed at left and right edges of the dielectric sheet 2, respectively. The internal capacitor electrode 33 is electrically connected between the curved segments 32a and 32b while the internal capacitor electrode 34 is electrically connected between the curved segments 32b and 32c.

The individual dielectric sheets 2 are stacked in the order shown in FIG. 5, and calcined to form a single laminated body. An external input terminal 36 and external output terminal 37 are formed at left and right end faces of the laminated body while a pair of external ground terminals 38 and 39 are formed at front and rear end faces, respectively, as illustrated in FIG. 6. The external input terminal 36 is electrically connected to the extreme left segment 32d of the internal inductor electrode 3 as well as to the extreme left end 5a of each internal capacitor electrode 5, while the external output terminal 37 is electrically connected to the extreme right segment 32e of the internal inductor electrode 3 as well as to the extreme

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right end 6a of each internal capacitor electrode 6. Further, the external ground terminals 38 and 39 are electrically connected to outer ends 4a and 4b of each internal ground electrode 4, respectively.

The four-terminal, layered capacitor 31 having the above-described structure can be regarded, with reference to its equivalent circuit shown in FIG. 7, as being constructed by separating the single capacitor of the conventional structure (shown in FIG. 10) into a pair of capacitors, that is, a capacitor C1 formed by the internal capacitor electrodes 5 and the internal ground electrodes 4 and a capacitor C2 formed by the internal capacitor electrodes 6 and the internal ground electrodes 4, and then connecting the capacitors C1 and C2 by an LC circuit made up of inductors 32a-32c formed by the internal inductor electrode 32 and capacitors C3 and C4 formed by the internal capacitor electrodes 33, 34 and 4. An advantage of this four-terminal, layered capacitor 31 is that its resonant frequency is even lower than that of the four-terminal, layered capacitor 1 of the first embodiment.

Additional features of the invention are described in further detail in the following with reference to the

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following third embodiment, in which three distinct capacitor elements are formed in a noise-absorbing, ceramic layered capacitor (hereinafter referred to simply as a ceramic layered capacitor).

THIRD EMBODIMENT

FIG. 11 is an exploded perspective view showing the construction of a ceramic layered capacitor 101 according to a third embodiment of the invention; FIG. 12 is a perspective view showing the external appearance of the ceramic layered capacitor 101; FIG. 13 is a cross-sectional diagram showing an internal electrode arrangement including capacitor and inductor element patterns of the ceramic layered capacitor 101; and FIG. 14 is an equivalent circuit of the ceramic layered capacitor 101. To facilitate understanding of the internal electrode arrangement, each layer (plane) containing capacitor and/or inductor element patterns is regarded as a distinct ceramic sheet.

As shown in FIGS. 11 and 12, the ceramic layered capacitor 101 comprises a laminated ceramic body 102 formed by stacking a plurality of ceramic sheets 102a to 102f and four external terminals 103a to 103d fitted to outer surfaces of the laminated ceramic body 102. Additional ceramic sheets

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carrying no electrodes (not shown) are laminated on the top and bottom of the laminated ceramic body 102.

The ceramic layered capacitor 101 contains capacitor element patterns 104a to 104d provided on the ceramic sheets 102a, 102b, 102e and 102f, respectively, to form a capacitor element 104, capacitor element patterns 105a to 105d provided on the same ceramic sheets 102a, 102b, 102e and 102f, respectively, to form a capacitor element 105, and capacitor element patterns 106a and 106b provided on the ceramic sheets 102c and 102d, respectively, to form a capacitor element 106. The individual capacitor element patterns 104a-104d, 105a-105d, 106a and 106b are so arranged that the capacitor elements 104 and 105 have the same value of capacitance and the capacitor element 106 has a smaller value of capacitance compared to the capacitor elements 104 and 105.

The ceramic layered capacitor 101 further contains inductor element patterns 107a to 110a provided on the ceramic sheets 102c and 102d to form four inductor elements 107 to 110 which interconnect the capacitor elements 104, 105 and 106. The individual inductor element patterns 107a to 110a are so arranged that all the inductor elements 107 to 110 have the same inductance.

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As can be seen from the equivalent circuit of the ceramic layered capacitor 101 shown in FIG. 14, the capacitor element 106 is connected to the capacitor element 104 by the inductor elements 107 and 108, and the capacitor element 105 is connected to the capacitor element 106 by the inductor elements 109 and 110 to form together a network in which the individual capacitor elements 104 to 106 are connected in parallel with one another by the inductor elements 107 to 110. The external terminals 103a and 103b are connected to both leads of the capacitor element 104 while the external terminals 103c and 103d are connected to both leads of the capacitor element 105 to complete the four-terminal, ceramic layered capacitor 101.

The ceramic layered capacitor 101 is bidirectional in operation because it has a bilaterally symmetric configuration with the capacitor elements 104 and 105 having the same capacitance located at both ends of the device. More specifically, the ceramic layered capacitor 101 may be connected so that the external terminals 103a and 103b act as input terminals and the external terminals 103c and 103d act as output terminals, or the external terminals 103c and 103d act as input terminals and the external terminals 103a and



103b act as output terminals.

FIG. 15 is a graph representing noise-absorbing characteristics of the ceramic layered capacitor 101 showing a relationship between frequency and attenuation factor. A solid line G1 in the graph shows noise-absorbing characteristics of the whole ceramic layered capacitor 101, an alternate long and short dashed line G2 shows noise-absorbing characteristics of each of the capacitor elements 104 and 105 only, and another alternate long and short dashed line G3 shows noise-absorbing characteristics of the capacitor element 106 only.

It can be seen from FIG. 15 that the ceramic layered capacitor 101 has two prominent attenuation bands F1 and F2. This indicates that the noise-absorbing characteristics of the individual capacitor elements 104, 105 and 106 remain effective in the ceramic layered capacitor 101. According to this embodiment, a single ceramic layered capacitor provides necessary noise-absorbing performance even when electrical noise is present in two separate frequency ranges.

VARIATIONS OF THE EMBODIMENTS

While the invention has been described in conjunction with embodiments thereof, details of the construction of the

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above-described multi-terminal, layered capacitors can be varied in various ways.

As an example, a dielectric sheet which acts as a spacer may be inserted between each internal inductor electrode and internal ground electrode in the aforementioned embodiments to eliminate or reduce stray capacitance appearing between the two electrodes.

In another variation, at least one set of internal inductor electrodes and internal ground electrodes is provided at a specific point in the vertical, or stacking, direction of a multi-terminal, layered capacitor for achieving symmetry in electrode arrangement or for adjusting the inductance component of the layered capacitor.

The foregoing discussion of the embodiments is based on the assumption that each multi-terminal, layered capacitor is manufactured singly. In the case of mass production, a plurality of multi-terminal, layered capacitors can be produced at once by making a large substrate having the layer structure as described above and then cutting it into chips of a desired size.

Although the capacitors of the aforementioned embodiments are made by stacking a plurality of dielectric

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sheets and calcining the stack, the invention is not limited to this construction. In one alternative, the individual dielectric sheets may be calcined before stacking. In another alternative, the layer structure of dielectric sheets and electrodes of each capacitor may be produced by alternately applying and drying pasty dielectric and conductive materials by using a printing technique, for instance.

In the first and second embodiments, each of the internal ground electrodes 4 need not necessarily be made of a single electrode element but may be divided into two separate parts as shown in FIG. 16.

Although there are produced three capacitor elements 104, 105 and 106 in the third embodiment described above, the embodiment may be modified to form two capacitor elements, or four or more capacitor elements, interconnected by as many inductor elements as necessary, within the scope of the invention.

The invention is not limited to the aforementioned preferred embodiments and the variations thereof in other respects as well. Shapes and arrangements of the individual capacitor element patterns, inductor element patterns and



external terminals may be altered or modified without departing from the spirit and scope of the invention.

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WHAT IS CLAIMED IS:

1. A multi-terminal, layered capacitor with a plurality of dielectric sheets, said dielectric sheets comprising:

an external input terminal;

an external output terminal;

an external ground terminal;

a first internal capacitor electrode electrically connected to said external input terminal;

a second internal capacitor electrode electrically connected to said external output terminal;

an internal ground electrode electrically connected to said external ground terminal, said internal ground electrode producing a capacitance between said first internal capacitor electrode and said internal ground electrode and another capacitance between said second internal capacitor electrode and said internal ground electrode; and

an internal inductor electrode electrically connected between said external input terminal and said external output terminal, wherein said plurality of dielectric sheets are stacked integrally.

2. A four-terminal, layered capacitor with a plurality

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of dielectric sheets, said dielectric sheets comprising:

an external input terminal;

an external output terminal;

a pair of external ground terminals;

a first internal capacitor electrode electrically connected to said external input terminal;

a second internal capacitor electrode electrically connected to said external output terminal;

an internal ground electrode electrically connected to said pair of external ground terminals, said internal ground electrode producing a capacitance between said first internal capacitor electrode and said internal ground electrode and another capacitance between said second internal capacitor electrode and said internal ground electrode; and

an internal inductor electrode electrically connected between said external input terminal and said external output terminal,

wherein said plurality of dielectric sheets are stacked integrally.

3. A four-terminal layered capacitor according to claim 2, wherein said internal ground electrode comprises a pair of

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* C L M S *



internal ground electrode members each connected to a respective one of said external ground terminals.

4. A four-terminal, layered capacitor according to claim 2, wherein said internal inductor electrode has a curved segment and a third internal capacitor electrode which forms a third capacitance with said internal ground electrode.

5. A noise-absorbing, ceramic layered capacitor comprising a plurality of internal electrodes embedded in a ceramic body, said internal electrodes including:

capacitor element patterns arranged to form a plurality of capacitor elements having different values of capacitance; and

inductor element patterns forming inductor elements which interconnect said capacitor elements in parallel with one another via said inductor elements in a plurality of stages,

wherein said ceramic body is formed by stacking a plurality of dielectric sheets.

6. A noise-absorbing, ceramic layered capacitor

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according to claim 5, further comprising a plurality of external terminals connected respectively to said capacitor elements.

7. A noise-absorbing, ceramic layered capacitor according to claim 6, wherein said capacitor element patterns are arranged in such a way that one of said capacitor elements has a smaller value of capacitance than the remainder thereof.

8. A noise-absorbing, ceramic layered capacitor according to claim 5, wherein said capacitor element patterns are arranged in such a way that one of said capacitor elements has a smaller value of capacitance than the remainder thereof.



* C L M S *

10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31. 32. 33. 34. 35. 36. 37. 38. 39. 40. 41. 42. 43. 44. 45. 46. 47. 48. 49. 50. 51. 52. 53. 54. 55. 56. 57. 58. 59. 60. 61. 62. 63. 64. 65. 66. 67. 68. 69. 70. 71. 72. 73. 74. 75. 76. 77. 78. 79. 80. 81. 82. 83. 84. 85. 86. 87. 88. 89. 90. 91. 92. 93. 94. 95. 96. 97. 98. 99. 100. 101. 102. 103. 104. 105. 106. 107. 108. 109. 110. 111. 112. 113. 114. 115. 116. 117. 118. 119. 120. 121. 122. 123. 124. 125. 126. 127. 128. 129. 130. 131. 132. 133. 134. 135. 136. 137. 138. 139. 140. 141. 142. 143. 144. 145. 146. 147. 148. 149. 150. 151. 152. 153. 154. 155. 156. 157. 158. 159. 160. 161. 162. 163. 164. 165. 166. 167. 168. 169. 170. 171. 172. 173. 174. 175. 176. 177. 178. 179. 180. 181. 182. 183. 184. 185. 186. 187. 188. 189. 190. 191. 192. 193. 194. 195. 196. 197. 198. 199. 200. 201. 202. 203. 204. 205. 206. 207. 208. 209. 210. 211. 212. 213. 214. 215. 216. 217. 218. 219. 220. 221. 222. 223. 224. 225. 226. 227. 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LAYERED CAPACITORS

ABSTRACT OF THE DISCLOSURE

Multi-terminal, layered capacitors having excellent attenuation characteristics over a wide frequency range. A four-terminal, layered capacitor has a dielectric sheet with an internal inductor electrode connecting an external input terminal to an external output terminal, dielectric sheets with internal capacitor electrodes connected to the external input terminal, and internal capacitor electrodes connected to the external output terminal, and dielectric sheets with internal ground electrodes connected to external ground terminals. All these dielectric sheets are integrally stacked and calcined to form a one-piece structure.

Fig. 1

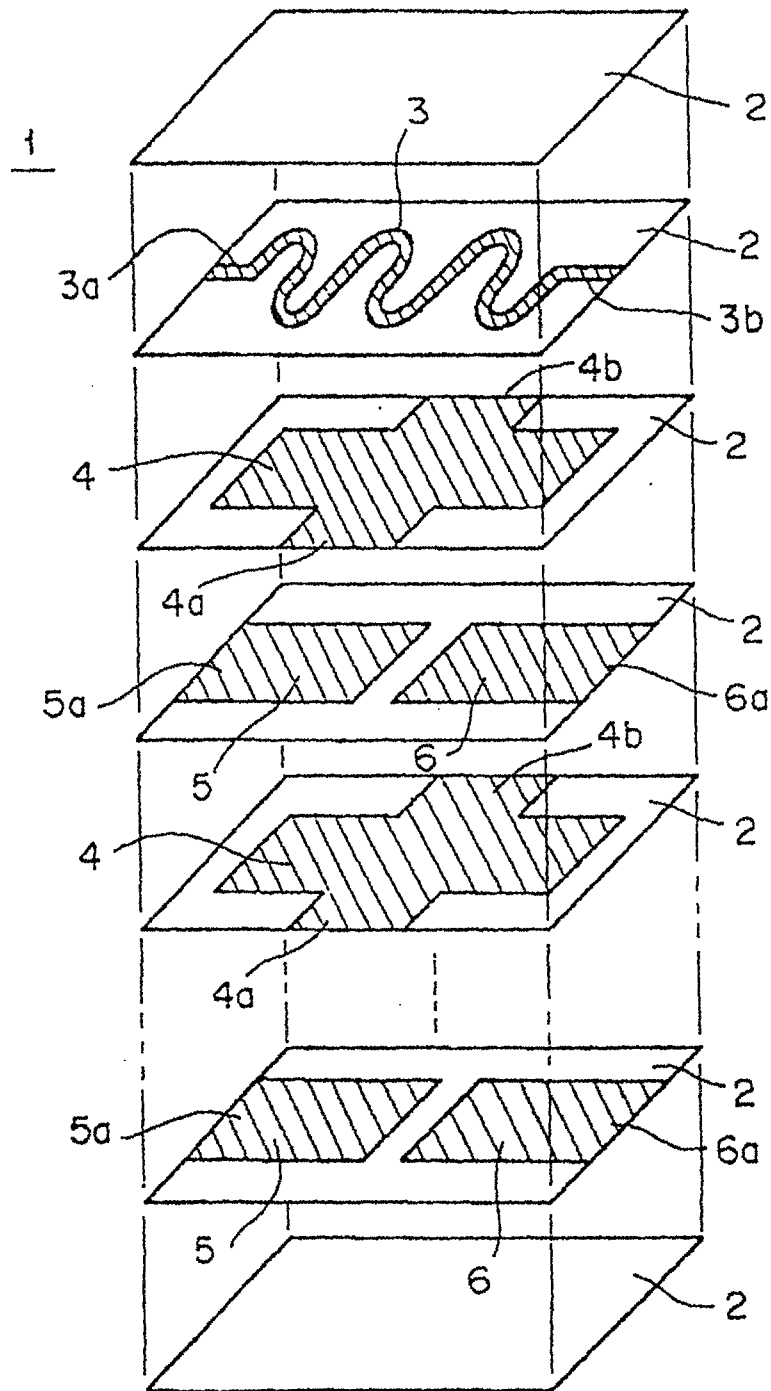
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FIG. 1



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2 FIG. 2

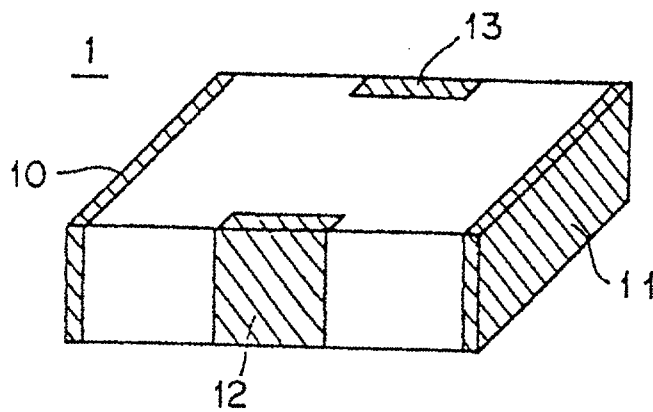


FIG. 3

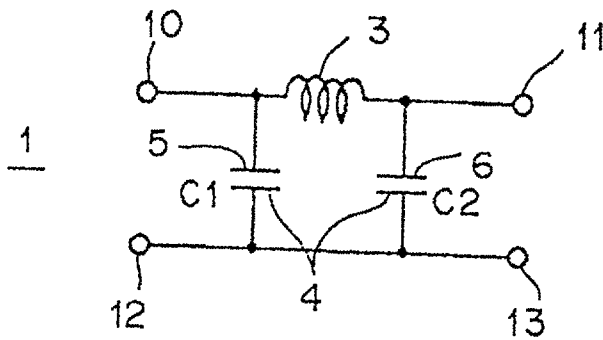
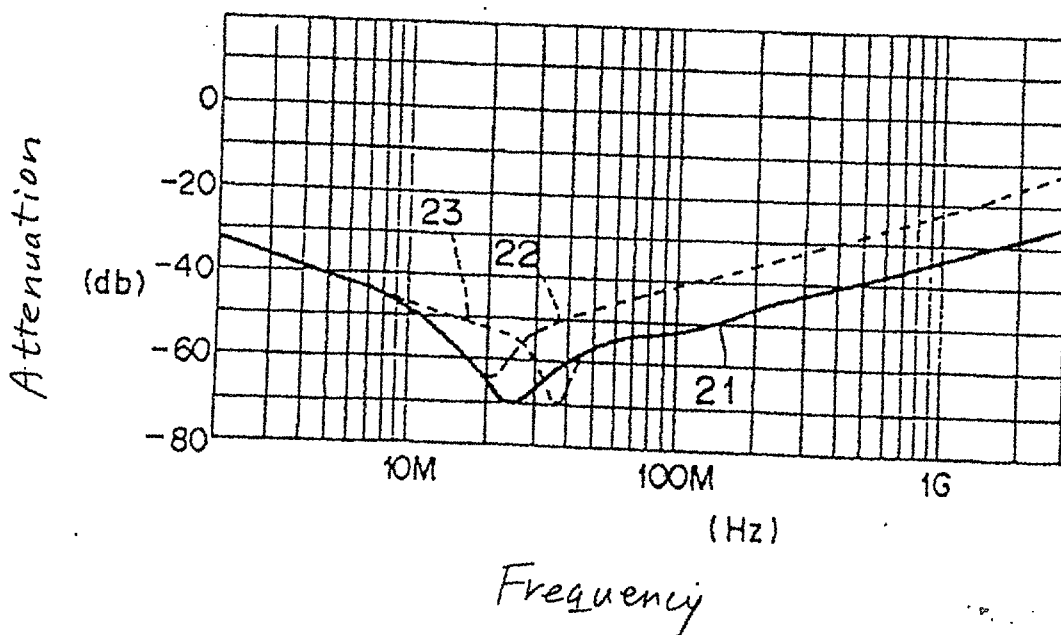
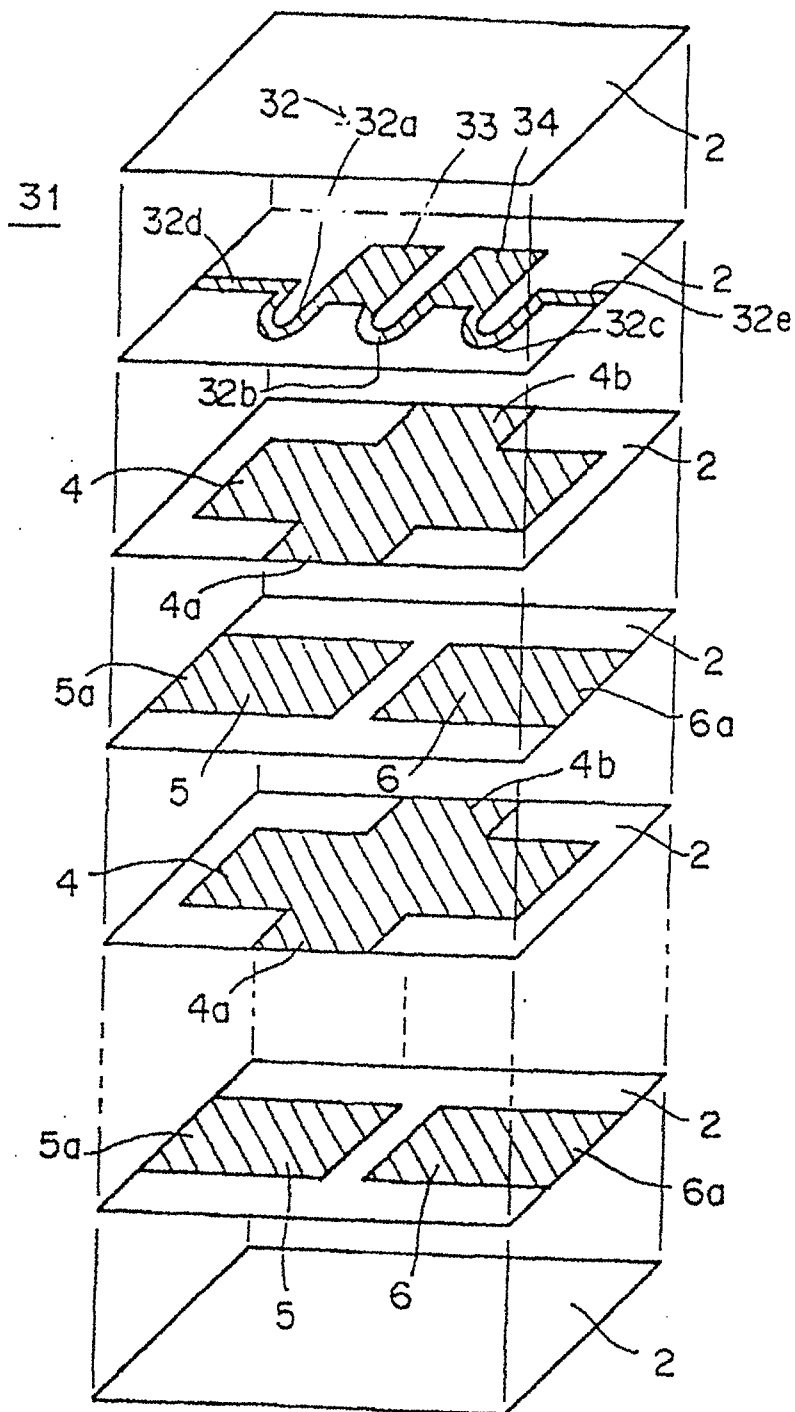


FIG. 4



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FIG. 5



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FIG. 6

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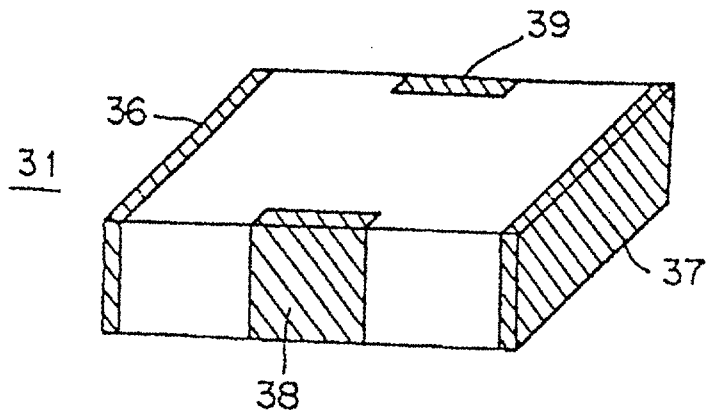
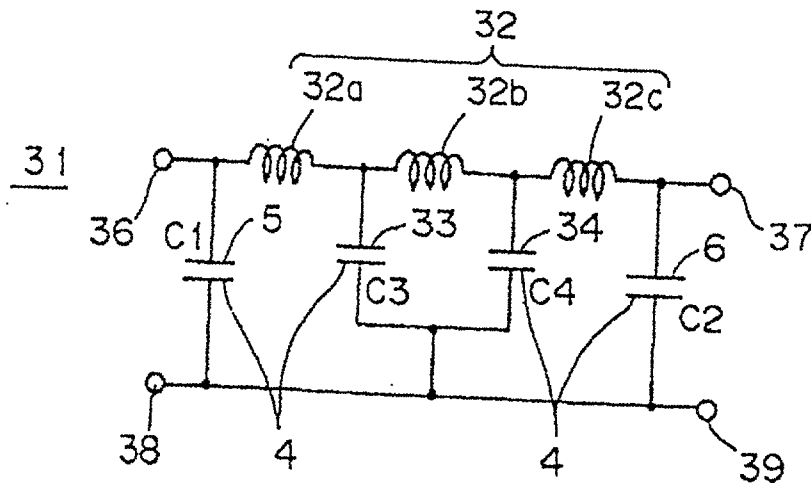


FIG. 7



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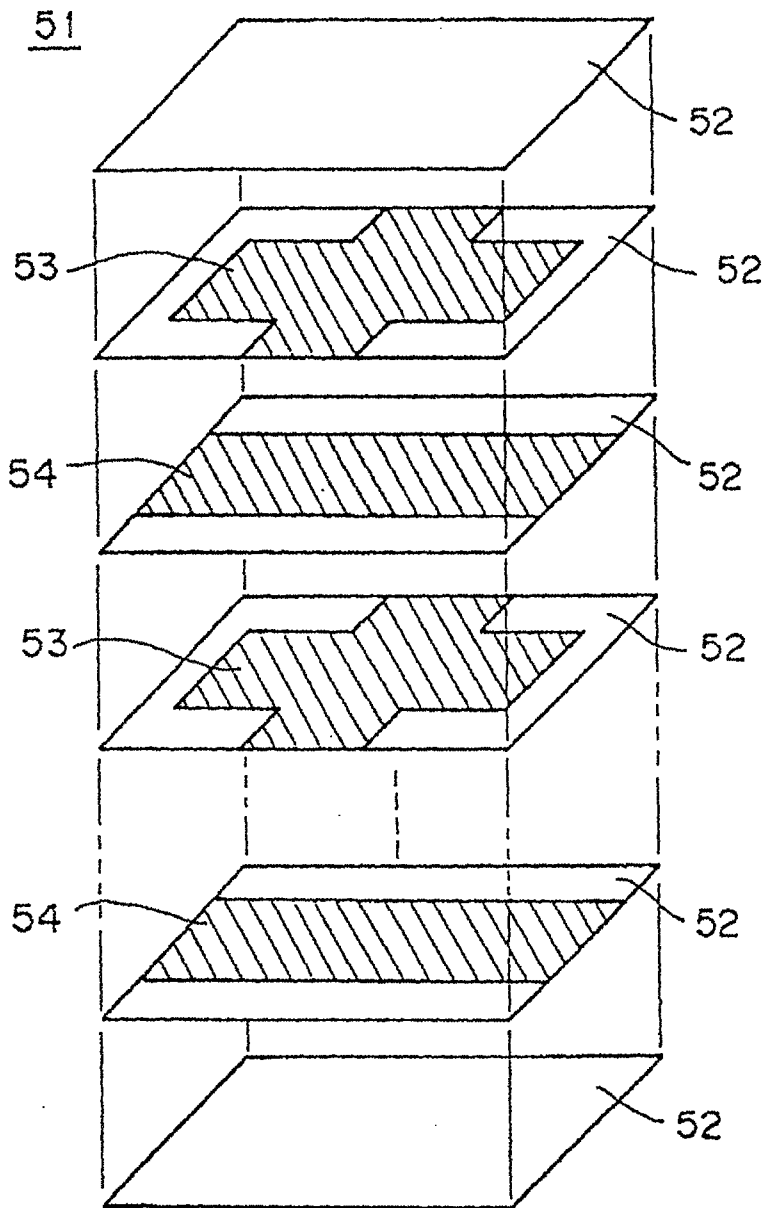


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FIG. 8

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FIG. 9

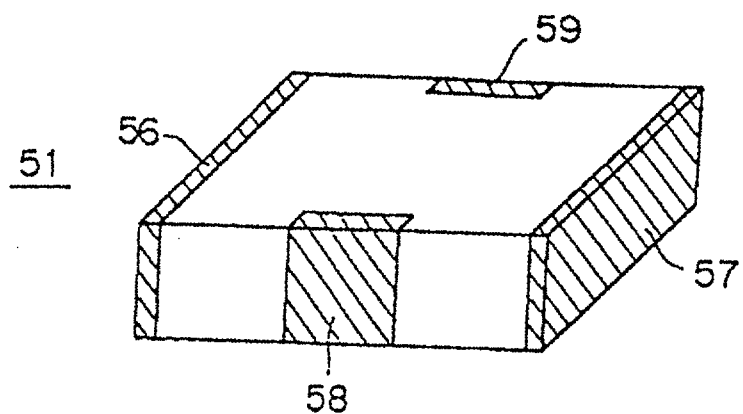
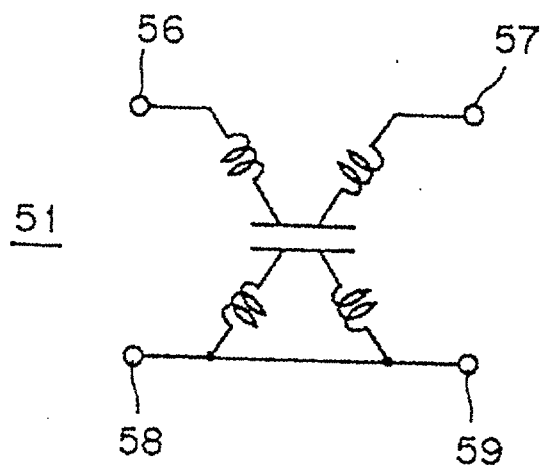


FIG. 10



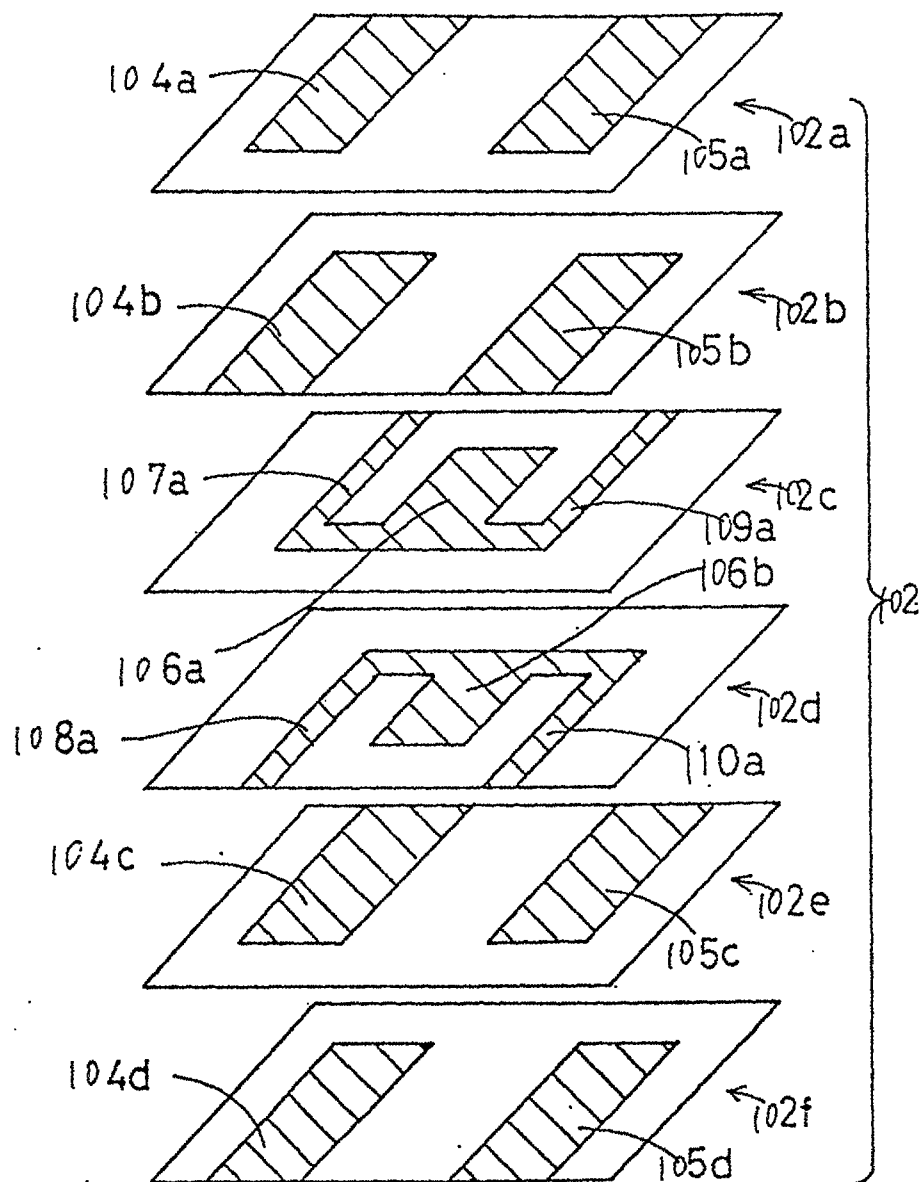
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FIG. 11

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FIG. 12

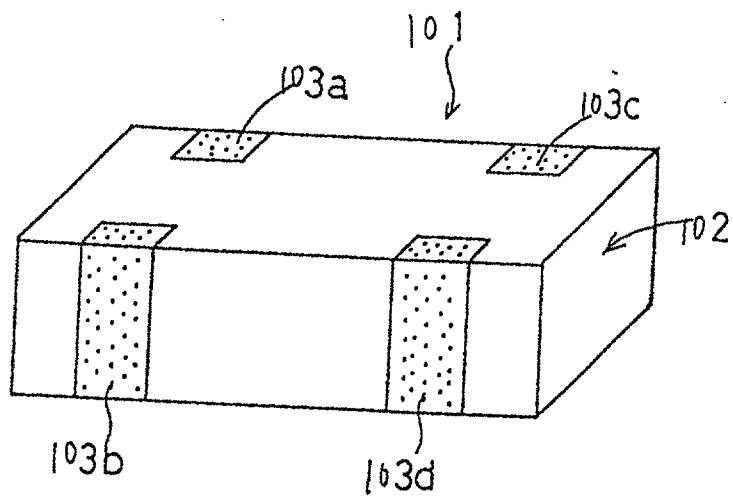


FIG. 13

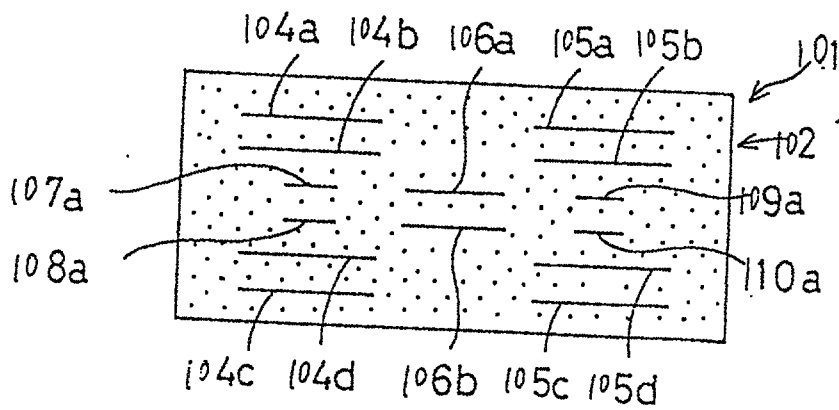
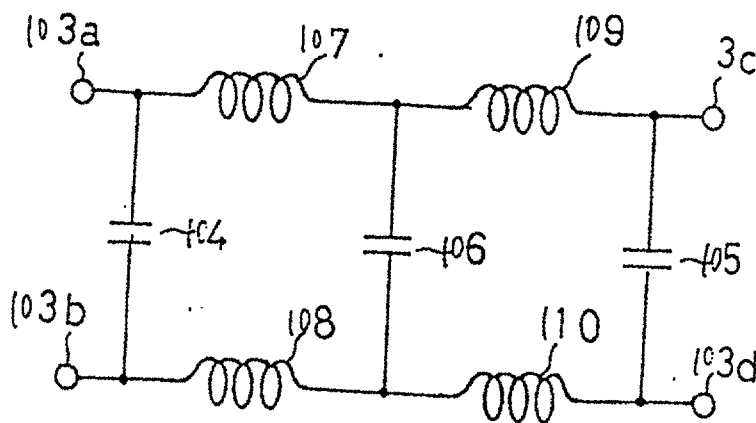


FIG. 14



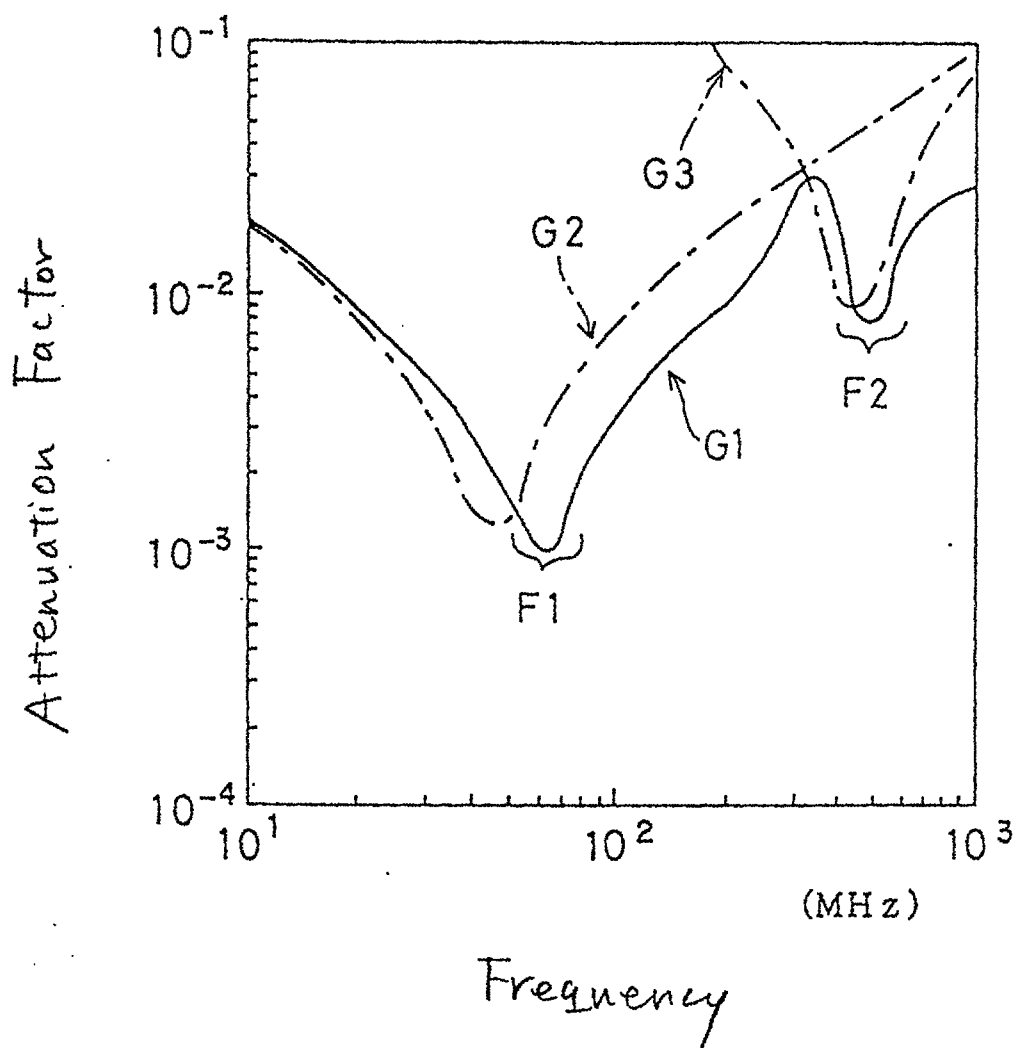
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FIG. 15



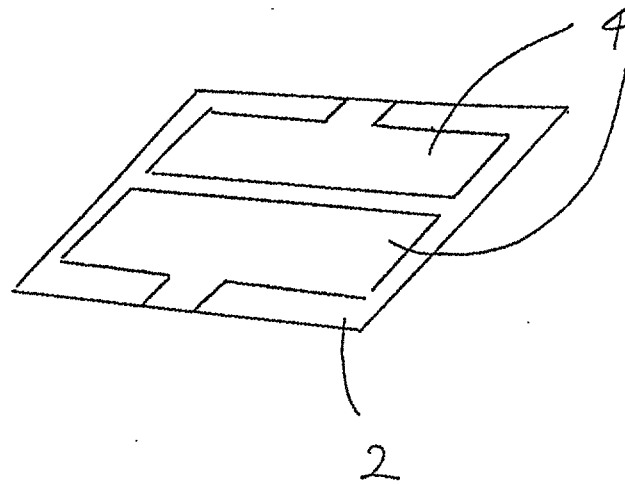
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FIG. 16



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| REPLACEMENT SHEETS | | SG |
|---|------------------------|----|
| ☒ Description : | paged 01 to paged 19 | |
| ☒ Claim(s) : | paged 20 to paged 23 | |
| ☒ Drawing(s) : | paged 01 to paged 10 | |
| ☒ Abstract : | paged 24 to paged | |
| DATE OF RECEIPT 07/07/97 | | |

1

LAYERED CAPACITORS

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

The present invention relates generally to layered capacitors and, more particularly, to multi-terminal, layered capacitors and noise-absorbing, ceramic layered capacitors which are used for reducing or eliminating electrical noise in electronic apparatus, for instance.

2. Description of the Related Art

Two-terminal and four-terminal, layered capacitors are commonly used for reducing or eliminating electrical noise in various electronic apparatus. As shown in FIG. 8, a conventional four-terminal, layered capacitor 51 comprises dielectric sheets 52 carrying internal ground electrodes 53 on their surfaces, dielectric sheets 52 carrying internal capacitor electrodes 54 on their surfaces, and outermost protective dielectric sheets 52.

The individual dielectric sheets 52 are stacked one on top of another and calcined as a whole to form the capacitor

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51 shown in FIG. 9. An external input terminal 56 and external output terminal 57 are formed at opposite end faces of the capacitor 51 while a pair of external ground terminals 58 and 59 are formed at its front and rear end faces, respectively, as illustrated in FIG. 9. FIG. 10 is an equivalent circuit of the capacitor 51. The four-terminal, layered capacitor 51 of this kind has a higher resonant frequency than conventional two-terminal, layered capacitors of the type having a plurality of internal electrodes on respective dielectric layers which are connected alternately to respective input and output end electrodes. Also, in general they provide high attenuation in a high-frequency range.

Although the conventional four-terminal, layered capacitors 51 generally offer high attenuation factors at high frequencies, the amount of attenuation they achieve is lower than that of two-terminal, layered capacitors around the resonant frequencies of the two-terminal, layered capacitors.

SUMMARY OF THE INVENTION

The invention provides multi-terminal, layered capacitors having excellent, improved attenuation

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characteristics even at resonant frequencies of the known two-terminal, layered capacitors while maintaining a high attenuation capability in high-frequency ranges.

To achieve this, a multi-terminal, layered capacitor according to an aspect of the invention comprises a first internal capacitor electrode electrically connected to an external input terminal, a second internal capacitor electrode electrically connected to an external output terminal, an internal ground electrode electrically connected to an external ground terminal to produce a capacitance between the first internal capacitor electrode and the internal ground electrode and another capacitance between the second internal capacitor electrode and the internal ground electrode, and an internal inductor electrode electrically connected between the external input terminal and the external output terminal.

Provided with the internal inductor electrode, first and second internal capacitor electrodes and internal ground electrode, the aforementioned multi-terminal, layered capacitor of the invention forms a circuit configured with two separate capacitor elements and an inductor element. The layered capacitor thus constructed provides a lower resonant

frequency than the conventional four-terminal, layered capacitors while maintaining a high-frequency attenuation capability comparable to the latter. As a result, it becomes possible to produce a four-terminal, layered capacitor featuring excellent attenuation characteristics over a wide frequency range.

A noise-absorbing, ceramic layered capacitor according to a second aspect of the invention comprises a plurality of internal electrodes embedded in a ceramic body, the internal electrodes including capacitor element patterns arranged in such a way that a plurality of capacitor elements are formed and inductor element patterns forming inductor elements, whereby a circuit in which the capacitor elements are connected in parallel with one another by the inductor elements in a plurality of stages is formed.

Preferably the plurality of capacitor elements provide different values of capacitance in the above noise-absorbing, ceramic layered capacitor of the invention. Thus, it is possible to absorb electrical noise in specific frequency bands corresponding to the respective values of capacitance of the capacitor elements. It is therefore apparent that this noise-absorbing, ceramic layered capacitor provides

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desired noise-absorbing performance even when the electrical noise is present in a plurality of frequency bands.

Furthermore, the necessary noise-absorbing performance is obtainable without increasing the number of components since the individual capacitor elements and inductor elements of the noise-absorbing, ceramic layered capacitor of the invention are integrally stacked into a one-piece structure.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an exploded perspective view of a four-terminal, layered capacitor according to a first embodiment of the invention;

FIG. 2 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 1;

FIG. 3 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 2;

FIG. 4 is a graph representing attenuation characteristics of the four-terminal, layered capacitor of

FIG. 2;

FIG. 5 is an exploded perspective view of a four-terminal, layered capacitor according to a second embodiment of the invention;

FIG. 6 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 5;

FIG. 7 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 6;

FIG. 8 is an exploded perspective view of a conventional four-terminal, layered capacitor;

FIG. 9 is a perspective view showing the external appearance of the four-terminal, layered capacitor shown in FIG. 8;

FIG. 10 is an equivalent circuit of the four-terminal, layered capacitor shown in FIG. 9;

FIG. 11 is an exploded perspective view of a ceramic layered capacitor according to a third embodiment of the invention;

FIG. 12 is a perspective view showing the external appearance of the ceramic layered capacitor of the third embodiment;

FIG. 13 is a cross-sectional diagram showing an internal electrode arrangement of the ceramic layered capacitor of the third embodiment;

FIG. 14 is an equivalent circuit of the ceramic layered capacitor of the third embodiment;

FIG. 15 is a graph representing noise-absorbing characteristics of the ceramic layered capacitor of the third embodiment; and

FIG. 16 is a perspective view of an internal ground electrode which is used in a four-terminal, ceramic layered capacitor according to a variation of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Multi-terminal, layered capacitors according to embodiments of the invention are now described in detail with reference to the accompanying drawings, in which like elements and assemblies are designated by like reference numbers.

FIRST EMBODIMENT

As shown in FIG. 1, a four-terminal, layered capacitor 1 of a first embodiment comprises a dielectric sheet 2 carrying an internal inductor electrode 3 on its surface, dielectric sheets 2 carrying internal ground electrodes 4 on

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their surfaces, dielectric sheets 2 carrying internal capacitor electrodes 5 and 6 on their surfaces, and outermost protective dielectric sheets 2. Each dielectric sheet 2 is made of a ceramic material, for example.

The internal inductor electrode 3 is generally patterned to form a sinuous shape with its extreme left segment 3a and extreme right segment 3b exposed at left and right edges of the dielectric sheet 2, respectively. The internal capacitor electrodes 5 are located on the left side of the individual dielectric sheets 2 with extreme left ends 5a of the internal capacitor electrodes 5 exposed at left edges of the dielectric sheets 2, while the internal capacitor electrodes 6 are located on the right side of the individual dielectric sheets 2 with extreme right ends 6a of the internal capacitor electrodes 6 exposed at right edges of the dielectric sheets 2. The electrodes 3 to 6 are layers of silver (Ag), silver-palladium alloy (Ag-Pd) or Nickel (Ni), for example, formed by using a technique such as printing, sputtering or vacuum evaporation.

All the dielectric sheets 2 are stacked in the order shown in FIG. 1, and calcined to form a single laminated body. As illustrated in FIG. 2, an external input terminal

10 and external output terminal 11 are formed at left and right end faces of the laminated body while a pair of external ground terminals 12 and 13 are formed at front and rear end faces, respectively. The external input terminal 10 is electrically connected to the extreme left segment 3a of the internal inductor electrode 3 as well as to the extreme left end 5a of each internal capacitor electrode 5, while the external output terminal 11 is electrically connected to the extreme right segment 3b of the internal inductor electrode 3 as well as to the extreme right end 6a of each internal capacitor electrode 6. Further, the external ground terminals 12 and 13 are electrically connected to outer ends 4a and 4b of each internal ground electrode 4, respectively.

The four-terminal, layered capacitor 1 having the above-described structure can be regarded, with reference to its equivalent circuit shown in FIG. 3, as being constructed by separating a single capacitor of the conventional structure (shown in FIG. 10) into a pair of capacitors, that is, a capacitor C1 formed by the internal capacitor electrodes 5 and the internal ground electrodes 4 and a capacitor C2 formed by the internal capacitor electrodes 6 and the internal ground electrodes 4, and then connecting the

capacitors C1 and C2 by means of the internal inductor electrode 3.

A curve (solid line 21) shown in FIG. 4 represents measured attenuation characteristics of the four-terminal, layered capacitor 1, of which capacitance is $0.15 \mu\text{F}$ in this embodiment. FIG. 4 also shows for comparison attenuation characteristics of a conventional two-terminal, layered capacitor (dotted line 22) and of a conventional four-terminal, layered capacitor (dotted line 23), both having the same value of capacitance as the four-terminal, layered capacitor 1 of the first embodiment. As can be seen from FIG. 4, the four-terminal, layered capacitor 1 of the first embodiment has a lower resonant frequency than the conventional four-terminal, layered capacitor due to the inductance of the internal inductor electrode 3, and has greater attenuation over a wider frequency range due to the capacitors C1 and C2.

SECOND EMBODIMENT

As shown in FIG. 5, a four-terminal, layered capacitor 31 of a second embodiment of the invention is the same as the capacitor 1 of the first embodiment except for the structure of an internal inductor electrode 32 which is made up of a

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series of segments 32a-32e which are formed in series with a pair of internal capacitor electrodes 33 and 34. The internal inductor electrode 32 includes curved segments 32a, 32b and 32c with extreme outer segments 32d and 32e exposed at left and right edges of the dielectric sheet 2, respectively. The internal capacitor electrode 33 is electrically connected between the curved segments 32a and 32b while the internal capacitor electrode 34 is electrically connected between the curved segments 32b and 32c.

The individual dielectric sheets 2 are stacked in the order shown in FIG. 5, and calcined to form a single laminated body. An external input terminal 36 and external output terminal 37 are formed at left and right end faces of the laminated body while a pair of external ground terminals 38 and 39 are formed at front and rear end faces, respectively, as illustrated in FIG. 6. The external input terminal 36 is electrically connected to the extreme left segment 32d of the internal inductor electrode 3 as well as to the extreme left end 5a of each internal capacitor electrode 5, while the external output terminal 37 is electrically connected to the extreme right segment 32e of the internal inductor electrode 3 as well as to the extreme

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right end 6a of each internal capacitor electrode 6. Further, the external ground terminals 38 and 39 are electrically connected to outer ends 4a and 4b of each internal ground electrode 4, respectively.

The four-terminal, layered capacitor 31 having the above-described structure can be regarded, with reference to its equivalent circuit shown in FIG. 7, as being constructed by separating the single capacitor of the conventional structure (shown in FIG. 10) into a pair of capacitors, that is, a capacitor C1 formed by the internal capacitor electrodes 5 and the internal ground electrodes 4 and a capacitor C2 formed by the internal capacitor electrodes 6 and the internal ground electrodes 4, and then connecting the capacitors C1 and C2 by an LC circuit made up of inductors 32a-32c formed by the internal inductor electrode 32 and capacitors C3 and C4 formed by the internal capacitor electrodes 33, 34 and 4. An advantage of this four-terminal, layered capacitor 31 is that its resonant frequency is even lower than that of the four-terminal, layered capacitor 1 of the first embodiment.

Additional features of the invention are described in further detail in the following with reference to the

following third embodiment, in which three distinct capacitor elements are formed in a noise-absorbing, ceramic layered capacitor (hereinafter referred to simply as a ceramic layered capacitor).

THIRD EMBODIMENT

FIG. 11 is an exploded perspective view showing the construction of a ceramic layered capacitor 101 according to a third embodiment of the invention; FIG. 12 is a perspective view showing the external appearance of the ceramic layered capacitor 101; FIG. 13 is a cross-sectional diagram showing an internal electrode arrangement including capacitor and inductor element patterns of the ceramic layered capacitor 101; and FIG. 14 is an equivalent circuit of the ceramic layered capacitor 101. To facilitate understanding of the internal electrode arrangement, each layer (plane) containing capacitor and/or inductor element patterns is regarded as a distinct ceramic sheet.

As shown in FIGS. 11 and 12, the ceramic layered capacitor 101 comprises a laminated ceramic body 102 formed by stacking a plurality of ceramic sheets 102a to 102f and four external terminals 103a to 103d fitted to outer surfaces of the laminated ceramic body 102. Additional ceramic sheets

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carrying no electrodes (not shown) are laminated on the top and bottom of the laminated ceramic body 102.

The ceramic layered capacitor 101 contains capacitor element patterns 104a to 104d provided on the ceramic sheets 102a, 102b, 102e and 102f, respectively, to form a capacitor element 104, capacitor element patterns 105a to 105d provided on the same ceramic sheets 102a, 102b, 102e and 102f, respectively, to form a capacitor element 105, and capacitor element patterns 106a and 106b provided on the ceramic sheets 102c and 102d, respectively, to form a capacitor element 106. The individual capacitor element patterns 104a-104d, 105a-105d, 106a and 106b are so arranged that the capacitor elements 104 and 105 have the same value of capacitance and the capacitor element 106 has a smaller value of capacitance compared to the capacitor elements 104 and 105.

The ceramic layered capacitor 101 further contains inductor element patterns 107a to 110a provided on the ceramic sheets 102c and 102d to form four inductor elements 107 to 110 which interconnect the capacitor elements 104, 105 and 106. The individual inductor element patterns 107a to 110a are so arranged that all the inductor elements 107 to 110 have the same inductance.

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As can be seen from the equivalent circuit of the ceramic layered capacitor 101 shown in FIG. 14, the capacitor element 106 is connected to the capacitor element 104 by the inductor elements 107 and 108, and the capacitor element 105 is connected to the capacitor element 106 by the inductor elements 109 and 110 to form together a network in which the individual capacitor elements 104 to 106 are connected in parallel with one another by the inductor elements 107 to 110. The external terminals 103a and 103b are connected to both leads of the capacitor element 104 while the external terminals 103c and 103d are connected to both leads of the capacitor element 105 to complete the four-terminal, ceramic layered capacitor 101.

The ceramic layered capacitor 101 is bidirectional in operation because it has a bilaterally symmetric configuration with the capacitor elements 104 and 105 having the same capacitance located at both ends of the device. More specifically, the ceramic layered capacitor 101 may be connected so that the external terminals 103a and 103b act as input terminals and the external terminals 103c and 103d act as output terminals, or the external terminals 103c and 103d act as input terminals and the external terminals 103a and

103b act as output terminals.

FIG. 15 is a graph representing noise-absorbing characteristics of the ceramic layered capacitor 101 showing a relationship between frequency and attenuation factor. A solid line G1 in the graph shows noise-absorbing characteristics of the whole ceramic layered capacitor 101, an alternate long and short dashed line G2 shows noise-absorbing characteristics of each of the capacitor elements 104 and 105 only, and another alternate long and short dashed line G3 shows noise-absorbing characteristics of the capacitor element 106 only.

It can be seen from FIG. 15 that the ceramic layered capacitor 101 has two prominent attenuation bands F1 and F2. This indicates that the noise-absorbing characteristics of the individual capacitor elements 104, 105 and 106 remain effective in the ceramic layered capacitor 101. According to this embodiment, a single ceramic layered capacitor provides necessary noise-absorbing performance even when electrical noise is present in two separate frequency ranges.

VARIATIONS OF THE EMBODIMENTS

While the invention has been described in conjunction with embodiments thereof, details of the construction of the

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above-described multi-terminal, layered capacitors can be varied in various ways.

As an example, a dielectric sheet which acts as a spacer may be inserted between each internal inductor electrode and internal ground electrode in the aforementioned embodiments to eliminate or reduce stray capacitance appearing between the two electrodes.

In another variation, at least one set of internal inductor electrodes and internal ground electrodes is provided at a specific point in the vertical, or stacking, direction of a multi-terminal, layered capacitor for achieving symmetry in electrode arrangement or for adjusting the inductance component of the layered capacitor.

The foregoing discussion of the embodiments is based on the assumption that each multi-terminal, layered capacitor is manufactured singly. In the case of mass production, a plurality of multi-terminal, layered capacitors can be produced at once by making a large substrate having the layer structure as described above and then cutting it into chips of a desired size.

Although the capacitors of the aforementioned embodiments are made by stacking a plurality of dielectric

sheets and calcining the stack, the invention is not limited to this construction. In one alternative, the individual dielectric sheets may be calcined before stacking. In another alternative, the layer structure of dielectric sheets and electrodes of each capacitor may be produced by alternately applying and drying pasty dielectric and conductive materials by using a printing technique, for instance.

In the first and second embodiments, each of the internal ground electrodes 4 need not necessarily be made of a single electrode element but may be divided into two separate parts as shown in FIG. 16.

Although there are produced three capacitor elements 104, 105 and 106 in the third embodiment described above, the embodiment may be modified to form two capacitor elements, or four or more capacitor elements, interconnected by as many inductor elements as necessary, within the scope of the invention.

The invention is not limited to the aforementioned preferred embodiments and the variations thereof in other respects as well. Shapes and arrangements of the individual capacitor element patterns, inductor element patterns and

external terminals may be altered or modified without departing from the spirit and scope of the invention.

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WHAT IS CLAIMED IS:

1. A multi-terminal, layered capacitor with a plurality of dielectric sheets, said dielectric sheets comprising:

an external input terminal;

an external output terminal;

an external ground terminal;

a first internal capacitor electrode electrically connected to said external input terminal;

a second internal capacitor electrode electrically connected to said external output terminal;

an internal ground electrode electrically connected to said external ground terminal, said internal ground electrode producing a capacitance between said first internal capacitor electrode and said internal ground electrode and another capacitance between said second internal capacitor electrode and said internal ground electrode; and

an internal inductor electrode electrically connected between said external input terminal and said external output terminal, wherein said plurality of dielectric sheets are stacked integrally.

2. A four-terminal, layered capacitor with a plurality

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of dielectric sheets, said dielectric sheets comprising:

an external input terminal;

an external output terminal;

a pair of external ground terminals;

a first internal capacitor electrode electrically connected to said external input terminal;

a second internal capacitor electrode electrically connected to said external output terminal;

an internal ground electrode electrically connected to said pair of external ground terminals, said internal ground electrode producing a capacitance between said first internal capacitor electrode and said internal ground electrode and another capacitance between said second internal capacitor electrode and said internal ground electrode; and

an internal inductor electrode electrically connected between said external input terminal and said external output terminal,

wherein said plurality of dielectric sheets are stacked integrally.

3. A four-terminal layered capacitor according to claim 2, wherein said internal ground electrode comprises a pair of



internal ground electrode members each connected to a respective one of said external ground terminals.

4. A four-terminal, layered capacitor according to claim 2, wherein said internal inductor electrode has a curved segment and a third internal capacitor electrode which forms a third capacitance with said internal ground electrode.

5. A noise-absorbing, ceramic layered capacitor comprising a plurality of internal electrodes embedded in a ceramic body, said internal electrodes including:

capacitor element patterns arranged to form a plurality of capacitor elements having different values of capacitance; and

inductor element patterns forming inductor elements which interconnect said capacitor elements in parallel with one another via said inductor elements in a plurality of stages,

wherein said ceramic body is formed by stacking a plurality of dielectric sheets.

6. A noise-absorbing, ceramic layered capacitor



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according to claim 5, further comprising a plurality of external terminals connected respectively to said capacitor elements.

7. A noise-absorbing, ceramic layered capacitor according to claim 6, wherein said capacitor element patterns are arranged in such a way that one of said capacitor elements has a smaller value of capacitance than the remainder thereof.

8. A noise-absorbing, ceramic layered capacitor according to claim 5, wherein said capacitor element patterns are arranged in such a way that one of said capacitor elements has a smaller value of capacitance than the remainder thereof.



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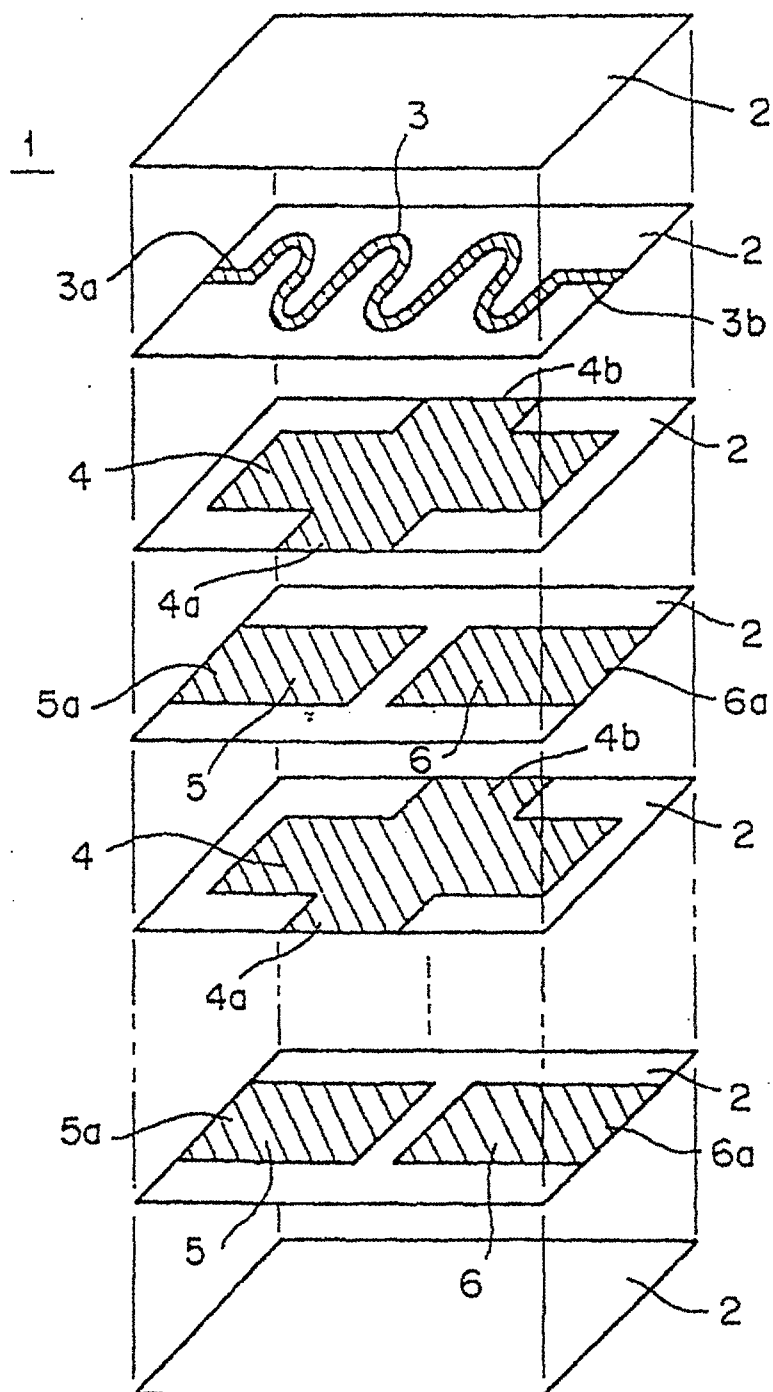
LAYERED CAPACITORS

ABSTRACT OF THE DISCLOSURE

Multi-terminal, layered capacitors having excellent attenuation characteristics over a wide frequency range. A four-terminal, layered capacitor has a dielectric sheet with an internal inductor electrode connecting an external input terminal to an external output terminal, dielectric sheets with internal capacitor electrodes connected to the external input terminal, and internal capacitor electrodes connected to the external output terminal, and dielectric sheets with internal ground electrodes connected to external ground terminals. All these dielectric sheets are integrally stacked and calcined to form a one-piece structure.

Fig 1

Fig 1



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Fig 2

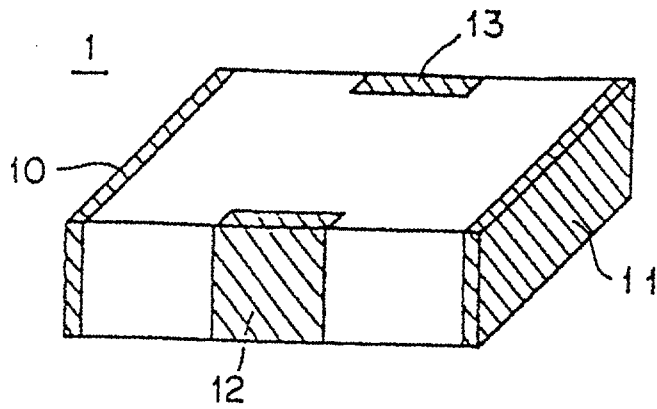


Fig 3

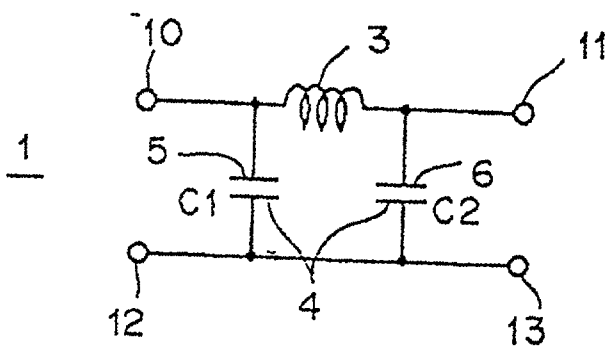
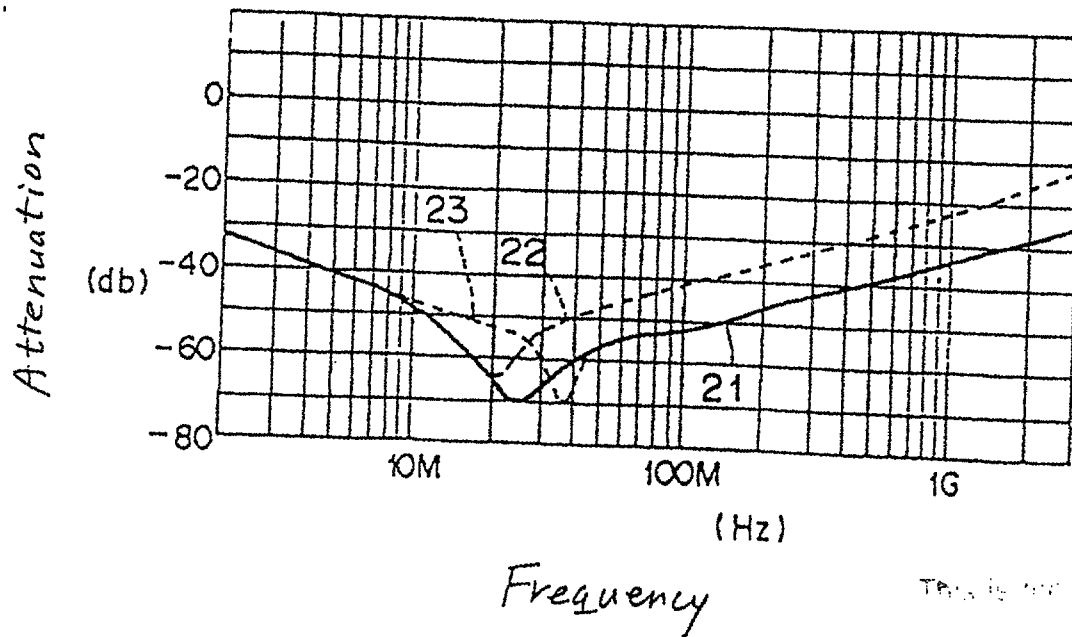


Fig 4



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Fig 5

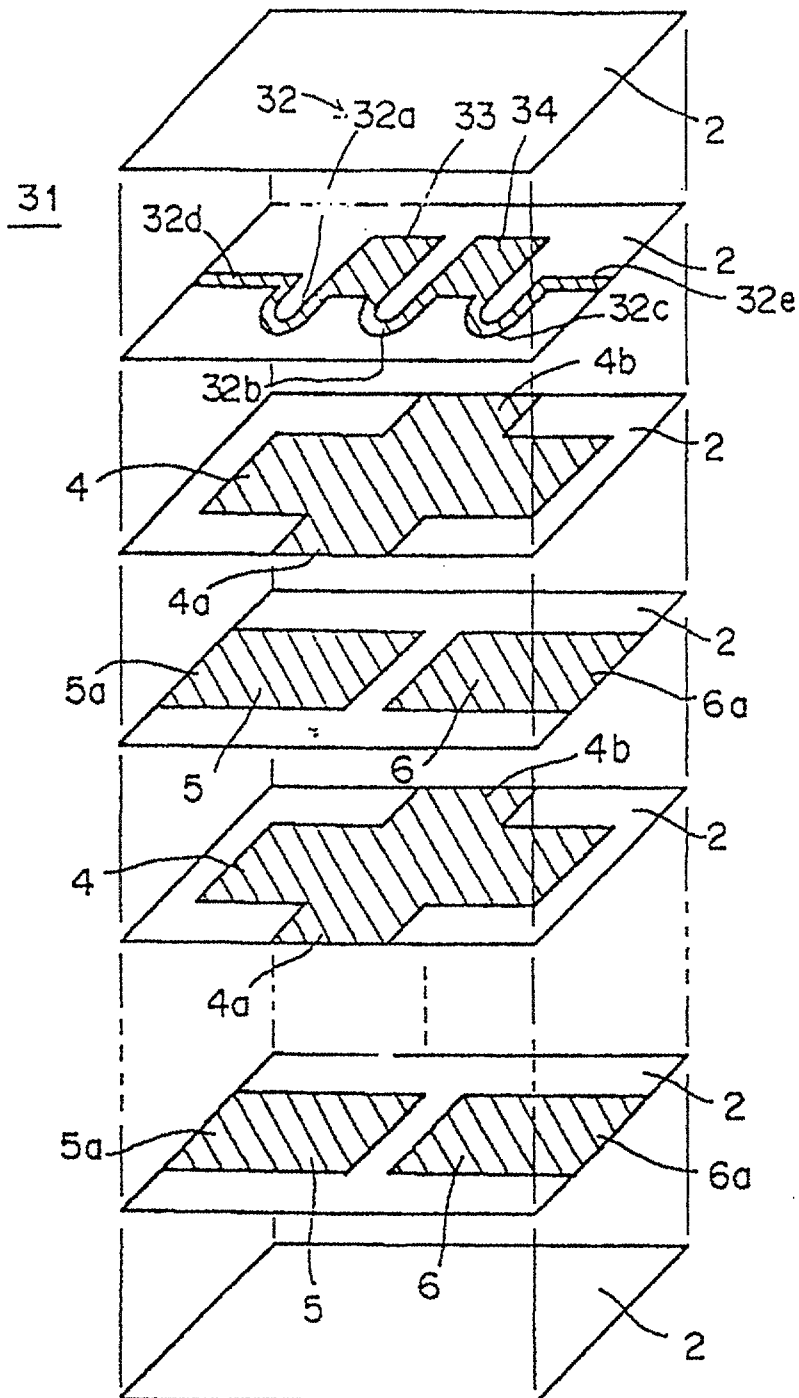
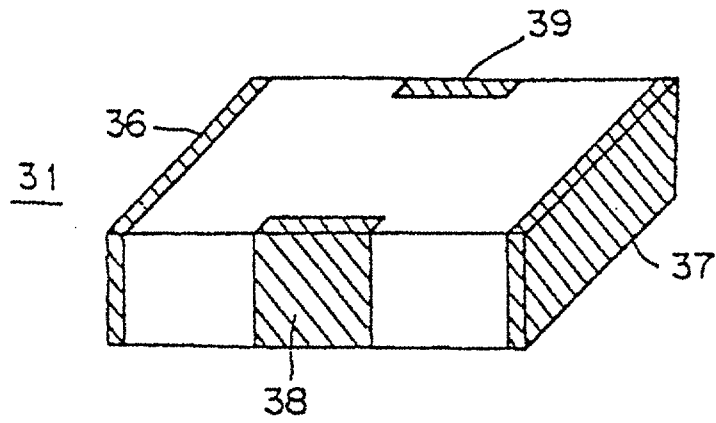
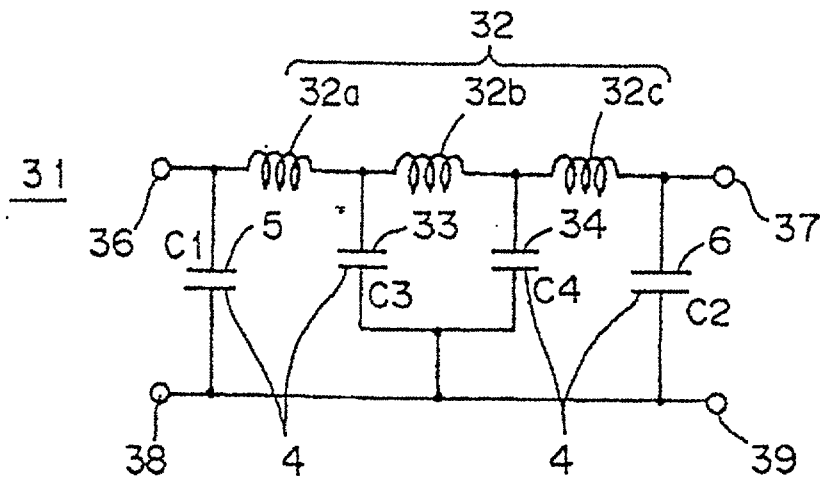
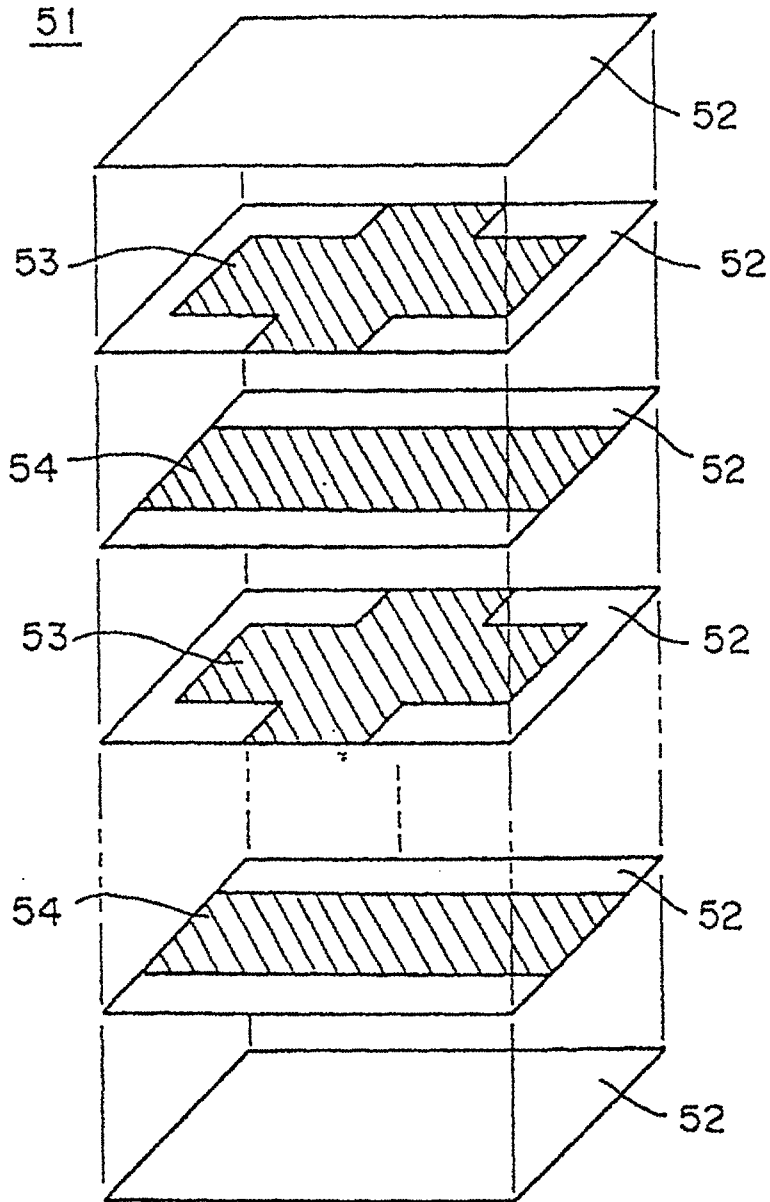


Fig 6Fig 7

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Fig 8

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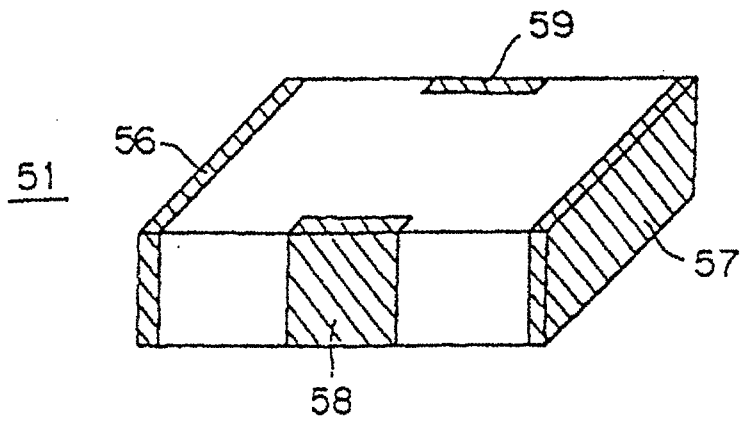
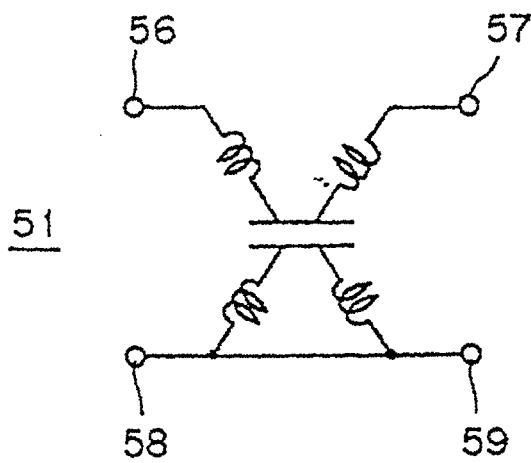
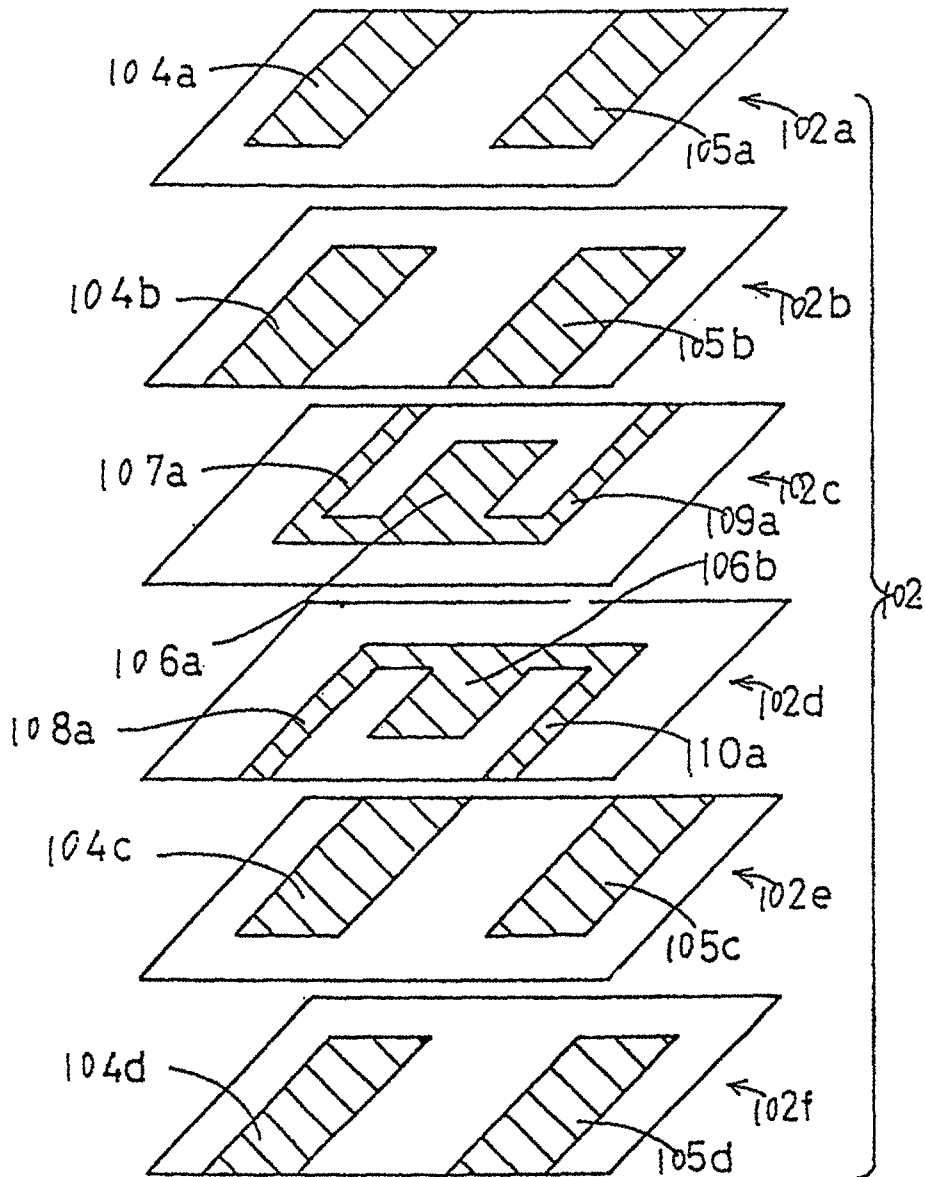
Fig 9Fig 10

Fig 11

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Fig 12

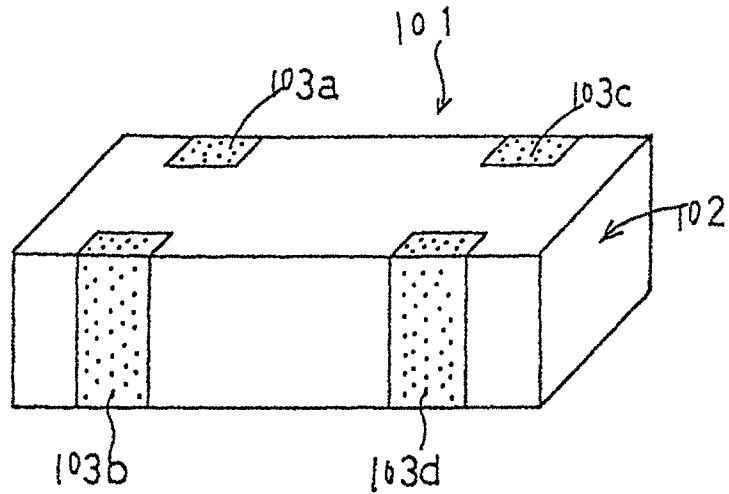


Fig 13

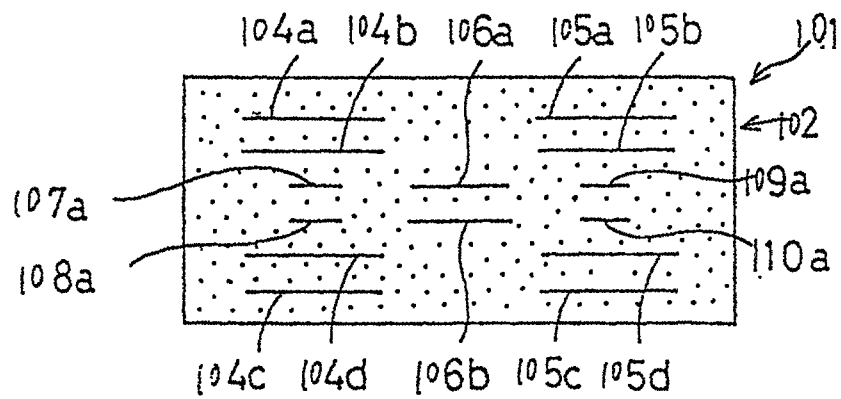
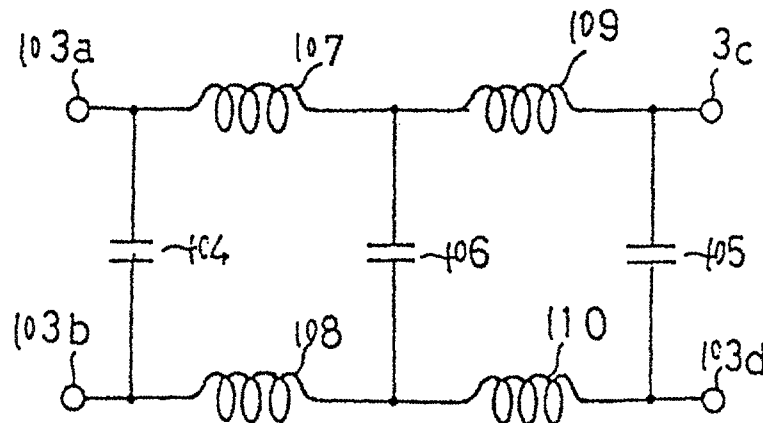


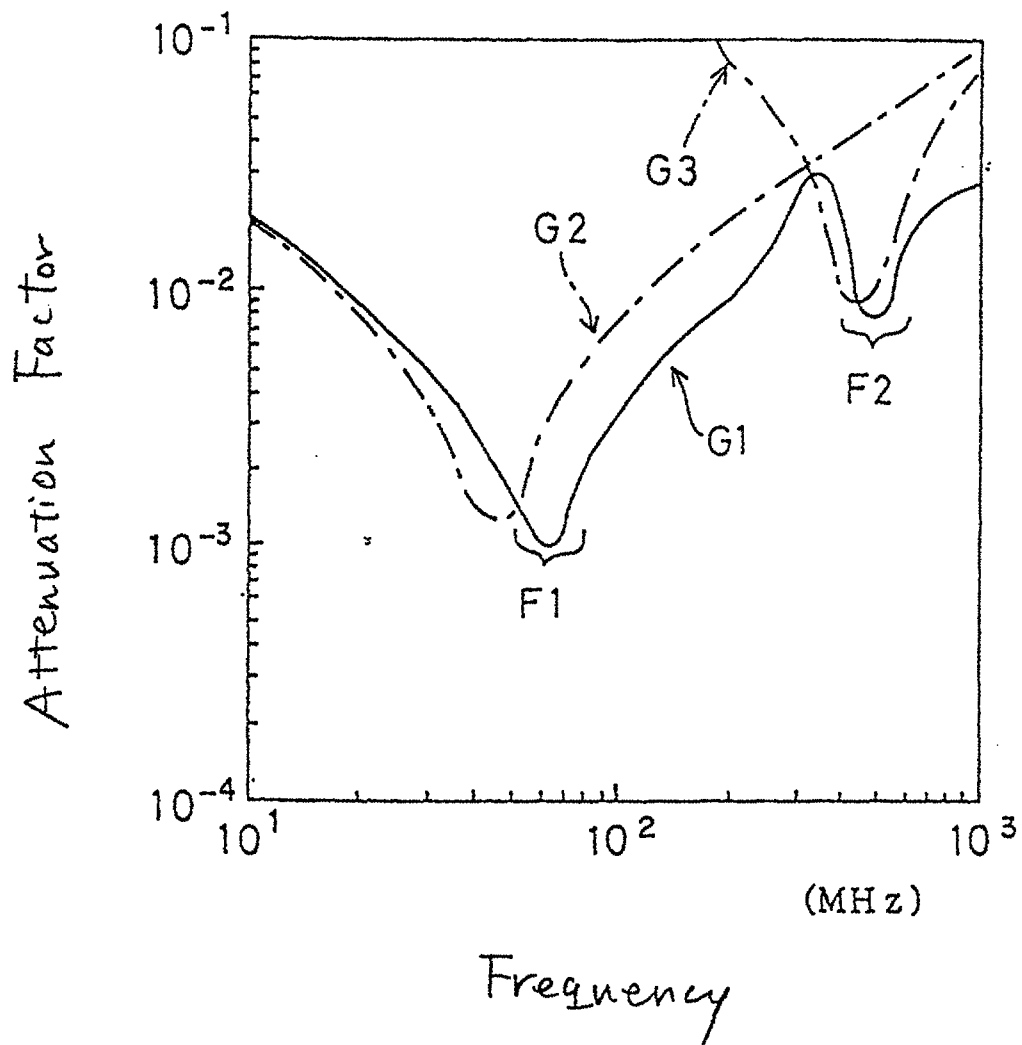
Fig 14



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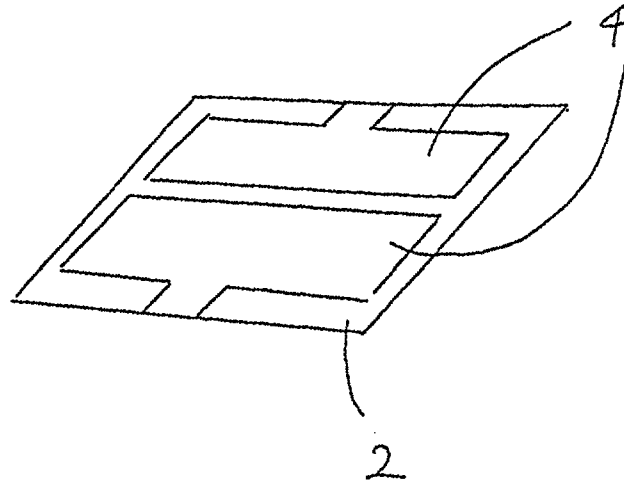
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Fig 15



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Fig 16

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