

Method and circuit arrangement for assuring the bit synchronization of a data block in a receiver.

The invention relates to a method of ensuring synchronization of a data block in a receiver as defined in the preamble of Patent Claim 1.

In digital information systems operating with block-wise transmission of information, the receiver has to be synchronized with the transmitter, so that a common
5 starting instant for the two arrangements is established. For synchronizing the receiver with the transmitter, a specific bit pattern can be produced in the transmitter and transmitted to the receiver. The receiver derives a criterion for establishing the starting instant by correlating the received data signal with a stored data signal.

If, as frequently happens with radio transmission links, interference in the
10 transmission path causes bit errors to occur that lead to relatively high bit error rates, the received bit pattern cannot always be recognized if one or more bits of the pattern are distorted on the transmission path.

Such a bit pattern which precedes the data block proper is, for example, a first bit sequence of alternating half-bits for determining the bit clock for the bits of the
15 data block and a second bit sequence for determining the block synchronization by correlation with the bit sequence stored in the receiver.

German Patent DE-PS 22 19 016 has disclosed a method of synchronizing the clock phase in a receiver with the phase position of the bit clock of a received data block; for simultaneously determining the bit clock and the block synchronization
20 according to this method, the bit sequence is applied to N correlators arranged in parallel whose associated shift registers are controlled by mutually offset shift-clock pulse sequences.

Recovering the bit clock and the block synchronization from the received data signal is hampered by the influence of noise voltages, transients and fading and the
25 phase jitter resulting therefrom, so that the phase synchronization is relatively inaccurate or unattainable within a relatively short time interval. Furthermore, the circuit implementation is relatively complex owing to the correlator bank and, without further measures, it is not possible to determine the instant at which correlation signals have to

be evaluated, for example, to avoid erroneous synchronization due to noise.

In addition, published German Patent Application DE-OS 30 12 075 discloses a circuit arrangement for bit synchronization, in which also the bit clock is derived from the received data signal. For this purpose, the overall phase range of the individual bits (from 0 to 360 degrees) is divided into sub-intervals (so-called phase windows). During a measuring interval the number of occurrences of the instantaneous phase values assigned to sub-intervals are stored (by means of edge counters). The number of sub-intervals (phase windows) is determined by a divider circuit in combination with AND circuits. These circuits produce pulse sequences that are phase-shifted according to the reciprocal value of the number of different phase windows.

Counters are connected to the outputs of these circuits in order to count the number of edges of the received data signal that have fallen in the associated sub-interval (phase window). At the end of the measuring interval the phase of the bit clock is corrected by an estimated phase value corresponding to the phase value of the sub-interval having the largest number of edges.

For this purpose, at the end of the measuring interval a higher bit clock is applied to the counters *via* a divider circuit and change-over switches whereby the up-counting is accelerated. Owing to the phase-shifted pulse sequences there will always be only a single counter that reaches the maximum count, and by means of a subsequent code converter a binary number, which is then stored in a memory, can be assigned to the count. Switching-over and reading-out the stored binary number that corresponds to the sub-interval having the largest number of edges and hence to the phase-synchronous bit clock, is controlled by a control logic and the received bit clock is corrected according to the estimated value of the phase.

Such a circuit arrangement has the disadvantage that, as a consequence of the recovery of the bit clock from the received data signal, the phase jitter of this data signal, *i.e.* the fluctuation of its significant instants around instants that are equidistant ideally, has its effect on the determination of the estimated phase value. More specifically in radio transmission links frequent re-synchronizations will be required as the bit error rate will adopt inadmissibly high values as a result of fading.

The invention has for its object to provide a method of ensuring bit synchronisation of a data block so that phase fluctuations do not affect the determination of the bit clock and the method can also be used for various types of modulation of the

data signals.

This object is achieved by a method in accordance with the invention which has the features specified in the characterizing part of Patent Claim 1.

As compared with the methods known from German Patent documents
5 DE-PS 22 19 016 and DE-OS 30 12 075, the method according to the invention has the advantage that it is independent of the modulation method for the data signals. Compared with the circuit arrangement according to DE-OS 30 12 075, the circuit arrangement implementing the method in accordance with the invention requires only a low degree of circuit complexity. Since the bit clock is obtained from a comparison of
10 the first bit sequence with alternating sample values of a predeterminable minimum number during a predeterminable time interval, fluctuations resulting from phase jitter hardly have any effect on the determination of the bit clock. During the comparison process, a shift of the predeterminable time interval (time window) can be made, so that a short clock drop-out does not entail an interruption of the synchronization process.

15 Compared with the method known from DE-PS 22 19 016, the method in accordance with the invention has the advantage that on the basis of the determined bit clock the bit synchronism can subsequently be checked with a second bit sequence to determine the block synchronization.

The method as claimed in Patent Claim 2 has the advantage that due to
20 the determination of the mean phase value it is possible to make a shift of the sampling instant to the centre position in between the edges of the data block bits.

The circuit arrangement as claimed in Patent Claim 3 for implementing the method requires only a low degree of circuit complexity and can be integrated in a simple way.

25 The invention will be further described hereinafter with reference to the embodiment of the invention shown in the drawing in which:

Figure 1 shows an embodiment of a circuit for implementing the method in accordance with the invention;

Figure 2 shows time diagrams of signals in the embodiment of Figure 1 in
30 the case of undisturbed synchronization; and

Figure 3 shows time diagrams of signals in the embodiment of Figure 1 in the case of a disturbed synchronization process.

The method according to the invention is described and explained for the

case where it is used in a cordless telephone set. In cordless telephone sets, the transmission of information between a base station and the associated mobile station is effected through a radio channel. The base station is connected to a public office line or to a private branch exchange by means of a connector box, so that the customer is given
5 access to the public telephone network. Owing to the fact that the base station and the mobile station are interconnected through a radio channel, the user's range of free movement relative to the fixed connector box in question is increased by approximately 200 metres.

In the Federal Republic of Germany 40 radio channels are available for
10 the transmission of information, which channels lie in the 900 MHz frequency range. If one wishes to set up a connection, a search for an idle radio transmission channel is started and the channel is seized. In the mobile station, the search for a radio channel is initiated by operating the cradle-switch. In order to ensure that messages to be transmitted between the mobile station and the base station cannot be overheard by any
15 other adjacent cordless telephone set and/or to guarantee the allocation of charges, the two stations each have a code arrangement, in which the code in the mobile station and the base station is set-bound and independent of the subscriber's number of the telephone user. During the search for an idle radio channel and the subsequent setting up of a radio connection identification numbers are exchanged between the two stations.

20 When a connection is set up, one of the two stations seizes a radio transmission channel that is found to be idle, activates the transmitter and transmits its identification number as a data telegram through this radio transmission channel. After each transmission of such a data telegram an acknowledgement telegram from the associated opposite station is waited for. The called station scans all radio transmission
25 channels for data telegrams and sends back an acknowledgement telegram to the calling station when a data telegram containing an identification number is received that is identical with its assigned identification number.

The above telegrams contain various bit sequences which are transmitted consecutively. A first bit sequence of alternating half bits consists of, for example, 16
30 bits and is used for determining the bit clock in the stations. Subsequently, a second bit sequence for achieving block synchronization is transmitted, which second sequence is, for example, 8 bits long and has the channel number as its information content. By using the channel number for block synchronization, the beginning of the subsequent

data block is recognized and, on the other hand, it is avoided that in the case of favourable field strength conditions the receiving station locks on to an adjacent channel having an adequate field strength level. The data block comprises, for example, 20 bits and contains, for example, the identification number during the setting up of the radio connection. A check sequence can further be added to this data block, which sequence is used for detecting and correcting bit errors in the useful information, for which purpose, *e.g.* a matrix-parity-check method can be used for the 12 bits of the check sequence.

During the conversation an inaudible exchange of identification numbers between the two stations can take place, in which the telegram is transmitted as inaudible out-of-band signalling. Because the data telegram, as already mentioned, contains the first bit sequence, bit synchronization is ensured during the conversation too.

The bit synchronization can also be effected by means of a program-controlled control arrangement provided both in the base station and in the mobile station of the cordless telephone set.

The method according to the invention will be further described with reference to the embodiment of a control arrangement shown in Figure 1, in which components of the two stations that are not essential for comprehending the invention have not been shown.

The clock of a clock generator TG is applied to N delay elements V1, ..., VN arranged in parallel. For the clock generation, it is also possible to utilize the internal clock of a microprocessor that is arranged in the two stations. The output of each delay element V1, ..., VN is connected to the clock input of a first D flip-flop D1, ..., DN. The data input of each of these first D flip-flops D1, ..., DN is connected to the inverting output. The non-inverting output of each first D flip-flop D1, ..., DN is connected to a first input of an Exclusive-OR circuit A1, ..., AN. The telegram is applied to the second input of each Exclusive-OR circuit A1, ..., AN. The output of each Exclusive-OR circuit A1, ..., AN is connected to the data input of a second D flip-flop D11, ..., D1N, whose clock input is connected to the output of the respective delay element V1, ..., VN. The output of each second D flip-flop D11, ..., D1N is connected to both the inverting input and the non-inverting input of a mono-stable flip-flop M1, ..., MN. The output of each mono-stable flip-flop M1, ..., MN is connected to the reset

input of a first counter $Z_1, \dots, Z_N$. The clock input of each counter $Z_1, \dots, Z_N$ is connected to the output of its associated delay element $V_1, \dots, V_N$.

The operation of the circuit arrangement according to Figure 1 will be further described hereinafter with reference to the time diagrams shown in Figure 2. At instant t_0 each one of the first D flip-flops $D_1, \dots, D_N$ is in the "1" state. The first D flip-flops $D_1, \dots, D_N$ effect a frequency division in the ratio 1:2 of the phase-shifted clock $T_1, \dots, T_N$ available at the output of the delay elements $V_1, \dots, V_N$. The signal A at the output of the first D flip-flop $D_1, \dots, D_N$ gives the expected state of the digital signal RxD .

In the Exclusive-OR circuits $A_1, \dots, A_N$, this expected state as given by the signal A is compared with the actual state of the digital signal RxD and the signal B at the output of the Exclusive-OR circuit $A_1, \dots, A_N$ is in its "1" state only if one of the respective two signals A and RxD is detected as being in the "1" state.

By means of the second D flip-flop $D_{11}, \dots, D_{1N}$ the result of this comparison is stored at the edge instant of the clock signal T at the output of the delay elements $V_1, \dots, V_N$. If the signal E at the output of the second D flip-flops $D_{11}, \dots, D_{1N}$ has a constant significant state during the predeterminable time interval (measuring interval), the monostable flip-flop $M_1, \dots, M_N$ is not triggered and the counter $Z_1, \dots, Z_N$ increments.

As the synchronizing bits (first bit sequence) have a transition in the centre of the bit interval, a certain number of "1" samples and "0" samples will occur during the sampling of the first bit sequence, irrespective of the phase position of the sampling pulse of the clock $T_1, \dots, T_N$. The number of respective sample changes is counted by the counters $Z_1, \dots, Z_N$ and as soon as one of these counters $Z_1, \dots, Z_N$ indicates the predeterminable minimum number, this clock is utilized as the phase-synchronous clock.

If, for example, the first bit sequence is sampled by means of three phase-shifted clocks $T_1, \dots, T_3$ of equal clock frequency, and if the phase position of one clock coincides with the transition edge in the centre of the synchronizing bit, this clock will not satisfy the requirement of the alternating "0" and "1" levels and will therefore not be utilized as the phase synchronous bit clock. On the other hand, the two remaining clocks are situated at a distance of 60° to the central transition edge of the synchronizing bit, so that one of the two clocks can be utilized as a phase-synchronous

bit clock.

If one of the counters Z1, ..., ZN reaches the predeterminable minimum value, the actual counts of the other counters can be checked. If three counters Z1, Z2, Z3 are used, different cases may arise.

5 On the basis of the actual counts there can be assumed that a short time afterwards the two other counters will exceed the predeterminable minimum value, so that each of the three clocks can be utilized as the phase-synchronous bit clock. A further improvement of the phase position can be achieved without modifying the method in accordance with the invention.

10 If only one counter is expected to reach the predeterminable minimum value a short time afterwards, the mean phase value of the two clocks can be determined from the clock phases for improving the phase position, and the clock having the mean phase value can be utilized as the phase-synchronous bit clock. If it is to be expected that neither of the two counters reaches the predeterminable minimum
15 value, the bit clock assigned to the first counter will be utilized as the phase--synchronous bit clock.

If, for example, the number of synchronizing bits is 16, the minimum number of the alternating "0" and "1" levels occurring in an uninterrupted sequence can be set at 25.

20 Figure 3 shows the synchronizing process in the case of a disturbance. At instant t1 a disturbance occurs to the effect that the "expected" signal A and the received signal RxD have different significant states. The signal E changes to the "1" state, triggering, for example, the monostable flip-flop M1 and resetting the counter Z1. If the counter Z1 reaches the predeterminable count during the measuring interval, the
25 bit clock assigned to the counter Z1 can be utilized as the phase-synchronous bit clock in spite of the disturbance.

The synchronizing method according to the invention can also be used in the case where the significant states of the "expected" signal A and the received digital signal RxD are always unequal during the predeterminable time interval (measuring
30 interval).

If the clock is derived from the internal clock of a microprocessor (program-controlled control arrangement), the minimal spacing of consecutive interrupts for 32 clock cycles of $2.5/\mu\text{s}$ each amounts to $80/\mu\text{s}$ when using 6 MHz quartz crystal.

This interrupt spacing of $80/\mu\text{s}$ is increased to double its length for reasons of processing and this clock is utilized for sampling the telegram. In order to achieve a subdivision of the phase range in a phase interval (sub-interval) of 60 degrees, at least 3 clocks are required that are distributed evenly over the phase range of the bits. The bit
5 length of the synchronizing bits in this case is $960/\mu\text{s}$.

CLAIMS:

1. Method of ensuring bit synchronization of a data block in a receiver, according to which method there are transmitted consecutively and prior to the data block: a first bit sequence of alternating "0" and "1" levels for determining the bit clock for the bits of a data block and a second bit sequence for determining the block synchronization by correlation with a bit sequence stored in the receiver, characterized in that the first bit sequence is sampled with N phase-shifted clocks (T1, ..., TN) of equal clock frequency that are generated in the receiver, whereby the overall phase range of the individual bit intervals is divided into sub-intervals, and in that such clock (T1, ..., TN) is utilized as the phase-synchronous bit clock, for which the number of changes of sample values the first bit sequence can be established as having a predetermined minimum value during a predetermined time-interval.
 2. Method as claimed in Claim 1, characterized in that for clocks (T1, ..., TN) having the same number of changes of sample values a mean phase value is determined from the clock phases and the clock having the mean phase value is utilized as the phase-synchronous bit clock.
 3. Receiver comprising a circuit arrangement for bit synchronization of an input signal (RxD), which signal contains at least a data block, the following means being included in the receiver:
 - means (TG, V1, ..., VN) for producing n phase-shifted clock signals having the same clock frequency, for sampling the input signal (RxD)
 - means (Z1, ..., ZN) for counting a specific sampling state for each of the n phase-shifted sampled input signals
 - means for evaluating the counting means for determining the phase-shifted clock signal which is the most suitable for sampling a data block,
- characterized
- in that the means (TG, V1, ..., VN), provided for producing the n clock frequencies, produce this clock signal independently of the input signal clock, and



- in that further means (D1, ..., DN, A1, ..., AN, D11, ..., D11N) are provided, which do not increment the associated counting means (Z1, ..., ZN) until a change of the sampling state can be detected between one sampling instant and the next for the associated sampled input signal.

5 4. Receiver as claimed in Claim 3, characterized

- in that the means for evaluating the counting means (Z1, ..., ZN) are provided for the purpose of determining a mean value from a plurality of clock signals that have been found to be equally suitable, and
- in that means are provided which produce a clock signal for sampling the data block, whose phase shift corresponds to this mean clock signal.

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5. Receiver as claimed in Claim 3, characterized

- in that the clock of a clock generator (TG) is applied to n delay elements (V1, ..., VN) arranged in parallel,

- in that the outputs of the delay elements (V1, ..., VN) are connected each to the clock input of a first D flip-flop (D1, ..., DN), to whose data input the inverting output is connected,

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- in that the non-inverting output of each first D flip-flop (D1, ..., DN) is connected to a first input of an Exclusive-Or circuit (A1, ..., AN) while the second input of each Exclusive-Or circuit (A1, ..., AN) is supplied with the digital signal (Rx D),

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- in that the output of each Exclusive-Or circuit (A1, ..., AN) is connected to a data input of a second D flip-flop (D11, ..., D1N) to whose clock input the output of the delay element (V1, ..., VN) is connected,

- in that the output of each of the second D flip-flops (D11, ..., D1N) is connected to the input of a monostable flip-flop (M1, ..., MN) whose output is connected to the reset input of a counter (Z1, ..., ZN) and the clock input of each counter (Z1, ..., ZN) is connected to the output of the delay element V1, ..., VN), and

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- in that the phase-synchronous bit clock is selected on the basis of the counts of the counters (Z1, ..., ZN).

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6. Receiver as claimed in Claim 3, 4 or 5, characterized in that the bit synchronization is effected by means of a program-controlled controller provided in both the base station and the associated mobile station of a cordless telephone set.