

ABSTRACT

A semiconductor device includes a substrate including a chip region and a scribe lane region including a chip adjacent region, a chip adjacent crossing region, and a peripheral crossing region; a passivation layer; row
5 trenches disposed between the boundary between the chip adjacent crossing region and a first boundary of the peripheral crossing region and the boundary between the chip adjacent crossing region and the chip adjacent region, in a direction crossing the first boundary, and disposed in the passivation layer; and column trenches disposed between the boundary
10 between the chip adjacent crossing region and a second boundary of the peripheral crossing region and the boundary between the chip adjacent crossing region and the chip adjacent region, in a direction crossing the second boundary, and disposed in the passivation layer.

15 FIG. 1