

DUAL-LOOP CONTROL FOR LASER ANNEALING OF SEMICONDUCTOR WAFERS

FIELD

[0001] The present disclosure relates generally to laser annealing of semiconductors, and in particular relates to dual-loop control for semiconductor laser annealing.

BACKGROUND ART

[0002] Laser annealing (also called laser spike annealing or laser thermal processing) is used in semiconductor manufacturing for a variety of applications, including for activating dopants in select regions of devices (structures) formed in a semiconductor wafer when forming active microcircuits such as transistors.

[0003] One form of laser annealing uses a scanned laser beam (“laser annealing beam” or “annealing laser beam”) to heat the surface of the semiconductor wafer to a temperature (the “annealing temperature”) for a time long enough to activate the dopants in the semiconductor structures (e.g., source and drain regions) but short enough to prevent substantial dopant diffusion. The time that the wafer surface is at the annealing temperature is determined by the power density of the laser annealing beam, as well as the exposure time, which is given by the width of the laser annealing beam along the scan direction divided by the velocity at which the laser annealing beam is scanned (the “scan velocity”).

[0004] Typical semiconductor processing requirements call for the annealing temperature to be between 400 °C and 1,300 °C, with a temperature uniformity of +/- 3 °C. To achieve this degree of temperature uniformity, the laser annealing beam needs to have a relatively uniform intensity in the cross-scan direction, which under most conditions represents less than a +/-5% intensity variation.

[0005] However, even when the laser annealing beam is made spatially very uniform, feedback to the laser is required to ensure that the annealing temperature remains uniform to within the stated tolerance. Local emissivity variations on patterned wafers can cause a temperature measurement error when the system cannot distinguish between a change in emission due to true temperature change and a local change in emissivity. For most logic

device wafers, the thickness and composition of the patterned regions is such that the deviation in pattern emissivity from bulk silicon is relatively small.

[0006] For other types of device wafers, the variations in emissivity can be substantial. For example, memory wafers have thick metal lines. Also, certain logic wafers include a silicide step wherein the patterned regions have a relatively thick metal-silicide (e.g., NiSi). In both of these cases, the variation in thermal emission from the emissivity variations is large. Consequently, as the laser annealing beam scans such wafers, the amplitude and time-frequency of the pattern-induced emission variation is such that the temperature control system can become unstable.

[0007] Re-tuning the temperature control system to respond to emission spikes would cause the laser power to be modulated in response to emissivity variations, and not temperature variations. As a result, the laser annealing system must process silicide and memory wafers in open loop (constant laser power) condition, which limits the temperature uniformity performance of the laser anneal due to the uncompensated effects such as laser power density fluctuation and/or variation in the local substrate temperature.

[0008] This in turn limits the maximum safe annealing temperature. The annealing temperature needs to be kept below the damage threshold temperature of the semiconductor wafer. The wider distribution of anneal temperatures under open-loop processing requires a reduction in the mean anneal temperature to keep the extremes of the anneal temperature distribution below the damage threshold. This presents a process compromise when (as is the case in most spike anneal process applications) a higher anneal temperature (below damage threshold) produces a superior process result

SUMMARY

[0009] An aspect of the disclosure is a method of laser annealing a wafer having a surface that supports an array of dies. The method includes scanning a laser annealing beam from the laser over the array of dies, wherein the laser has laser noise and is adjustable to control an amount of power in the laser annealing beam. The method also includes measuring and controlling the amount of power in the laser annealing beam using a first control loop that measures the amount of power and operates at a first frequency f_1 to

control the laser noise in the laser. The method further includes controlling the amount of power in the laser annealing beam using a second control loop that operates at a second frequency $f_2 < f_1$ by measuring thermal emission radiation from the wafer, including averaging the thermal emission radiation over at least one die and determining therefrom a corresponding average measured temperature, and using the average measured temperature and an annealing temperature set point to adjust the laser to control the amount of power in the laser annealing beam.

[0010] Another aspect of the disclosure is the method as described above, wherein the first frequency f_1 is in a range from 1 kHz to 100 kHz and the second frequency f_2 is in the range from 1 Hz to 100 Hz.

[0011] Another aspect of the disclosure is the method as described above, wherein f_1 is about $(100) \cdot f_2$.

[0012] Another aspect of the disclosure is the method as described above, wherein measuring the amount of power in the laser annealing beam includes deflecting a portion of the laser annealing beam to a photodetector system.

[0013] Another aspect of the disclosure is the method as described above, wherein deflecting a portion of the laser annealing beam includes diffracting a portion of the laser annealing beam using a grating formed on a reflective surface from which the laser annealing beam otherwise reflects.

[0014] Another aspect of the disclosure is the method as described above, wherein the wafer has a Brewster's angle, and wherein the measuring thermal emission radiation from the wafer is performed at Brewster's angle.

[0015] Another aspect of the disclosure is the method as described above, wherein the wafer is either a logic wafer or a memory wafer.

[0016] Another aspect of the disclosure is the method as described above, wherein the first and second control loops respectively employ first and second proportional-integral-derivative controllers that are coupled to one another.

[0017] Another aspect of the disclosure is the method as described above, wherein the laser annealing beam creates an annealing temperature at the wafer in the range from 400 °C to 1350 °C.

[0018] Another aspect of the disclosure is a laser annealing system for annealing dies supported by a wafer having a surface that supports dies each having a variation in emissivity. The laser annealing system includes a chuck that supports the wafer, and a movable stage that supports the chuck and that is adapted to move the chuck and wafer. The laser annealing system also has a laser that generates an initial laser beam and that has an adjustable output power and $1/f$ noise. The laser annealing system further includes an optical system configured to receive the initial laser beam and form therefrom a laser annealing beam and to direct a portion of the laser annealing beam to a photodetector system that in response generates a detector signal. The optical system is arranged so that the laser annealing beam is made incident upon and scans over the surface of wafer due to the movement of the wafer, and heats the wafer to an annealing temperature. The laser annealing system also includes a thermal emission detector system arranged relative to the surface of wafer and configured to receive thermal emission radiation therefrom that is generated by the laser annealing beam and average the received thermal emission radiation over an area of one or more of the dies, and in response generates a thermal emission signal. The laser annealing system also has a first control loop configured to receive the detector signal and control the laser to adjust the output power at a first frequency f_1 in the range from 1 kHz to 100 kHz to reduce the $1/f$ noise. The laser annealing system further has a second control loop configured to receive the thermal emission signal and control the laser to adjust the output power at a second frequency f_2 in the range from 1 Hz to 100 Hz to reduce variations in the annealing temperature.

[0019] Another aspect of the disclosure is the laser annealing system as described above, wherein the annealing temperature is in the range from 400 °C to 1350 °C.

[0020] Another aspect of the disclosure is the laser annealing system as described above, wherein the thermal emission signal is filtered to reduce or eliminate spikes.

[0021] Another aspect of the disclosure is the laser annealing system as described above, wherein the first and second control loops respectively include first and second proportional-integral-derivative controllers that are coupled to one another.

[0022] Another aspect of the disclosure is the laser annealing system as described above, wherein the wafer is either a logic wafer or a memory wafer.

[0023] Another aspect of the disclosure is a dual-loop control system for a laser annealing system that uses a laser annealing beam from a laser having $1/f$ noise and a controllable output power to anneal a wafer having dies that each have a variation in emissivity. The dual-loop control system has first and second control loops. The first control loop operates at first frequency f_1 in a range between 1 kHz and 100 kHz and is configured to control the laser output power to reduce the $1/f$ laser noise. The second control loop operates at a second frequency f_2 in a range between 1 Hz and 100 Hz and measures thermal emission radiation from the wafer over an area of one die or greater. The thermal emission radiation is caused by the laser annealing beam heating the wafer to an annealing temperature. The second control loop is configured to determine a measured wafer temperature from the measured thermal emission radiation and generate a measured temperature signal. The measured temperature signal is then used in combination with an annealing temperature set point signal to control the laser output power to minimize variations in the annealing temperature.

[0024] Another aspect of the disclosure is the dual-loop control system as described above, wherein the second control loop includes a thermal emission detector system. The thermal emission detector system measures the thermal emission radiation within one or more dies and then averages the within-die measurements to said area of one die or greater.

[0025] Another aspect of the disclosure is the dual-loop control system as described above, wherein the first control loop includes a photodetector system. The photodetector system receives a portion of the laser annealing beam created by a beam-turning element. The photodetector system also generates in response a detector signal representative of an amount power in the laser annealing beam. The first control loop includes a first proportional-integral-derivative (PID) controller that receives the detector signal as well as a second control signal from the second control loop and that generates a first control signal in response thereto and sends the first control signal to the laser.

[0026] Another aspect of the disclosure is the dual-loop control system as described above, wherein the second control loop includes a second proportional-integral-derivative (PID) controller. The second PID controller receives the measured temperature signal and the annealing temperature set point signal and in response generates the second control signal.

[0027] Another aspect of the disclosure is the dual-loop control system as described above, wherein the second control loop includes emission to temperature (E/T) logic. The E/T logic calculates the measured wafer temperature from the measured thermal emission radiation.

[0028] Another aspect of the disclosure is the dual-loop control system as described above, wherein the second control loop includes a low-pass filter. The low-pass filter filters the measured temperature signal from the E/T logic prior to inputting the measured temperature signal to the second PID controller.

[0029] Additional features and advantages of the disclosure are set forth in the detailed description that follows, and in part will be readily apparent to those skilled in the art from that description or recognized by practicing the disclosure as described herein, including the detailed description which follows, the claims, as well as the appended drawings.

[0030] It is to be understood that both the foregoing general description and the following Detailed Description present embodiments of the disclosure, and are intended to provide an overview or framework for understanding the nature and character of the disclosure as it is claimed.

[0031] The claims are incorporated into and constitute part of the Detailed Description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings are included to provide a further understanding of the disclosure, and are incorporated into and constitute a part of this specification. The drawings illustrate various embodiments of the disclosure, and together with the description serve to explain the principles and operations of the disclosure. In certain of the drawings, Cartesian coordinates are provided for reference and are not intended to be limiting as to direction and orientation.

[0033] FIG. 1 is a schematic diagram of an example laser annealing system that illustrates an embodiment of the dual-loop control system for the laser annealing system when performing laser annealing of a semiconductor wafer; and

[0034] FIG. 2 is a plan view of an example wafer showing the line image formed by the laser annealing beam scanning over the wafer surface, and including an inset that shows the wafer having an array of dies formed on the wafer surface.

DETAILED DESCRIPTION

[0035] Reference is now made in detail to embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Whenever possible, the same or like reference numbers and symbols are used throughout the drawings to refer to the same or like parts.

[0036] FIG. 1 is a schematic diagram of an example laser annealing system 10 that illustrates an embodiment of the dual-loop control configuration for the laser annealing system 10. A Cartesian coordinate system is shown for the sake of reference. Example laser annealing systems 10 are described, for example, U.S. Patents No. 7,612,372, 7,154,066 and 6,747,245, and U.S. Patent Application Publications No. 2010/0084744 and 2012/0100640, all of which are incorporated by reference herein.

[0037] The laser annealing system 10 includes a laser 20 that emits an initial laser beam 22 along an optical axis A1 that runs in the X-direction. An example laser 20 is a CO₂ laser that emits light at a nominal annealing wavelength λ_A of 10.6 μm . The laser 20 may also consist of or include one or more diode lasers.

[0038] The laser annealing system 10 also includes an optical system 30 arranged along an optical axis A1 downstream of the laser 20. The optical system 30 is configured to receive initial laser beam 22 and form therefrom a laser annealing beam 24. Example optical system 30 can include lenses, mirrors, apertures, filters, active optical elements (e.g., variable attenuators, etc.) and combinations thereof. Examples of the optical systems 30 are disclosed in U.S. Patents No. 8,026,519, 8,014,427, 7,514,305, 7,494,942, 7,399,945 and 6,366,308, all of which are incorporated by reference herein, and are also disclosed in the aforementioned U.S. Patent Publication No. 2012/0100640.

[0039] In an alternate embodiment of laser annealing system 10, a second laser and a second laser beam (not shown) are used to enhance the annealing process, e.g., by pre-heating a semiconductor wafer.

[0040] Also arranged along the optical axis A1 downstream of the optical system 30 is a beam-turning element 34, such as a mirror having a surface 36 that is substantially reflective at the annealing wavelength λ_A . This may be accomplished, for example, by making the beam-turning element 34 out of copper and providing the surface 36 as a gold

coating. In an example, the beam-turning element 34 is part of the optical system 30, and is shown as being separate by way of example and for ease of illustration and discussion.

[0041] The beam-turning element 34 defines a second optical axis A2 that is directed toward a semiconductor wafer ("wafer") 40 having a top surface ("surface") 42 with a surface normal N. The wafer 40 is supported by a chuck 50 (e.g., a heated chuck), which in turn is supported by a moveable wafer stage 52 that is driven by a stage driver 54. The second optical axis A2 defines an incident angle θ_2 on the surface 42 of wafer 40 relative to surface normal N. The laser annealing beam 24 travels down the second optical axis A2 and intersects the surface 42 of wafer 40. The wafer 40 has an overall wafer temperature T_w , which in an example is determined by the heated chuck 50, and which in an example is at least greater than room temperature.

[0042] In an example, the intersection of laser annealing beam 24 with the surface 42 of wafer 40 defines a laser beam line or "line image" 24L that scans over the surface 42 of wafer 40. The scanning of line image 24L can be accomplished by moving the moveable wafer stage 52 by the operation of stage driver 54, by adjusting the beam-turning element 34 to cause the laser annealing beam 24 to be scanned, or a combination of these two actions.

[0043] As discussed above, typical semiconductor processing requirements call for the annealing temperature T_A to be between 400 °C and 1,300 °C, with a temperature uniformity of ± 3 °C. To achieve this degree of temperature uniformity, the laser annealing beam 24 needs to have a relatively uniform intensity in the cross-scan direction, which under most conditions is less than a $\pm 5\%$ intensity variation.

[0044] In an example, the maximum temperature for laser spike annealing is at least about 25°C below the melt temperature of the material being annealed. In the case of silicon-based devices, the melt temperature of silicon is 1413 °C so that in an example the maximum temperature will be about 1388 °C.

[0045] In the case of germanium-enriched silicon, the melt temperature of the alloy depends on the percentage of Ge in the alloy. For 30% Ge, the melt temperature is approximately 1225 °C, so that an example maximum temperature for laser annealing will be about 25 °C lower, or about 1200 °C.

[0046] In the case of GaN on sapphire devices, the melt temperature of GaN is over 2500 °C, but the melt temperature of the Sapphire substrate is lower at 2040 °C. Thus, the non-melt annealing process is limited by the melt temperature of the sapphire substrate, and in an example the maximum anneal temperature about 2015 °C.

[0047] FIG. 2 is a plan view of an example wafer 40 that includes a close-up inset that shows the surface 42 of wafer 40 supporting an array of dies 44 each separated by a kerf region 46. The dies 44 represent regions where one or more integrated circuit (IC) chips are formed, with each IC chip comprising semiconductor devices and semiconductor device structures (not shown). In one example, the wafer 40 is a logic wafer used to make logic IC chips, while in another example the wafer 40 is a memory wafer used to make memory IC chips.

[0048] As discussed above, the semiconductor devices and semiconductor device structures within the dies 44 can have features with different emissivities, which can lead to the miscalculation of annealing temperatures T_A during the annealing process when trying to measure the annealing temperatures T_A within a given die 44. For example, as mentioned above, memory wafers usually have thick metal lines. Also, logic wafers can include a silicide step wherein the patterned regions have a relatively thick metal-silicide (e.g., NiSi) layer. Metal lines and metal-silicide have much lower emissivities than the underlying silicon.

[0049] In FIG. 2, the line image 24L is shown as being scanned back and forth over the surface 42 of wafer 40 to cover adjacent rows of the dies 44. The scanning is indicated by arrows AR1 and AR2, which correspond to adjacent scan paths SP1 and SP2 for the line image 24L. Scanning of the line image 24L across the surface 42 of wafer 40 may be accomplished by using the moveable wafer stage 52 to scan the surface 42 of wafer 40 under a stationary line image 24L or by scanning the line image 24L across a stationary surface 42 of wafer 40 by use of appropriate scanning optical elements as part of the optical system 30 or the beam-turning element 34. By extension, a combination of these two approaches may be used.

[0050] In an example, the surface 36 of beam-turning element 34 is configured to deflect a relatively small portion 24P of the laser annealing beam 24 along an optical axis A3. In an example, this is accomplished by providing a weak (e.g., lightly scribed) diffraction grating

36G onto the surface 36 of beam-turning element 34. A photodetector system 60 is arranged along the optical axis A3 and is arranged to receive a portion 24P of the laser annealing beam 24 and in response thereto generate a detector signal SD representative of the measured power. In an example, the amount of power in the portion 24P of laser annealing beam 24 is only a few percent of the power in the laser annealing beam 24. Whether by design or by calibration, the amount of power in the portion 24P of laser annealing beam 24 is a known fraction of the laser annealing beam 24, so that a measurement of the portion 24P of laser annealing beam 24 provides a measure of the amount of optical power in the laser annealing beam 24.

[0051] The photodetector system 60 is selected to detect the portion 24P of laser annealing beam 24 at the laser (annealing) wavelength λ_A . In the case where the laser 20 is a CO₂ laser, an example photodetector system 60 includes a cooled HgCdTe detector. In this case, the portion 24P of laser annealing beam 24 is substantially monochromatic so that the photodetector system 60 can include a narrow-band optical filter 61 configured to prevent the detection of light of other wavelengths. The narrow-band optical filter 61 may be cooled to reduce background thermal emission.

[0052] The laser annealing system 10 also includes a thermal emission detector system 80 that resides along an optical axis A4 that defines an angle θ_4 on the surface 42 of wafer 40 relative to the surface normal N. In an example, the optical axis A4 intersects the second optical axis A2 at the surface 42 of wafer 40. In an example, the angle θ_4 is equal to the Brewster's angle for the wafer 40. The Brewster's angle for silicon is about 75°.

[0053] The thermal emission detector system 80 is configured to measure thermal emission radiation 82 emitted by the surface 42 of wafer 40 during the laser annealing process, and generate in response thereto an electrical emission signal SE representative of the measured thermal emission E. An example thermal emission detector system 80, along with method of calculating a measured temperature T_M from the measured thermal emission E, is described in the aforementioned U.S. Patent Application Publication No. 2012/0100640.

[0054] The laser annealing system 10 also includes a controller 100 that is operably connected to the laser 20, the stage driver 54, the photodetector system 60 and the thermal emission detector system 80. The controller 100 has a number of logic and control

components and can be configured using one or more field-programmable gate arrays (FPGAs) and other programmable and non-programmable electronic components known to those skilled in the art, such as processor units, memory units, filters, feedback controllers, etc. The controller 100 is configured (e.g., via instructions embodied in computer-readable media of one or more of the programmable components) to carry out the dual-loop control methods described herein.

[0055] The controller 100 includes a first feedback controller 112-1 shown by way of example and referred to hereinafter as a first proportional-integral-derivative (PID) controller. The first PID controller 112-1 has an input end (“input”) 113 and an output end (“output”) 114. The photodetector system 60 is electrically connected to the input 113, while the laser 20 is electrically connected to the output 114.

[0056] The controller 100 also includes an emission-to-temperature logic unit (“E/T logic”) 120 electrically connected to the thermal emission detector system 80. The E/T logic 120 is configured to receive the measured electrical emission signal SE and convert the measured thermal emission E to a measured temperature T_M , and output a corresponding measured temperature signal ST_M . The measured temperature signal ST_M represents an averaged measured temperature, as calculated from the measured electrical emission signal SE. The average is over a time window determined by the bandwidth of thermal emission detector system 80 and the measured electrical emission signal SE.

[0057] The measured electrical emission signal SE generally includes spikes due to die emissivity variations. These spikes will show up in the measured temperature signal ST_M if they not suppressed. Consequently, in an example embodiment, the E/T logic 120 is electrically connected to a low-pass filter (LPF) 130 that low-pass filters the measured temperature signal ST_M to form a low-pass filtered (“filtered”) measured temperature signal ST_{MF} . In an example, the LPF 130 is formed from a signal-processing device such as a field-programmable gate array (FPGA) that performs a running average or a spike suppression algorithm in addition to performing low-pass filtering.

[0058] The controller 100 also includes a second feedback controller 112-2 also referred to hereinafter as the second PID controller by way of example. The LPF 130 is electrically connected to the input 113 of second PID controller 112-2. An annealing temperature set-point that is embodied in an annealing temperature set-point signal ST_{SET} is also inputted to

the input 113 of second PID controller 112-2. The set-point defines a set-point annealing temperature T_{AS} for the annealing process.

[0059] The output of second PID controller 112-2 is electrically connected to the input 113 of the first PID controller 112-1. The second PID controller 112-2 outputs a second control signal SC2 that corresponds to a requested amount of laser power to maintain a substantially uniform the annealing temperature T_A , i.e., as close to the set-point annealing temperature T_{AS} as possible. The second control signal SC2 and the detector signal SD from the photodetector system 60 are inputted into the first PID controller 112-1. The first PID controller 112-1 processes the second control signal SC2 and the detector signal SD and outputs a first control signal SC1 to the laser 20 that instructs the laser 20 to deliver a select amount of power, or to adjust its output by a select amount so that laser annealing beam 24 has the select amount of power.

[0060] The configuration of laser annealing system 10 defines two coupled control loops schematically indicated in FIG. 1 as L1 and L2. The first control loop L1 operates at a first frequency f_1 and is defined by the laser 20, the photodetector system 60 and the first PID controller 112-1. The second control loop L2 operates at a second frequency $f_2 < f_1$ and is defined by the thermal emission detector system 80, the E/T logic 120, the LPF 130 and the second PID controller 112-2. The two control loops L1 and L2 are coupled at the first PID controller 112-1.

[0061] There are several sources of noise in the laser annealing system 10 that must be controlled to maintain a constant (uniform) annealing temperature T_A . One noise source is the inherent noise in the output of laser 20, which has a characteristic $1/f$ distribution. Another source arises from systematic effects within the laser annealing system 10 itself. One example of this type of noise is the variation of the overall wafer temperature T_W due to non-uniformities in the heated chuck 50. Another example is variation in the power density of the laser annealing beam 24 due to out-of-plane motion of the wafer 40 relative to the laser annealing beam 24, due to imperfections or setup tolerances in the moveable wafer stage 52, which causes the power density in the line image 24L to vary during the scan.

[0062] Another source of noise is emissivity “noise” stemming from the laser annealing beam 24 passing over regions within a given die 44 that have varying values of emissivity.

This type of noise is uncompensated in an emission feedback system, since there is no real-time, localized measurement of emissivity available to correct the conversion of electrical emission signal SE to the measured temperature signal ST_M . This emissivity “noise” has a characteristic frequency that is determined by the physical spacing of the structures (e.g., metal lines or pads) within die 44, and the speed of moveable wafer stage 52. This constitutes “noise” in the sense that it arises from a change of the measured signal resulting from an unmeasured (and thus uncompensated) physical attribute (emissivity) of the emitting surface.

[0063] In the absence of emissivity variations, a single control loop based on emission feedback from the local annealing line image 24L can manage the control of both the laser 20 and systematic sources of error to maintain a substantially constant annealing temperature T_A . Such a system can maintain the required power density at the wafer 40 regardless if the error being compensated for arises from the laser 20 or from the system itself.

[0064] However, when the temperature measurement itself is erroneous because of localized changes in emissivity, such a loop will drive the system to an incorrect annealing temperature T_A due to the change in emission signal level contributed by the change in emissivity.

[0065] The laser annealing system 10 thus employs dual-loop control using the first and second control loops L1 and L2 that cooperate to manage the main sources of noise, including eliminating or greatly reducing the above-described sensitivity to emissivity “noise.”

[0066] The first control loop L1 operates to control the amount of power in the laser annealing beam 24 by detecting the portion 24P of laser annealing beam 24 with the photodetector system 60 and providing the corresponding detector signal SD to the input 113 of first PID controller 112-1. The first PID controller 112-1 also receives the second control signal SC2 from the second control loop L2. The first control loop L1 operates at higher frequency f_1 than the second frequency f_2 of the second control loop L2. The first control loop L1 operates at the first frequency f_1 sufficient to mitigate laser noise, which extends out to several hundred Hz (with a 1/f roll-off). In an example, the first frequency f_1 is in the range from about 1KHz to about 100KHz.

[0067] The second control loop L2 operates at the second frequency $f_2 < f_1$ and looks at the emission from wafer 40. The low-pass filtering of measured temperature signal ST_M generates the filtered measured temperature signal ST_{MF} . This filtered measured temperature signal ST_{MF} is an average emission/temperature with a time average corresponding to a spatial average (that correspondence stemming from the scanning stage) that spans die-scale dimensions on wafer 40. The averaging reduces or eliminates the adverse effects of signal spikes due to emissivity variations. Thus, the temperature calculation is based on an average emissivity, where the “average” is taken over a relatively large distance (i.e., die scale). The Logic in the E/T Logic 120 may also be used to facilitate suppression of emissivity-related variations in the electrical emission signal SE, by numerical filtering, spike detection logic or other algorithms designed to mitigate the influence of emissivity-related variations in the electrical emission signal SE on the filtered measured temperature signal ST_{MF} .

[0068] The second control loop L2 then controls and corrects for low frequency (relative to the first frequency f_1) error components, which mainly come from the aforementioned systematic errors. These systematic errors have a spatial period larger than die scale and so manifest themselves (in the time domain) at low frequency (as determined by the scan speed). The second control loop L2 updates the first control loop’s operational set point at the first PID controller 112-1. In an example, the second frequency f_2 of second control loop L2 is in the range from 1 Hz to 100 Hz.

[0069] Compared to the laser 1/f noise, the signal content resulting from emissivity variations is typically more harmonic in spectral content because the surface structures creating the signal variations are themselves structured with more or less well-defined spatial periods. This results in a more or less well defined time-domain frequency response determined by the stage speed and physical spacing of the structures.

[0070] Thus, the second control loop L2 measures the measured thermal emission E from the surface 42 of wafer 40 at the location where the line image 24L is being scanned. In an example, the thermal emission detector system 80 has a field of view that is at least the size of die 44 in the Y-direction (i.e., the cross-scan direction) and that is at least as wide as the line image 24L in the X-direction (i.e., the scan direction). In another example, the field of view need not cover the size of die 44 in the Y-direction, e.g., it can be several millimeters in

the Y-direction while the die 44 can have a Y-dimension of 1 cm or so. In an example, the thermal emission detector system 80 includes a linear array of optical fibers (not shown).

[0071] The spatial averaging of the thermal emission measurement (and hence the annealing temperature measurement) is obtained by time-averaging during the scanning of laser annealing beam 24 over one or more dies 44. Thus, the measurement of the measured thermal emission E is used to measure the annealing temperature averaged over a select area, which is translated into a sample time based on the speed of line image 24L, which in an example is the speed of moveable wafer stage 52. In an example, the thermal emission detector system 80 has a refresh rate of about 80 KHz that is then averaged by 4X to reduce the effective refresh rate to about 20 kHz.

[0072] In an example, the select area over which the emission/temperature is averaged is the size of a die 44 or larger so that the second control loop L2 responds to larger-than-die changes in temperature. Such temperature changes can arise, for example, from variations in the heating from the heated chuck 50, variations in laser power density as might be caused by various mechanical drifts, laser efficiency/power drift, and the lower-frequency $1/f$ laser power variations. The second control loop L2 operates at substantially slower frequency f_2 than the first frequency f_1 , such $f_1 > 5 \cdot f_2$, with an exemplary second frequency f_2 being about 10 Hz. In one example, $f_1 \approx (100) \cdot f_2$.

[0073] In an example, the second control loop L2 is intended to provide feedback for relatively low-frequency changes in the emission/temperature resulting from more or less die-sized and up to wafer-diameter-size changes in substrate temperature and/or power density. If the second frequency f_2 is set too close to the first frequency f_1 , the second control loop L2 will try to adjust the amount of power in the laser annealing beam 24 based on small changes in emission due to local changes in emissivity, e.g., the emissivity changes within a single die 44. It has been found that the annealing process is improved when such small-scale emissivity changes are ignored and the amount of power in the laser annealing beam 24 is adjusted based on relatively large-area average emissivity (e.g., a die-size area, a multiple-die size area, etc.).

[0074] The thermal emission detector system 80 can include one or more detectors 81, including multiple detectors operating at multiple wavelengths for multi-color pyrometry. The one or more detectors 81 preferably have sufficient detectivity (D^*) to yield a

reasonable signal-to-noise ratio (SNR) for the photon flux associated with the thermal emission radiation 82 at the set-point annealing temperature T_{AS} and for the given laser annealing beam geometry. An example thermal emission detector system 80 operates over a band-limited wavelength range for which the band-integrated thermal emission has good sensitivity to changes in temperature about the set-point annealing temperature T_{AS} .

[0075] For example, in the case of laser annealing junctions, the annealing temperature T_A is in the range 1100 °C to 1250 °C, and the appropriate wavelength range for thermal emission radiation is 500 nm to 900 nm. At these wavelengths, photo-multiplier tubes or Si-based photodiodes can be used as detectors. For contact annealing, the annealing temperatures T_A are lower, e.g., in the range 800 °C to 1000 °C, and a longer wavelength detector sensitive in the 1 μ m to 2 μ m region is appropriate, such as an InGaAs detector.

[0076] While the first and second control loops L1 and L2 are physically coupled and serve to adjust the laser power, the aforementioned difference in the control loop frequencies f_1 and f_2 serve to functionally decouple the two control loops L1 and L2 so that each can operate independently and in a stable manner, so that one control loop does not introduce instabilities into the other.

[0077] The dual-loop control approach to laser annealing disclosed herein can be considered a hybrid approach based on wafer-to-wafer (WTW) and wafer-within-wafer (WIW) approaches. The second control loop L2 provides WIW-like feedback, but operates at a relatively “slow” frequency f_2 so that it is averaging emission over one or more dies 44, while the first control loop L1 is “fast” to compensate for corresponding 1/f noise in the laser 20 that contributes to unwanted power fluctuations and thus unwanted annealing temperature variations.

[0078] It will be apparent to those skilled in the art that various modifications and variations can be made to the present disclosure without departing from the spirit and scope of the disclosure. Thus it is intended that the present disclosure cover the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of annealing with a laser a wafer having a surface that supports an array of dies, comprising:

scanning a laser annealing beam from the laser over the array of dies, wherein the laser has laser noise and is adjustable to control an amount of power in the laser annealing beam;

measuring and controlling the amount of power in the laser annealing beam using a first control loop that measures the amount of power and operates at a first frequency f_1 to control the laser noise in the laser; and

controlling the amount of power in the laser annealing beam using a second control loop that operates at a second frequency $f_2 < f_1$ by measuring thermal emission radiation from the wafer, including averaging the thermal emission radiation over at least one die and determining therefrom a corresponding average measured temperature, and using the average measured temperature and an annealing temperature set point to adjust the laser to control the amount of power in the laser annealing beam.

2. The method of claim 1, wherein the first frequency f_1 is in a range from 1 kHz to 100 kHz and the second frequency f_2 is in the range from 1 Hz to 100 Hz.

3. The method of claim 1 or 2, wherein f_1 is about $(100) \cdot f_2$.

4. The method of any of claims 1 through 3, wherein measuring the amount of power in the laser annealing beam includes deflecting a portion of the laser annealing beam to a photodetector system.

5. The method of claim 4, wherein deflecting a portion of the laser annealing beam includes diffracting a portion of the laser annealing beam using a grating formed on a reflective surface from which the laser annealing beam otherwise reflects.

6. The method of any of claims 1 through 5, wherein the wafer has a Brewster's angle, and wherein the measuring thermal emission radiation from the wafer is performed at Brewster's angle.
7. The method of any of claims 1 through 6, wherein the wafer is either a logic wafer or a memory wafer.
8. The method of any of claims 1 through 7, wherein the first and second control loops respectively employ first and second proportional-integral-derivative controllers that are coupled to one another.
9. The method of any of claims 1 through 8, wherein the laser annealing beam creates an annealing temperature at the wafer in the range from 400 °C to 1350 °C.
10. A laser annealing system for annealing dies supported by a wafer having a surface that supports dies each having a variation in emissivity, comprising:
 - a chuck that supports the wafer, and a movable stage that supports the chuck and that is adapted to move the chuck and wafer;
 - a laser that generates an initial laser beam and that has an adjustable output power and 1/f noise;
 - an optical system configured to receive the initial laser beam and form therefrom an laser annealing beam and to direct a portion of the laser annealing beam to a photodetector system that in response generates a detector signal, the optical system being arranged so that the laser annealing beam is made incident upon and scans over the surface of wafer due to the movement of the wafer, and heats the wafer to an annealing temperature;
 - a thermal emission detector system arranged relative to the surface of wafer and configured to receive thermal emission radiation therefrom that is generated by the laser annealing beam and average the received thermal emission radiation over an area of one or more of the dies, and in response generates a thermal emission signal;

a first control loop configured to receive the detector signal and control the laser to adjust the output power at a first frequency f_1 in the range from 1 kHz to 100 kHz to reduce the $1/f$ noise; and

a second control loop configured to receive the thermal emission signal and control the laser to adjust the output power at a second frequency f_2 in the range from 1 Hz to 100 Hz to reduce variations in the annealing temperature.

11. The laser annealing system of claim 10, wherein the annealing temperature is in the range from 400 °C to 1350 °C.

12. The laser annealing system of claim 10 or 11, wherein the thermal emission signal is filtered to reduce or eliminate spikes.

13. The laser annealing system of any of claims 10 through 12, wherein the first and second control loops respectively include first and second proportional-integral-derivative controllers that are coupled to one another.

14. The laser annealing system of any of claims 10 through 13, wherein the wafer is either a logic wafer or a memory wafer.

15. A dual-loop control system for a laser annealing system that uses a laser annealing beam from a laser having $1/f$ noise and a controllable output power to anneal a wafer having dies that each have a variation in emissivity, comprising:

a first control loop operating at first frequency f_1 in a range between 1 kHz and 100 kHz and configured to control the laser output power to reduce the $1/f$ laser noise; and

a second control loop operating at a second frequency f_2 in a range between 1 Hz and 100 Hz and that measures thermal emission radiation from the wafer over an area of one die or greater, the thermal emission radiation being caused by the laser annealing beam heating the wafer to an annealing temperature, the second control loop being configured to determine a measured wafer temperature from the measured thermal emission radiation and generate a measured temperature signal, which is used in combination with

an annealing temperature set point signal to control the laser output power to minimize variations in the annealing temperature.

16. The dual-loop control system of claim 15, wherein the second control loop includes a thermal emission detector system that measures the thermal emission radiation within one or more dies and then averages the within-die measurements to said area of one die or greater.

17. The dual-loop control system of claim 15 or 16, wherein the first control loop includes a photodetector system that receives a portion of the laser annealing beam created by a beam-turning element, the photodetector system generating in response a detector signal representative of an amount power in the laser annealing beam, and wherein the first control loop includes a first proportional-integral-derivative (PID) controller that receives the detector signal as well as a second control signal from the second control loop and that generates a first control signal in response thereto and sends the first control signal to the laser.

18. The dual-loop control system of claim 17, wherein the second control loop includes a second proportional-integral-derivative (PID) controller that receives the measured temperature signal and the annealing temperature set point signal and in response generates the second control signal.

19. The dual-loop control system of any of claims 15 through 17, wherein the second control loop includes emission to temperature (E/T) logic that calculates the measured wafer temperature from the measured thermal emission radiation.

20. The dual-loop control system of claim 18, wherein the second control loop includes emission to temperature (E/T) logic that calculates the measured wafer temperature from the measured thermal emission radiation.

21. The dual-loop control system of claim 20, wherein the second control loop includes a low-pass filter that filters the measured temperature signal from the E/T logic prior to inputting the measured temperature signal to the second PID controller.