CLAIMS

1. A device comprising:

a substrate defined with a device region, the device region comprises an ESD protection circuit having a transistor, wherein the transistor includes

a gate having first and second sides,

a first diffusion region in the device region adjacent to the first side of the gate,

a second diffusion region in the device region displaced away from the second side of the gate, wherein the first and second diffusion regions comprise dopants of a first polarity type, and

a drift isolation region disposed between the gate and the second diffusion region;

a first device well encompasses the device region;

a second device well disposed within the first device well; and

a drain well having dopants of the first polarity type is disposed under the second diffusion region and within the first device well.

2. The device of claim 1 wherein the first device well comprises dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

3. The device of claim 2 wherein the first polarity type comprises n type and the second polarity type comprises p type.

4. The device of claim 1 wherein the second device well encompasses at least the first diffusion region and a part of the gate.

5. The device of claim 4 wherein the second device well encompasses the gate, the drift isolation region and the second diffusion region.

6. The device of claim 1 further comprises:

a drift well disposed within the second device well.

7. The device of claim 6 wherein the first device well and the drift well comprise dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

8. The device of claim 7 wherein the first polarity type comprises n type and the second polarity type comprises p type.

9. The device of claim 6 wherein the drift well encompasses the second diffusion region.

10. The device of claim 9 wherein the drift well extends under the gate from the second side of the gate.

11. The device of claim 6 further comprises a low voltage (LV) well, wherein the LV well is disposed within the drift well.

12. The device of claim 11 wherein the LV well is disposed under the drift isolation region.

13. The device of claim 11 wherein the LV well comprises dopants of a second polarity type.

14. A device comprising:

a substrate having first and second device wells in a device region, wherein the second device well is disposed within the first device well;

a transistor in the device region, wherein the transistor includes

a gate having first and second sides, and

a first diffusion region disposed adjacent to the first side of the gate and a second diffusion region displaced away from the second side of the gate, and

a drift isolation region disposed between the gate and the second diffusion region; and

a drain well is disposed under the second diffusion region and within the first device well.

15. The device of claim 14 wherein the first and second diffusion regions, the first device well and the drain well comprise dopants of a first polarity type and the second device well comprises dopants of a second polarity type.

16. The device of claim 15 wherein the first polarity type comprises n type and the second polarity type comprises p type.

17. The device of claim 14 wherein the second device well encompasses at least the first diffusion region and a part of the gate.

18. The device of claim 17 wherein the second device well encompasses the gate, the drift isolation region and the second diffusion region.

19. The device of claim 14 further comprises:

a drift well disposed within the second device well.

20. The device of claim 19 further comprises a low voltage (LV) well, wherein the LV well is disposed within the drift well.

CLAIMS

1. A device comprising:

a substrate defined with a device region, the device region comprises an ESD protection circuit having a transistor, wherein the transistor includes

a gate having first and second sides,

a first diffusion region in the device region adjacent to the first side of the gate, wherein the gate overlaps the first diffusion region,

a second diffusion region in the device region displaced away from the second side of the gate, wherein the first and second diffusion regions comprise dopants of a first polarity type, and

a drift isolation region disposed between the gate and the second diffusion region;

a first device well encompasses the device region;

a second device well disposed within the first device well; and

a drain well having dopants of the first polarity type is disposed under the second diffusion region and within the first device well.

2. The device of claim 1 wherein the first device well comprises dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

3. The device of claim 2 wherein the first polarity type comprises n type and the second polarity type comprises p type.

4. The device of claim 1 wherein the second device well encompasses at least the first diffusion region and a part of the gate.

5. The device of claim 4 wherein the second device well encompasses the gate, the drift isolation region and the second diffusion region.

6. The device of claim 1 further comprises:

a drift well disposed within the second device well.

7. The device of claim 6 wherein the first device well and the drift well comprise dopants of the first polarity type and the second device well comprises dopants of a second polarity type.

8. The device of claim 7 wherein the first polarity type comprises n type and the second polarity type comprises p type.

9. The device of claim 6 wherein the drift well encompasses the second diffusion region.

10. The device of claim 9 wherein the drift well extends under the gate from the second side of the gate.

11. The device of claim 1 wherein the gate overlaps the first diffusion region by about 0.1-0.5 μm.

12. The device of claim 1 wherein the drain well has a depth between the bottom of the drift isolation region and the second device well.

13. The device of claim 12 wherein the drain well has a width narrower than the second diffusion region.

14. A device comprising:

a substrate having first and second device wells in a device region, wherein the second device well is disposed within the first device well;

a transistor in the device region, wherein the transistor includes

a gate having first and second sides, and

a first diffusion region disposed adjacent to the first side of the gate, wherein the gate overlaps the first diffusion region and a second diffusion region displaced away from the second side of the gate, and

a drift isolation region disposed between the gate and the second diffusion region; and

a drain well is disposed under the second diffusion region and within the first device well.

15. The device of claim 14 wherein the first and second diffusion regions, the first device well and the drain well comprise dopants of a first polarity type and the second device well comprises dopants of a second polarity type.

16. The device of claim 15 wherein the first polarity type comprises n type and the second polarity type comprises p type.

17. The device of claim 14 wherein the second device well encompasses at least the first diffusion region and a part of the gate.

18. The device of claim 17 wherein the second device well encompasses the gate, the drift isolation region and the second diffusion region.

19. The device of claim 14 further comprises:

a drift well disposed within the second device well.

20. The device of claim 14 wherein the gate overlaps the first diffusion region by about 0.1-0.5 μm.