A B S T R A C T

Design System for VLSI Chips Arranged on a Carrier and Module thus Designed

A system design for VLSI chips arranged on a carrier and the module thus designed is described. In a top-down design system synoptically and simultaneously an electrical circuitry is optimized by designing synoptically the chips and the chip carrier. The overall logic is divided in partitions which fit on chips. A chip placement on the carrier is performed considering minimum overall connection length and providing preferably parallel connection. Input/Output contacts are assigned on chips vis-a-vis each other when they correspond. They are connected by parallel lines. The design of the several chips is done from outside to inside, starting with the assigned I/O contacts. Overall, in combining optimum overall design and optimum chip design, a semiconductor thin film silicon multichip module of high yield and performance is provided. As carrier that is included in the design from the beginning, preferably a thin film passive silicon carrier is used.

This Sheet Has Been Replaced