

LOW LEAKAGE CIRCUIT BOARD FOR PROBE CARD AND LOW LEAKAGE PROBE CARD, AND FABRICATION METHOD OF SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a method of making a circuit board for use in a probe card, the circuit board made therefrom, a probe card using the circuit board and a method of making a probe card by using the circuit board.

2. Description of the Related Art

Following the development of integrated circuit devices toward high density and small size features, the electrical test precision level must be relatively raised to meet the requirement. Therefore, many factors include substrate capability of electric insulating and mechanical stress, precise wiring path of circuit pattern, electrical effect of parasitic capacitance and resistance, current leakage among adjacent circuits, and etc, must be taken into account when selecting substrate materials and making wiring circuits for probe cards. FIG. 8 is a schematic sectional elevation of a part of a probe card 90 according to the prior art. The fabrication of forming conductive wires 91 on the surface of a substrate 92 contains the process of coating a layer of adhesive on the backside surface of a single piece of copper foil, adhering the copper foil to the top surface of the substrate 92, and patterning the copper foil into the desired conductive wires 91 by means of chemical etching. However, chemical etching process cannot react to the adhesive material and move it away from the top surface of the substrate 92 but instead keep the unwanted adhesive left between neighboring conductive wires 91. Therefore, the residual adhesives provide the current leakage path when test signals transmitting through the relative conductive wires 91. This problem lowers the yield of

wafer level test by the probe card 90, affecting semiconductor wafer manufacturing efficiency.

FIG. 9 shows a probe card 95 disclosed in Taiwan Patent Publication No. 522449. According to this design, mechanical processing is employed to a ceramic substrate 96 and a piece of a conductive member 97 adhered on the ceramic substrate 96 for patterning a predetermined circuit layout. Accordingly, a plurality of conductive wires corresponded to the circuit layout are carved out of the conductive member 97 and the ceramic substrate 96, and simultaneously formed a plurality of wiring gaps deepened into the substrate 96 at a predetermined depth. This processing method eliminates the aforesaid problem of adhesive residues and uses air as existent electric insulation within the wiring gaps to isolate the conductive wires from one another. Except for the improvement of electrical quality, this structural design further enhances the strength of the probe card due to the non-deformable and high-hardness features of the ceramic substrate. However, during the mechanical processing sequentially to the conductive member 97 and the ceramic substrate 96, different process conditions must be corresponded with the processed materials at different stages. Especially when making a minor change on the circuit structure, the mechanical conditions must be fine controlled to precisely meet the fine structure, thus complicating the fabrication and lowering the probe card manufacturing efficiency. Further, as the applicable substrate material is limited to the consideration of electric insulation and low flexibility, ceramic material is the most practical choice, however it is expensive. Therefore, it is an important subject in high precision test engineering of how to obtain the optimal material of a probe card structure that saves the cost, avoids current leakage in the test environment, and improves the semiconductor manufacturing efficiency.

SUMMARY OF THE INVENTION

The present invention has been accomplished under the circumstances in view. It is therefore the main object of the present invention to provide a high-efficiency probe card and the fabrication method of the same, which saves the probe card manufacturing cost and effectively avoids current leakage of test signals transmitted through the probe card.

To achieve this and other objects of the present invention, the low leakage probe card fabrication method is to make a circuit board, and then module with a plurality of signal lines and a probe set to form a probe card. The circuit board is stacked from the bottom toward the top in proper order of a support layer, an insulating layer, and a conducting layer. The support layer is prepared from a high hardness material having a predetermined flexural strength. The insulating layer is prepared from an electric insulating material, having a plurality of grooves engraved thereon. The grooves divide the top surface of the insulating layer into a plurality of bonding surface. The conducting layer comprises a plurality of conducting strips respectively adhered to the bonding surfaces of the insulating layer. By means of electrically connecting the two ends of each of the signal lines to the conducting strips and the probes of the probe set, a probe card is thus obtained. The probe card effectively avoids from current leakage among the signal transmission paths.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an exploded view of a circuit board made according to a first embodiment of the present invention.

FIG. 2 is an exploded view of a probe card made according to the first embodiment of the present invention.

FIG. 3 is a top view of the probe card according to the first embodiment of

the present invention.

FIG. 4 is a schematic structural view of the probe card according to the first embodiment of the present invention.

FIG. 5 is a bottom view of the probe card according to the first embodiment of the present invention.

FIG. 6 is an exploded view of a probe card in accordance with a second embodiment of the present invention.

FIG. 7 is a top view of the probe card according to the second embodiment of the present invention.

FIG. 8 is a schematic sectional elevation of a part of a probe card according to the prior art.

FIG. 9 is a schematic sectional elevation of a part of another structure of probe card according to the prior art.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIGS. 1, a circuit board 1 for probe card for testing semiconductor wafers or the like in accordance with a first embodiment of the present invention is shown comprised of a support layer 10, an insulating layer 20, and a conducting layer 30.

The fabrication of the circuit board 1 comprises the steps of:

a) preparing a wafer-sized substrate having centered through a test hole 11 to form the said support layer 10, which wafer-sized substrate is made of a high hardness material having a flexural strength over 100kgs/cm² subject to ASTM (American Society for Testing and Materials) standards, for example, a certain thickness of metal or ceramic material, or glass epoxy of FR-4 (Flame Resistant laminates level-4) or FR-5 (Flame Resistant laminates level-5);

b) preparing an insulating material having a shape and size approximately equal to the support layer **10** and a surface resistivity over $10^{13} \Omega/\text{cm}^2$ subject to ASTM (American Society for Testing and Materials) standards;

c) making a test hole **21** through the center of the prepared insulative material corresponding to the test hole **11** of the support layer **10**;

d) making a plurality of grooves **22** radial around the border area of the insulating material subject to a predetermined depth and pattern so as to form the aforesaid insulating layer **20** in which a plurality of protruding portions **23** are formed corresponding to the grooves **22** and radial around the border area of the insulating layer **20**, and the surfaces of the protruding portions **23** show a radial distributed circuit pattern and are divided into first bonding surfaces **231** and second bonding surfaces **232**. The insulating material can be a regular and low cost engineering plastic material such as PE (polyethylene), UPE (ultra-high molecular weight polyethylene), PP (polypropylene), ABS (acrylonitrile-butadiene-styrene), PTEE (poly tetra fluoro ethylene), PMMA (para-methoxymethamphetamine), or PVC (polyvinyl chloride) so that the grooves **22** can be formed by a conventional mechanical processing on the insulating material. Alternatively, the insulating material can be formed of a photoresist material so that the grooves **22** can be formed by the photolithography processing on the insulating material; and

e) patterning a copper foil subject to the circuit pattern of the surfaces of the protruding portions **23** to form a plurality of copper sheets **31** having defined as a plurality of first conducting strips **311** and second conducting strips **312**, and also subject to the mounting location of the insulating layer **20** provided for mounting screws on the circuit board **1** to form a mounting ring **32**, and then adhering the first conducting strips **311**, the second conducting strips **312**, and the mounting ring **32**

respectively to the first bonding surfaces **231**, the second bonding surfaces **232**, and the mounting location of the insulating layer **20** so as to form the said conducting layer **30**.

Referring to FIGS. 2~4, the aforesaid circuit board **1** is mounted with a plurality of signal lines **40** and a probe set **50**, thereby forming a cantilever-type probe card **2** subject to the procedure stated hereinafter.

First, making a plurality of through holes **101** and **201** through the support layer **10** and the insulating layer **20** having the diameter similar to that of the signal lines **40**. Thereafter, sequentially inserting the signal lines **40** through the through holes **101** of the support layer **10** and the through holes **201** of the insulating layer **20**. As the signal lines **40** are adopted from the regular coaxial cables, each of which comprising an axial wire **401** coaxially surrounded by the sequence of an insulator, a grounded shielding layer **402**, and a protective layer, the electrical connection of the signal lines **40** are to connect the grounded shielding layers **402** and the axial wires **401** of the signal lines **40** respectively to the first conducting strips **311** and second conducting strips **312** of the conducting layer **30** of the circuit board **10**, so that each first conducting strips **311** and the associating grounded shielding layer **402** constitute one grounding circuit **41** of the circuit board **1**, and each second conducting strip **312** and the associating axial wire **401** constitute one signal circuit **42** of the circuit board **1**.

Referring to FIGS. 4 and 5, the probe set **50** is a regular cantilever pin structure comprised of a jumping holder **51**, a probe holder **52**, and a plurality of probes **53**. The jumping holder **51** provides a plurality of solder pads **510** corresponding to the through holes **101** and **201** for the connection of the signal lines **40** and the probes **53**. The probe holder **52** is made of a shock absorbing and electric insulating material for receiving the probes **53** and holding the probes **53** positively in place. The probes **53** are made of a metal material of high conductivity, each of which

having a tip for positively contacting with one respective electronic device of a semiconductor wafer to be tested.

When the testing tips of a testing machine electrically connecting to the outer part of the first conducting strips **311** and second conducting strips **312** of the circuit board **1**, the probe card **2** transmits test signals sent out from the testing machine through the signal circuits **42** and the respective probes **53** to the respective electronic devices to be tested, and the respectively neighbored grounding circuits **41** make sure for signal transmission integrity. Because each first conducting strip **311** is isolated from the adjacent second conducting strip **312** by one respective groove **22** of the insulative layer **20** to ensure electrical insulation characteristic, the invention effectively avoids from current leakage during transmission of test signals through the probe card **2** and provides the probe card **2** excellent test reliability. Further, the invention uses the insulation characteristic of the insulating layer **20** and the high stress capability of the support layer **10** to substitute for the ceramic substrate adopted by the aforementioned probe card **95** according to the prior art, thereby saving much cost and simplifying the circuit engineering.

FIGS. 6 and 7 show a vertical-type probe card **3** made according to a second embodiment of the present invention. The vertical probe card **3** is comprised of a circuit board **60**, a plurality of signal lines **70**, and a probe set **80**.

The circuit board **60** is prepared in the same way as the preparation of the circuit board of the cantilever probe card of the aforesaid first embodiment, comprising a plurality of first conducting strips **61**, second conducting strips **62**, grooves **63**, and a test hole **64** centered through the circuit board **60**. The signal lines **70** are respectively electrically connected to the first conducting strips **61** and second conducting strips **62**, and then inserted through the test hole **64** for connection to the probe set **80**.

The probe set **80** is a regular vertical pin structure provided at the bottom side of the circuit board **60** aligning with the test hole **64**, comprising a probe holder **81** and a plurality of probes **82** inserted through the probe holder **81**. The probe holder **81** is made of a shock absorbing and electric insulating material. The probes **82** are respectively electrically connected to the signal lines **70**, each having a tip for positively contacting with one respective electronic device of a semiconductor wafer to be tested.

During application, the outer part of the first conducting strips **61** and second conducting strips **62** of the circuit board **60** is electrically connected to the testing machine so that the probe card **3** transmits test signals from the testing machine to the electronic devices to be tested. The circuit board fabrication method of the present invention is applicable to the fabrication of most conventional probe cards to effectively avoid from current leakage during transmission of test signals. In addition to providing high quality probe cards, the invention greatly saves the probe card manufacturing cost and simplifies the manufacturing process.

Although particular embodiments of the invention have been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims

WHAT IS CLAIMED IS:

1. A method of making a low leakage probe card comprising the steps of:
 - a) providing a support layer made of a high hardness material having a predetermined flexural strength;
 - b) forming, on the support layer, an insulating layer having a plurality of grooves downwardly recessed from a top surface of the insulating layer to pattern a plurality of embosses relative to the grooves;
 - c) bonding a plurality of conducting strips to the embosses of the insulating layer respectively;
 - d) disposing a plurality of probes beneath the support layer for probing electronic devices; and
 - e) electrically respectively connecting the conducting strips and the probes by a plurality of signal lines.
2. The low leakage probe card fabrication method as claimed in claim 1, wherein the support layer and the insulating have a center test hole and the probes are located beneath the center test hole.
3. The low leakage probe card fabrication method as claimed in claim 2, wherein the support layer and the insulating layer have a plurality of through holes, which have a diameter greater than the diameter of the signal lines and surround the center test hole, and the signal lines are inserted respectively through the through holes in step e).
4. The low leakage probe card fabrication method as claimed in claim 3,

further comprising a sub-step of disposing a probe holder beneath the support layer and surrounded by the through holes for holding the probes to be suspended below the center test hole in step d).

5. The low leakage probe card fabrication method as claimed in claim 2, further comprising a sub-step of disposing a probe holder beneath the center test hole for vertically holding the probes to be suspended beneath the probe holder.

6. The low leakage probe card fabrication method as claimed in claim 1, wherein said insulating layer is prepared from an insulating material having a surface resistivity over $10^{13} \Omega/\text{cm}^2$ subject to ASTM (American Society for Testing and Materials) standards.

7. The low leakage probe card fabrication method as claimed in claim 6, wherein said insulating material is an engineering plastic material.

8. The low leakage probe card fabrication method as claimed in claim 7, wherein said grooves are engraved on said insulating material by mechanical processing in step b).

9. The low leakage probe card fabrication method as claimed in claim 6, wherein said insulating layer is made of a photoresist material.

10. The low leakage probe card fabrication method as claimed in claim 9, wherein said grooves are formed on said insulating material by photolithography

processing.

11. The low leakage probe card fabrication method as claimed in claim 1, wherein said support layer is prepared from a material having a flexural strength over 100kgs/cm² subject to ASTM (American Society for Testing and Materials) standards.

12. The low leakage probe card fabrication method as claimed in claim 11, wherein said support layer is prepared from one of the materials of metal, ceramics, and glass epoxy.

13. The low leakage probe card fabrication method as claimed in claim 1, wherein said signal lines are coaxial cables each having an axial wire and a grounded shielding layer coaxially surrounding said axial wire and insulated from said axial wire, and the axial wire and grounded shielding layer of each of said signal lines are respectively and electrically connected to each two adjacent conducting strips in step e).

14. A probe card for the connection of a testing machine electrically for probing electronic devices to be tested, comprising:

a circuit board comprising:

a support layer made of a high hardness material having a predetermined flexural strength;

an insulating layer formed on the support layer and provided with a plurality of grooves downwardly recessed from a top surface of the insulating layer to pattern a plurality of embosses having a plurality of

bonding surfaces relative to the grooves; and

a conducting layer including a plurality of conducting strips bonded to the bonding surfaces of the insulating layer respectively;

a plurality of probes disposed beneath the support layer for probing electronic devices; and

a plurality of signal lines inserted through the circuit board and electrically connecting the conducting strips and the probes respectively.

15. The probe card as claimed in claim 14, wherein said circuit board comprises a center test hole and the probes are located beneath the center test hole.

16. The probe card as claimed in claim 15, wherein the support layer and the insulating layer have a plurality of through holes, which have a diameter greater than the diameter of the signal lines and surround the center test hole, and the signal lines are respectively inserted through the through holes of said circuit board.

17. The probe card as claimed in claim 16, wherein said circuit board comprises a probe holder disposed beneath the support layer and surrounded by the through holes for holding the probes to be suspended below the center test hole.

18. The probe card as claimed in claim 15, wherein said circuit board comprises a probe holder disposed beneath the center test hole for vertically holding the probes to be suspended beneath the probe holder.

19. The probe card as claimed in claim 14, wherein said insulating layer is

prepared from a material having a surface resistivity over $10^{13} \Omega/\text{cm}^2$ subject to ASTM (American Society for Testing and Materials) standards.

20. The probe card as claimed in claim 19, wherein said insulating material is selected from one of the materials of engineering plastics and photoresist.

21. The probe card as claimed in claim 14, wherein said support layer is prepared from a high hardness material having a flexural strength over 100kgs/cm² subject to ASTM (American Society for Testing and Materials) standards.

22. The probe card as claimed in claim 21, wherein said support layer is prepared from one of the materials of metal, ceramic and glass epoxy.

23. The probe card as claimed in claim 14, wherein said signal lines are coaxial cables each having an axial wire and a grounded shielding layer coaxially surrounding said axial wire and insulated from said axial wire, and the axial wire and grounded shielding layer of each of said signal lines are respectively and electrically connected to each two adjacent ones of said conducting strips.

24. The probe card as claimed in claim 23, wherein said conducting strips include a plurality of first conducting strips and a plurality of second conducting strips, each of said second conducting strips being adjacent to at least one of said first conducting strips; the grounded shielding layers of said signal lines are respectively electrically connected to said first conducting strips; the axial wires of said signal lines are respectively electrically connected to said second conducting strips.

25. A method of making a circuit board for a probe card, the method comprising the steps of:

a) providing a support layer made of a high hardness material having a predetermined flexural strength;

b) forming an insulating layer on the support layer, the insulating layer having a plurality of grooves downwardly recessed from a top surface of the insulating layer to pattern a plurality of bonding surfaces relative to the grooves; and

c) bonding a plurality of conducting strips to the embosses of the insulating layer respectively.

26. A circuit board made according to the method of claim 25, comprising:

a support layer made of a high hardness material having a predetermined flexural strength;

an insulating layer formed on the support layer and provided with a plurality of grooves downwardly recessed from a top surface of the insulating layer to pattern a plurality of embosses having a plurality of bonding surfaces relative to the grooves; and

a conducting layer including a plurality of conducting strips bonded to the bonding surfaces of the insulating layer respectively.

27. The circuit board as claimed in claim 26, wherein said insulating layer is prepared from an insulating material having a surface resistivity over $10^{13} \Omega/\text{cm}^2$ subject to ASTM (American Society for Testing and Materials) standards.

28. The circuit board as claimed in claim 27, wherein said insulating material is an engineering plastic material.

29. The circuit board as claimed in claim 28, wherein said grooves are engraved on said insulating material by mechanical processing.

30. The circuit board as claimed in claim 27, wherein said insulating layer is made of a photoresist material.

31. The circuit board as claimed in claim 30, wherein said grooves are formed on said insulating material by photolithography processing.

32. The circuit board as claimed in claim 26, wherein said support layer is formed of a material having a flexural strength over 100kgs/cm² subject to ASTM (American Society for Testing and Materials) standards.

33. The circuit board as claimed in claim 32, wherein said support layer is formed of one of the materials of metal, ceramics, and glass epoxy.