LOW PROFILE INTREGRATED CIRCUIT PACKAGES

Abstract

The specification describes methods for manufacturing thin tiles for IC packages using thinning techniques. The method includes the step of thinning the IC devices in chip form. This is achieved at the final stage of assembly where the chips are flip-chip bonded to the substrate and the backside of the chips is exposed for thinning. Using this approach, final chip thickness of the order of 2-8 mils can be produced and overall package thickness is dramatically reduced.

This Sheet Has Been Replaced

