ABSTRACT

DUMMY LAYER DIODE STRUCTURES FOR ESD PROTECTION

Described are structures for a device with a controllable dummy layer which can provide a low controllable trigger voltage and can be used as a first triggered device in ESD protection networks. A controllable dummy layer diode is provided which is structured as a butting diode with a dummy polysilicon layer above the butting region. The dummy polysilicon layer functions as an STI block to remove the STI between the n+ and p+ regions of the diode. In one embodiment the diode has the function of a controllable gate with a punchthrough-like-trigger, in which a capacitor-couple circuit couples a portion of the ESD voltage into the gate of the diode to provide a gate voltage. By changing the channel length under the gate of the diode as well as the gate voltage, the reverse-biased voltage of the diode is readily adjusted to a predetermined level. In a second embodiment the p+ region of the diode overlaps the n+ region turning the diode into a zener diode. The low doping channel region under the dummy polysilicon layer functions as a channel stopper and suppresses the occurrence of the leakage current caused by the zener diode. The adjustment of the channel stopper length and the controllable gate voltage enables the controlling of a zener voltage. When ESD stress is present at the integrated circuit pad the diode, of either type, goes into a controllable voltage level breakdown.

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