

GROUND CONDUCTOR DISCONTINUITIES FOR THERMAL ISOLATION OF QUBIT CIRCUITS

BACKGROUND

[0001] The currently claimed embodiments of the present invention relate to quantum mechanical circuits, and more specifically, to a quantum mechanical circuit having an electrical conductor that is a poor thermal conductor.

[0002] In a typical printed circuit board (PCB), a relatively large continuous ground plane is generally provided. The return current from a signal running across the typical PCB travels uninhibited. While this may be desirable in a normal electrical application, in an electrical application where thermal isolation plays an important role, the electrically conductive continuous ground plane also thermally shorts together everything connected to it. This can create problems in any thermal gradient sensitive application.

[0003] Splitting the ground plane where signals need to cross a boundary between two split ground planes is usually avoided entirely in applications where a common electrical ground is needed. A conventional method to mitigate heat transmission is by using capacitors to bridge the gap between the two separated or split ground planes. For thermal gradient sensitive applications, PCBs are typically not used because of the aforementioned thermal shorting issue.

[0004] As a result, there remains a need for an electric circuit that reduces heat transmission while allowing electrical conduction. Therefore, it would be desirable to solve this and other problems of the prior art by providing a new kind of circuit for use in a quantum computer, for example a superconducting quantum computer, where heat dissipation or transmission is often not desirable.

SUMMARY

[0005] An aspect of the present invention is to provide a quantum mechanical circuit. The quantum mechanical circuit includes a substrate; a first electrical conductor and a second electrical conductor provided on the substrate and spaced apart to provide a gap therebetween; and a third electric conductor to electrically connect the first electrical conductor and the second electrical conductor. The third electrical conductor is a poor thermal conductor.

[0006] In an embodiment, the third electrical conductor comprises at least one of Copper-Nickel (CuNi) or stainless steel. In an embodiment, CuNi has an electrical resistivity that is approximately $3.8 \times 10^{-8} \Omega\text{m}$ at ambient temperature and a thermal conductivity that is between $25 \text{ W/m}^{\circ}\text{K}$ and $40 \text{ W/m}^{\circ}\text{K}$. In an embodiment, the first and second electrical conductors comprise copper (Cu). In an embodiment, the first, second and third electrical conductor are configured to transmit a radiofrequency electrical current. In an embodiment, the third electrical conductor is coupled to the substrate using fasteners. In an embodiment, the fasteners comprise brass. In an embodiment, the first and second electrical conductors are connected to electrical ground. In an embodiment, the first and second electrical conductors are electrically decoupled by providing a gap or a channel between the first and second electrical conductors within the substrate. In an embodiment, the quantum mechanical circuit further includes attenuator chips electrically coupled the first and second electrical conductors.

[0007] Another aspect of the present invention is a superconducting quantum mechanical computer. The superconducting quantum mechanical computer includes a refrigeration system comprising a temperature-controlled vessel; a quantum processor disposed within the temperature-controlled vessel, the quantum processor comprising a plurality of qubits; and a superconducting circuit disposed inside the temperature-controlled vessel. The superconducting circuit includes a substrate; a first electrical conductor and a second electrical conductor provided on the substrate and spaced apart to provide a gap therebetween; and a third electrical conductor to electrically connect the first electrical conductor and the second electrical conductor, the third electrical conductor being a poor thermal conductor. Each of the plurality of qubits is provided on the substrate and is at least electrically connected to ground via at least one of the first or second electrical conductors.

[0008] Yet another aspect of the present invention is to provide a method of manufacturing a quantum mechanical circuit. The method includes providing a substrate having a top face and a bottom face; forming a conductive layer on at least one of the top face and bottom face of the substrate; forming conductor lines in a selected pattern on the substrate by removing portions of the conductive layer, the conductor lines including a first electrical conductor and a second electrical conductor on the substrate, the first electrical conductor and the second electrical conductor being spaced apart and separated by a gap therebetween; and electrically connecting the first electrical conductor and the second

electrical conductor using a third electrical conductor, the third electrical conductor being a poor thermal conductor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present disclosure, as well as the methods of operation and functions of the related elements of structure and the combination of parts and economies of manufacture, will become more apparent upon consideration of the following description and the appended claims with reference to the accompanying drawings, all of which form a part of this specification, wherein like reference numerals designate corresponding parts in the various figures. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only and are not intended as a definition of the limits of the invention.

[0010] FIG. 1 is an electronic schematic of a quantum mechanical circuit 100, according to an embodiment of the present invention;

[0011] FIG. 2 is a three-dimensional perspective view of electrical coupling between the first electrical conductor, the second electrical conductor, and the third electrical conductor, according to an embodiment of the present invention;

[0012] FIG. 3 is a three-dimensional perspective view of a configuration of the first electrical conductor and the second electrical conductor, according to an embodiment of the present invention;

[0013] FIG. 4 is a schematic diagram showing a superconducting quantum mechanical computer, according to an embodiment of the present invention; and

[0014] FIG. 5 is a flow chart of a method of manufacturing the quantum mechanical circuit, according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0015] FIG. 1 is an electronic schematic of a quantum mechanical circuit 100, according to an embodiment of the present invention. The quantum mechanical circuit 100 includes a substrate 102. The quantum mechanical circuit 100 also includes a first electrical conductor 104, and a second electrical conductor 106 provided on the substrate 102. The quantum mechanical circuit 100 further includes a third electrical conductor 108 (shown in FIG. 2) to electrically connect the first electrical conductor 104 and the second electrical conductor 106. The third electrical conductor 108 is a poor thermal conductor. The term

“poor thermal conductor” is used herein broadly to mean the third electrical conductor 108 has a thermal conductivity substantially lower than a thermal conductivity of the first electrical conductor 104 and the thermal conductivity of the second electrical conductor 106. In an embodiment, the material of the third electrical conductor 108 (poor thermal conductor) can be selected to have a sufficiently low thermal conductivity such that the cooling apparatus (e.g., cooling vessel) in which the circuit 100 is used can sufficiently cool the circuit 100 to desired temperatures (e.g., temperatures of operation of the circuit). Selecting a material with a certain thermal conductivity is dependent on a system in which the circuit 100 is used. For example, if the cooling apparatus (e.g., cooling vessel) has enough cooling power, a material with a higher thermal conductivity can be acceptable.

[0016] FIG. 2 is a three-dimensional perspective view of electrical coupling between the first electrical conductor 104, the second electrical conductor 106, and the third electrical conductor 108, according to an embodiment of the present invention. As shown in FIG. 2, the third electrical conductor 108 is configured to electrically connect the first electrical conductor 104 and the second electrical conductor 106. In an embodiment, the third electrical conductor 108 includes at least one of Copper-Nickel (CuNi) or stainless steel. In an embodiment, CuNi has an electrical resistivity that is approximately $3.8 \times 10^{-8} \Omega\text{m}$ at ambient temperature and a thermal conductivity that is between about $25 \text{ W/m}^\circ\text{K}$ and $40 \text{ W/m}^\circ\text{K}$. However, as it must be appreciated other materials having poor thermal conductivity can also be used for the third electrical conductor 108.

[0017] In an embodiment, the first electrical conductor 104 and the second electrical conductor 106 include copper (Cu). A material of the third electrical conductor 108 is different from a material of the first electrical conductor 104 and a material of the second electrical conductor 106. In an embodiment, the material of the first electrical conductor 104 and the material of the second electrical conductor 106 can be substantially the same. For example, both the material of the first electrical conductor 104 and the material of the second electrical conductor 106 can be essentially copper (Cu) while the material of the third electrical conductor 108 is essentially CuNi and/or stainless steel. In an embodiment, the substrate 102 is an electrically non-conductive (electrically insulating) material such as silicon (Si), sapphire (Al_2O_3), printed circuit board material (e.g., FR-4 (woven glass and epoxy) or other laminate board, fiberglass), or a polymer (e.g., a polyimide), for example.

[0018] In an embodiment, the third electrical conductor 108 is coupled to the substrate 102 using fasteners 110. In an embodiment, the fasteners 110 include brass

fasteners, for example. However, other types of fasteners can also be used. In addition, in another embodiment, the third electrical conductor 108 can also be coupled to the substrate 102 using other means, such as by using an adhesive.

[0019] In an embodiment, the first electrical conductor 104, the second electrical conductor 106 and the third electrical conductor 108 are configured to transmit a radiofrequency (RF) electrical current. In an embodiment, the first electrical conductor 104 and the second electrical conductor 106 are connected to electrical ground potential.

[0020] In an embodiment, the first electrical conductor 104 and the second electrical conductor 106 are electrically decoupled by providing a discontinuity, a gap or a channel 112 between the first electrical conductor 104 and the second electrical conductor 106 within the substrate 102. The first electrical conductor 104 and the second electrical conductor 106 are spaced apart to provide the gap 112 therebetween.

[0021] FIG. 3 is a three-dimensional perspective view of a configuration of the first electrical conductor 104 and the second electrical conductor 106, according to an embodiment of the present invention. As shown in FIG. 3, a discontinuity, a gap or channel 112 is provided between the first electrical conductor 104 and the second electrical conductor 106. In embodiment, as shown in FIG. 3, two layers 116A and 116B can be used for signal transmission. For example, the discontinuity, channel or gap 112 in layers 116A and 116B provides improved thermal isolation and helps steer return current. This dual sided configuration provides an increase in density. In addition, in an embodiment, the top and bottom split locations 112 are offset by removing internal ground planes from the internal layers of the substrate 102 (not shown) and by providing blind vias (i.e., vias on layers 116A and 11B that are not aligned with each other) to reduce electrical coupling.

[0022] Furthermore, as shown in FIG. 3, attenuator chips 114 can be provided on top and bottom sides of layers 116A and 116B to increase electrical signal isolation. The attenuator chips 114 are electrically coupled (e.g., wire-bonded or soldered, etc.) to the first and second electrical conductors 104 and 106. In an embodiment, the attenuator chips 114 can be wire-bonded or soldered (for example, either surface mount soldered or ball grid array soldered) across the ground split 112. In addition, in other embodiments, other types of components, such as a filter for example, can also be used in addition or alternatively to the attenuator chips 114. In an embodiment, as shown in FIG. 3, removing ground planes internal to the substrate 102 (not shown) by providing the discontinuity or gap 112 in both

layers 116A and 116B allows to reduce coupling to increase thermal isolation. Furthermore, vias 118 can be arranged within the substrate 102 (not shown) to allow electrical signals to have proper electromagnetic mode conversion to reduce coupling. In this way, electromagnetic (EM) fields can use the electrical ground potential more efficiently for return current path across the discontinuity 112 in the ground planes (i.e., the discontinuity or gap or channel 112 between the first electrical conductor 104 and the second electrical conductor in both layer 116A and layer 116B). The electrical ground potential is thus provided by the first electrical conductor 104, the second electrical conductor 106 and the third electrical conductor 108 connected to each other and to ground.

[0023] Therefore, as it can be appreciated from the above paragraphs, in some embodiments of the present invention, the problem of thermal isolation can be addressed by splitting the ground plane. The ground plane corresponds to the first electrical conductor 104 and the second electrical conductor 106 both connected to electrical ground potential. The splitting in the ground plane thus corresponds to the gap or discontinuity or channel 112 provided between the first electrical conductor 104 and the second electrical conductor 106. While the gap or channel 112 provides good thermal isolation, this may cause many issues with the return current path. As a result, the third electrical conductor 108 is provided to electrically connect the first electrical conductor 104 and the second electrical conductor 106. However, to provide thermal isolation between the first electrical conductor 104 and the second electrical conductor 106 (in the ground plane in this example), the third electrical conductor 108 is selected as being a poor thermal conductor such as CuNi alloy or Stainless steel, for example. CuNi is relatively a good electrical conductor but a poor thermal conductor.

[0024] FIG. 4 is a schematic diagram showing a superconducting quantum mechanical computer 200, according to an embodiment of the present invention. The superconducting quantum mechanical computer 200 includes a refrigeration system comprising a temperature-controlled vessel 202. The superconducting quantum computer includes a quantum processor 204 disposed within the temperature-controlled vessel 202, the quantum processor including a plurality of qubits 206. The superconducting quantum mechanical computer 200 further includes the quantum mechanical circuit 100 disposed inside the temperature-controlled vessel 202. As shown in FIG. 1, the circuit 100 includes the substrate 102, the first electrical conductor 104 and the second electrical conductor 106 provided on the substrate 102. The circuit 100 also includes the third electrical conductor

108 for electrically connecting the first electrical conductor 104 and the second electrical conductor 106, the third electrical conductor 108 being a poor thermal conductor. Each of the plurality of qubits 206 is provided on the substrate 102 and is at least electrically connected to ground via at least one of the first or second electrical conductors 104 and 106.

[0025] FIG. 5 is a flow chart of a method of manufacturing the quantum mechanical circuit, according to an embodiment of the present invention. The method includes:

1. providing the substrate 102 (e.g., silicon, polymer, laminate board, fiberglass, etc.) having a top face and a bottom face, at S100;
2. forming a conductive layer (e.g., copper layer) on at least one of the top face and bottom face of the substrate, at S102;
3. forming conductor lines in a selected pattern on the substrate 102 by removing portions of the conductive layer, the conductor lines including first electrical conductor 104 and second electrical conductor 106 on the substrate 102, the first electrical 104 and second electrical conductor 106 being spaced apart and separated by a gap therebetween, at S104; and
4. electrically connecting the first electrical conductor 104 and the second electrical conductor 106 using a third electrical conductor 108 (shown in FIG. 2), the third electrical conductor 108 is a poor thermal conductor (e.g., CuNi or stainless steel), at S106. In an embodiment, the first and second electrical conductors 104 and 106 can be connected to electrical ground.

[0026] The method further includes, before forming the conductor lines in the selected pattern on the substrate 102:

5. applying a photoresist layer on the conductive layer;
6. applying a light absorbing material on the photoresist layer in the selected pattern so as to cover portions of the photoresist layer corresponding to the selected pattern;
7. irradiating the photoresist layer with electromagnetic radiation (e.g., ultraviolet radiation) to harden areas of the photoresist layer that are not covered by the light absorbing material;
8. removing areas of the photoresist layer corresponding to the covered portions of the photoresist layer that are not hardened by the electromagnetic radiation to expose portions of the conductive layer;

9. etching away the exposed portions of the conductive layer while not etching portions of the conductive layer under the hardened areas of the photoresist;
10. removing the hardened areas of the photoresist layer to expose portions of the conductive layer that are not etched, the portions of the conductive layer not etched corresponding to the selected pattern to form the conductor lines; and
11. forming vias within the substrate at selected locations within the substrate.

[0027] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A quantum mechanical circuit comprising:
 - a substrate;
 - a first electrical conductor and a second electrical conductor provided on the substrate and spaced apart to provide a gap therebetween; and
 - a third electrical conductor to electrically connect the first electrical conductor and the second electrical conductor,wherein the third electrical conductor is a poor thermal conductor.
2. The quantum mechanical circuit according to claim 1, wherein the third electrical conductor comprises at least one of Copper-Nickel (CuNi) or stainless steel.
3. The quantum mechanical circuit according to claim 2, wherein CuNi has an electrical resistivity that is approximately $3.8 \times 10^{-8} \Omega\text{m}$ at ambient temperature and a thermal conductivity that is between about $25 \text{ W/m}^\circ\text{K}$ and $40 \text{ W/m}^\circ\text{K}$.
4. The quantum mechanical circuit according to any one of the preceding claims, wherein the first and second electrical conductors comprise copper (Cu).
5. The quantum mechanical circuit according to any one of the preceding claims, wherein the first, second and third electrical conductor are configured to transmit a radiofrequency electrical current.
6. The quantum mechanical circuit according to any one of the preceding claims, wherein the third electrical conductor is coupled to the substrate using fasteners.
7. The quantum mechanical circuit according to claim 6, wherein the fasteners comprise brass.

8. The quantum mechanical circuit according to any one of the preceding claims, wherein the first and second electrical conductors are connected to electrical ground.
9. The quantum mechanical circuit according to any one of the preceding claims, wherein the first and second electrical conductors are electrically decoupled by providing the gap between the first and second electrical conductors within the substrate.
10. The quantum mechanical circuit according to any one of the preceding claims, further comprising attenuator chips electrically coupled the first and second electrical conductors.
11. A superconducting quantum mechanical computer comprising:
a refrigeration system comprising a temperature-controlled vessel;
a quantum processor disposed within the temperature-controlled vessel, the quantum processor comprising a plurality of qubits; and
a superconducting circuit disposed inside the temperature-controlled vessel, the superconducting circuit comprising:
a substrate;
a first electrical conductor and a second electrical conductor provided on the substrate and spaced apart to provide a gap therebetween; and
a third electric conductor to electrically connect the first electrical conductor and the second electrical conductor, the third electrical conductor being a poor thermal conductor,
wherein each of the plurality of qubits is provided on the substrate and is at least electrically connected to ground via at least one of the first or second electrical conductors.
12. The superconducting quantum mechanical computer according to claim 11, wherein the third electrical conductor comprises at least one of Copper-Nickel (CuNi) or stainless steel.

13. The superconducting quantum mechanical computer according to claim 12, wherein CuNi has an electrical resistivity that is approximately $3.8 \times 10^{-8} \Omega\text{m}$ at ambient temperature and a thermal conductivity that is between about $25 \text{ W/m}^{\circ}\text{K}$ and $40 \text{ W/m}^{\circ}\text{K}$.
14. The superconducting quantum mechanical computer according to any one of claims 11 to 13, wherein the first and second electric conductors comprise copper (Cu).
15. The superconducting quantum mechanical computer according to any one of claims 11 to 14, wherein the first, second and third electrical conductor are configured to transmit a radiofrequency electrical current.
16. The superconducting quantum mechanical computer according to any one of claims 11 to 15, wherein the third electrical conductor is coupled to the substrate using fasteners.
17. The superconducting quantum mechanical computer according to any one of claims 11 to 16, wherein the first and second electrical conductors are connected to electrical ground.
18. The superconducting quantum mechanical computer according to any one of claims 11 to 17, wherein the first and second electrical conductors are electrically decoupled by providing the gap between the first and second electrical conductors within the substrate.
19. The superconducting quantum mechanical computer according to any one of claims 11 to 18, further comprising attenuator chips electrically coupled to the first and second electrical conductors.
20. A method of manufacturing a quantum mechanical circuit comprising:
providing a substrate having a top face and a bottom face;
forming a conductive layer on at least one of the top face and bottom face of the substrate;

forming conductor lines in a selected pattern on the substrate by removing portions of the conductive layer, the conductor lines including a first electrical conductor and a second electrical conductor on the substrate, the first electrical conductor and the second electrical conductor being spaced apart and separated by a gap therebetween; and

electrically connecting the first electrical conductor and the second electrical conductor using a third electrical conductor, the third electrical conductor being a poor thermal conductor.