WHAT IS CLAIMED IS:

1. A semiconductor wafer assembly, comprising:

a first wafer including a first surface and an integrated circuit;

a second wafer having a first surface and a second surface, the first surface is bonded to the first wafer, wherein the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer including an integrated circuit, and having a first surface that is bonded to the second surface of the second wafer, thereby encapsulating the semiconductor die within the cavity,

wherein the wafer assembly is configured to produce one or more stacked integrated circuits, each including one or more encapsulated semiconductor dies, when the wafer assembly is diced, and the second wafer includes an active integrated circuit interconnected to the integrated circuits of the first wafer and third wafer.

2. The semiconductor wafer assembly of claim 1, wherein the semiconductor die is mechanically and electrically connected to the first wafer by at least one of a bump bond, a wire interconnection, an ultrasonic bond, and an oxide bond.

3. The semiconductor wafer assembly of claim 1, wherein the cavity is hermetically sealed to encapsulate the semiconductor die.

4. The semiconductor wafer assembly of claim 1, wherein the integrated circuit of the third wafer is proximate the first surface of the third wafer and electrically connected to the first and second wafers.

5. The semiconductor wafer assembly of claim 1, wherein the integrated circuit of the first wafer is proximate the first surface of the first wafer that is electrically connected to the second and third wafers.

6. The semiconductor wafer assembly of claim 1, further comprising at least one electrical path to the semiconductor die through at least one of the first, second and third wafers to an exterior surface of the wafer assembly.

7. The semiconductor wafer assembly of claim 1, further comprising one or more thermal interfaces between the semiconductor die and one or more of the first, second, and third wafers.

8. The semiconductor wafer assembly of claim 1, wherein the second wafer and the third wafer are bump bonded so as to define an air gap providing thermal isolation from the cavity.

9. The semiconductor wafer assembly of claim 1, wherein the integrated circuit of the first wafer is proximate the first surface, and the first wafer includes electrical paths through the first wafer to the integrated circuit.

10. The semiconductor wafer assembly of claim 1, wherein:
    the second surface of the second wafer and the first surface of the third wafer each include an oxide layer; and
    the second wafer and the third wafer are oxide bonded together at their respective oxide layers.

11. The semiconductor wafer assembly of claim 1, wherein one or more of the first, second and third wafers defines a conduit to the cavity from the exterior of the wafer assembly.

12. The semiconductor wafer assembly of claim 11, wherein the conduit and the cavity are at least partially filled with a thermally conductive material.

13. The semiconductor wafer assembly of claim 11, wherein the conduit and the cavity are evacuated and sealed providing a vacuum package.

14. The semiconductor wafer assembly of claim 11, wherein the conduit and the cavity are evacuated and backfilled with a liquid or gas before scaling.

15. The semiconductor wafer assembly of claim 1, wherein the semiconductor die further comprises at least one oxide layer oxide bonded to at least one of the first wafer and the third wafer.

16. A semiconductor wafer assembly, comprising:

a first wafer including an integrated circuit and a first surface;

a second wafer having a first surface and a second surface, the first surface is bonded to the first wafer, wherein the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer including an integrated circuit, and having a first surface that is bonded to the second surface of the second wafer, thereby encapsulating the semiconductor die within the cavity,

wherein the integrated circuit of the third wafer is proximate the first surface of the third wafer and electrically connected to the first and second wafers.

17. A semiconductor wafer assembly, comprising:

a first wafer including an integrated circuit and a first surface;

a second wafer bonded to the first wafer such that the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer including an integrated circuit and being bonded to the second wafer such that the semiconductor die is encapsulated within the cavity,

wherein the integrated circuit of the first wafer is proximate the first surface of the first wafer that is electrically connected to the second and third wafers.

18. A semiconductor wafer assembly, comprising:

a first wafer;

a second wafer bonded to the first wafer such that the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer;

a third wafer bonded to the second wafer, thereby encapsulating the semiconductor die within the cavity, and one or more thermal interfaces between the semiconductor die and one or more of the first, second, and third wafers.

19. A semiconductor wafer assembly, comprising: a first wafer;

a second wafer bonded to the first wafer such that the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer bonded to the second wafer, thereby encapsulating the semiconductor die within the cavity,

wherein the second wafer and the third wafer are bump bonded so as to define an air gap providing thermal isolation from the cavity.

20. A semiconductor wafer assembly, comprising:

a first wafer;

a second wafer bonded to the first wafer, wherein the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer bonded to the second wafer, thereby encapsulating the semiconductor die within the cavity,

wherein one or more of the first, second and third wafers defines a conduit to the cavity from the exterior of the wafer assembly.

21. A semiconductor wafer assembly, comprising:

a first wafer including an integrated circuit;

a second wafer bonded to the first wafer, wherein the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer including an integrated circuit, and bonded to the second wafer, thereby encapsulating the semiconductor die within the cavity,

wherein the second wafer includes an active integrated circuit interconnected to the integrated circuits of the first wafer and third wafer.

22. A semiconductor wafer assembly, comprising:

a first wafer including an integrated circuit, and having a first surface that includes an oxide layer; a second wafer having a first surface and

a second surface, the first surface including an oxide layer that is bonded to the oxide layer of the first semiconductor wafer, wherein the first wafer and the second wafer define a cavity;

a semiconductor die within the cavity mechanically and electrically connected to the first wafer; and

a third wafer including an integrated circuit, and having a first surface that is bonded to the second surface of the second wafer, thereby encapsulating the semiconductor die within the cavity,

wherein the semiconductor die further comprises at least one oxide layer oxide bonded to at least one of the first wafer and the third wafer.