

DUAL OUTPUT DIGITAL FILTER AND TELEVISION RECEIVER
INCLUDING SUCH A FILTER.

1 This invention relates to digital filters, and, in particular,
to digital filter networks which produce two output signals at outputs
which exhibit different response characteristics with respect to the input
signal. The invention also relates to a television receiver including
5 such a filter.

 In television receivers in which the baseband
video signal is processed in digital form, it is frequently
desirable to separate signals which occupy contiguous bands
of frequencies. For instance, when a video signal is comb
10 filtered over the full video bandwidth to separate the
interleaved luminance and chrominance signal components,
some luminance information will be contained in the low-
frequency portion of the signal produced in what is commonly
termed the chrominance channel of the comb filter. This
15 luminance information, termed the vertical detail
information, must then be separated from the higher
frequency combed chrominance signal and recombined with
the combed luminance signal to provide a fully restored
luminance signal. In the NTSC television system, the
20 chrominance signal extends down to about 1.5 MHz below
the color subcarrier frequency of 3.58 MHz, and the vertical
detail information is contained in the lower 1.0 MHz of the
signal produced in the chrominance channel of the comb filter.
The luminance and chrominance signal components of the
25 output signal of the chrominance channel may be separated
between the upper frequency of the vertical detail signal,
1.0 MHz, and the lower frequency of the chrominance signal
of approximately 2.1 MHz.

 An arrangement for separating the vertical detail
30 information and the chrominance information at the output
of the chrominance comb filter is shown in U.S. Patent
4,096,516. In that arrangement, the video signal is comb
filtered by a sampled data system comprising a charge
coupled device (CCD) comb filter. The combed chrominance
35 signal at the output of the chrominance comb filter is
separated by two filters, each including lumped frequency
selective filter elements. A lowpass filter having a
passband of 0 to 1.5 MHz separates the vertical detail
information from the chrominance information, and couples

1 the vertical detail information to the luminance signal
at the output of the luminance comb filter. A bandpass
filter couples bandpassed chrominance signals from the
output of the chrominance comb filter to a chrominance
5 signal processor.

In a digital television receiver, in which the
luminance and chrominance signals are separated by a
digital comb filter, it is likewise desirable to separate
the vertical detail information from the chrominance
10 information for recombination with the combed luminance
signal when the video signal is comb filtered over the
full band of video frequencies. In order to minimize the
number of circuit elements required to perform the
separation, it is desirable to use a single filter having
15 a lowpass filter output for the vertical detail information
and a bandpass filter output for the chrominance signal.

In accordance with a preferred embodiment of
the present invention, a digital filter is provided which
processes an input signal, and produces two output signals
20 which have different response characteristics with respect
to the input signal. This filter comprises a delaying
means which is responsive to the input signal. The delaying
means comprises a shift register having a plurality of
signal taps, and a given delay from input to output. The
25 delaying means also produces the input signal delayed by
at least half the given delay of the shift register. The
filter also comprises a signal coupling means coupled to
the signal taps of the shift register. The signal means
weights the signals passing through it. The filter also
30 comprises a means for summing the tap weighted signals of
the signal coupling means in cooperation with the shift
register. Finally, the filter comprises two signal
combining means. The first combines the tap-weighted sum
with the delayed input signal in one sense to generate
35 the first output signal. The second combines the tap-
weighted sum with the delayed input signal in a different
sense to generate the second output signal.

In a first embodiment, an output tap weighted FIR

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filter is constructed in accordance with

the present invention to provide both a bandpassed
5 output signal for passing the chrominance information,
and a lowpassed output signal for passing the vertical
detail information. In a second embodiment, an input tap
weighted FIR filter is arranged in accordance with
the present invention to provide the filtered
10 output signals.

In the drawings:

FIGURE 1 illustrates, in block diagram form, the
baseband digital signal processing section of a television
receiver, constructed in accordance with
15 the present invention;

FIGURE 2 illustrates, in block diagram form, an
output tapped FIR filter constructed in accordance with
the principles of the present invention;

FIGURE 3 illustrates, in block diagram form and in
20 more detail, a modification of the FIR filter of FIGURE 2;

FIGURE 4 illustrates, in block diagram form, an
input tap weighted FIR filter in accordance
with the present invention; and

FIGURES 5, 6 and 7 illustrate response
25 characteristic curves used to explain the operation of the
embodiments of FIGURES 1 through 4.

Referring to FIGURE 1, the baseband digital
signal processing section of a television receiver,
in accordance with the
30 present invention, is illustrated in block diagram form.
Video signals are supplied from a source of video signals 10
which may comprise, for instance, a video detector in a
television receiver. The video signals are applied to
an analog to digital converter 12, which converts the analog
35 video signals to digital signals in the form of successive
eight-bit words, for instance. In this and subsequent
embodiments of the present invention, the broad arrows
shown in the drawing figures represent parallel lines of
digital information which couple digital words of a plurality

1 of bits from one element to another. The digital signals
are applied to the input of a digital comb filter 14,
5 which separates the signals into separate luminance (Y)
and chrominance (C) components. The digital comb filter
14 may be constructed to operate as described in the
article "Digital Television Image Enhancement" by John P.
Rossi, 84 SMPTE at 545-51 (1974).

10 The separated Y signal is applied by way of
a delay element 16 to an input of an adder 30. The delay
of the delay element 16 is chosen to substantially match
the delay encountered by a vertical detail signal as it is
processed by a combination bandpass and lowpass filter
15 network 20. The combination bandpass/lowpass filter
network 20 is coupled between the C output of the comb
filter 14 and a second input of adder 30 and produces
lowpass filtered vertical detail information. The adder
30 combines the vertical detail information signal with
20 the combed luminance signal to produce a restored
luminance signal. The restored Y signal is applied to
one input of an adder 32.

The bandpass/lowpass filter 20 is coupled to
supply the vertical detail information to the input of a
25 nonlinear detail signal processor 34 also. The nonlinear
processor 34 exhibits a nonlinear transfer function
as shown in FIGURE 1 and described on pages 12-15 of the
article "A CCD Comb Filter for Color TV Receiver Picture
Enhancement: by D.H. Pritchard, and published in Volume
30 41 of the RCA review at pages 3, et. seq. (March, 1980).
The nonlinear processor 34 operates to core low amplitude
signals, to peak intermediate amplitude signals, and to
pare, or attenuate, high amplitude signals. The nonlinear
processor 34 may comprise, for example, a random access
35 memory (RAM), with the transfer function applied to the
vertical detail information being a function of data
stored in the RAM under control of a processor (not shown).
New data may be stored in the RAM by processor control of
a read/write control line 38 and RAM address lines 36

1 during inactive video intervals, such as the vertical
blanking interval. The processed vertical detail signal
5 is applied to the other input of adder 32 as a peaking
signal. The peaked Y signal produced at the output of
adder 32 is applied to luminance signal processing
circuitry 40, which may be controlled to modify the
brightness and contrast of the luminance signal. The
10 processed luminance signal Y' at the output of processing
circuitry 40 is applied to an input of a matrix 60. The
chrominance signal processing circuitry 50 may comprise a chroma peaker
and a color mixture signal demodulator, as described in UK Patent applic-
ation 8223987 corresponding to US Patent application Number 297,556,
15 entitled "DIGITAL COLOR TELEVISION SIGNAL DEMODULATOR",
filed August 31, 1981. The chrominance signal processing
circuitry 50 produces demodulated color mixture signals,
such as color difference signals (B-Y) and (R-Y) or I and
Q signals. The color mixture signals are applied to the
20 matrix 60. The matrix 60 combines the color mixture
and luminance signals to produce red, green and blue color
signals, which are then converted to analog form by a
digital to analog converter 54 for application to a
television kinescope (not shown).

25 In the arrangement of FIGURE 1, the bandpass/
lowpass filter network 20 serves to separate the vertical
detail information, contained in the low frequency portion
of the signal produced by the chrominance comb filter,
from the chrominance information contained in the high
30 frequency portion of the signal produced by the chrominance
comb filter. The filter network 20 produces bandpass
filtered chrominance signals, free of luminance signal
components, for application to the chrominance signal
processing circuitry. The filter network 20 also produces,
35 at a separate output, lowpass filtered vertical detail
information for the luminance channel, free of chrominance
signal residue which could create "dot crawl" on edges of
the restored luminance signal.

A bandpass/lowpass filter network, suitable for use in the arrangement of FIGURE 1 and constructed in accordance with the present invention, is shown in FIGURE 2. The network of FIGURE 2 comprises an output tap weighted digital FIR filter, including a tapped shift register 100, weighting function circuits 102-118, and an adder tree arrangement 120-140.

In FIGURE 2, combed chrominance signals in the form of, for example, eight-bit words, are applied to the first stage of shift register 100. Each stage of the shift register 100 is capable of temporarily storing and transferring a word of the chrominance signal under control of a clock signal. Thus, each stage of the shift register 100, numbered one through twenty-one can simultaneously hold eight bits. The shift register 100 exhibits a delay from the input of the first stage to the output of the last stage which is a function of the number of stages and the frequency of the clock signal which shifts the signals through the register. The arrangement of FIGURE 2 therefore comprises a 21-order FIR filter with taps being coupled to the outputs of stages one, five, nine, eleven, thirteen, seventeen and twenty-one.

The weighting function circuits 102-118 are coupled to the output taps of shift register 100 and multiply the tapped signals by the fractional coefficients shown in the FIGURE. The FIR filter exhibits an impulse response which is relatively concentrated and symmetrical about the tapped center stage eleven. Signals from stage eleven are weighted by one-half in this example by weighting function circuit 102 and the tap-weighted signals are then applied to an input of an adder 130, and to an input of a subtractor 140. Signals from stages nine and thirteen, both located two stages away from the center stage eleven, are weighted by the coefficient $+(5/16)$ by weighting

function circuits 104 and 114 respectively, and applied to inputs of adder 120. Signals from stages five and seventeen, both located six stages away from the center stage, are weighted by the coefficient $-(5/64)$ by weighting function circuits 106 and 116 respectively, and applied to inputs of an adder 122. Signals from stages one and twenty-one, both located ten stages away from the center stage, are weighted by the coefficient $+(1/64)$ by weighting function circuits 108 and 118 respectively, and applied to inputs of an adder 124. The symmetrical distribution of tapped stages one, five and nine, and thirteen, seventeen and twenty-one and the symmetrical weighted values of this distribution about the center stage eleven give this FIR filter a linear phase characteristic.

The outputs of adders 122 and 124 are coupled to inputs of an adder 126, which combines the applied signals and has an output coupled to an input of an adder 128. Adder 128 combines signals produced by adder 126 with signals provided by adder 120, and has its output coupled to an input of adder 130. Adder 130 combines the tap-weighted signals summed in adder 128 with the center tap-weighted signal, and exhibits a lowpass filter response characteristic at its output. Lowpass filtered vertical detail signals are thus produced at the output of adder 130.

The combined tap-weighted signals at the output of adder 128 are also applied to an input of subtractor 140, where they are subtractively combined with the weighted center tap signals. Subtractor 140 thereby exhibits a bandpass filter response characteristic at its output, which is a complement of the response characteristic at the output of adder 130. Bandpass filtered chrominance signals are produced at the output of subtractor 140. Thus, a single filter is used to provide both lowpass filtering and bandpass filtering.

1 A more detailed embodiment of the FIR filter of
FIGURE 2 is illustratively shown in FIGURE 3. Since the
weighting function coefficients of FIGURE 2 all have
denominators which are powers of two, the tapped signals
5 may be weighted by a shift-and-add technique, as shown in
FIGURE 3, which obviates the need for coefficient
multipliers. For example, because signals from shift
register stages nine and thirteen are both weighted by
the same coefficient value of $(5/16)$, these two signals
10 may be added in adder 120 before weighting, as shown in
FIGURE 3. If, as in this example, the tapped signals are
each eight bits in length, the output of adder 120 will be
a nine-bit word. The nine-bit output of adder 120 is
15 divided by sixteen, as indicated by block 154, and by four,
as indicated by block 156, in the coupling of adder 120 to
the inputs of an adder 158.

In decimal arithmetic, division of a number by
a power of 10 can be thought of either as shifting the
decimal point one digit to the left, or as shifting the
20 digits of the number one digit to the right. Similarly,
in binary arithmetic, division of a number by a power of
two can be thought of either as shifting the binary point
one bit to the left, or as shifting the bits of the number
one bit to the right. The nine-bit output of adder 120
25 is divided by sixteen by coupling only the five most
significant bits of the output to the low-order bit inputs
of one input of adder 158, thus shifting the bits
four bits to the left and is divided by four by
30 coupling the seven most significant bits to the lower
order bit inputs of a second input of adder 158 thus
shifting the bits two bits to the left. Adder 158
adds these two words to produce an eight-bit output
signal, which is the sum of $(1/16)$ plus $(1/4)$, or $(5/16)$ of
the values of the tapped signals. This is the desired
35 weighting coefficient for signals tapped from stages nine
and thirteen.

1 In a similar manner, signals tapped from shift
register stages five and seventeen are summed in adder 122,
10 which produces a nine-bit output signal. The output of
adder 122 is divided by sixty-four and by sixteen in its
5 coupling to the two inputs of an adder 160, as indicated
by blocks 162 and 164 respectively. Adder 160 produces
a six-bit output signal which is weighted by $(5/64)$
with respect to the tapped signals. This output signal
10 is inverted by an inverting circuit 170 and applied to
an input of adder 126, together with a logical "1"
carry-in bit. The signal inversion and the carry-in
bit perform a two's complementing of the output of adder
160, which in binary arithmetic effectively provides the
15 minus sign for the weighting coefficient.

Signals tapped from shift register stages one and
twenty-one are summed in adder 124, the output of which is
divided by sixty-four by coupling the three most significant
output bits of adder 124 to the second input of adder 126,
20 as indicated by block 166. The output of adder 126 is
coupled to one input of adder 128, and the output of adder
158 is coupled to a second input of adder 128. Adder 128
produces an output signal which is the sum of weighted
signals from all of the shift register taps except the
25 center tap eleven.

The output of adder 128 is coupled to one input
of adder 130. The seven most significant bits of the
signal tapped from center stage eleven are coupled to the
second input of adder 130, as connoted by block 152. Adder
30 130 thereby exhibits a lowpass filter characteristic at its
output, at which the vertical detail information of the
input signal is produced.

The seven most significant bits of the signal
35 tapped from center stage eleven are coupled to one input of

1 an adder 180. The output of adder 128 is coupled to a
second input of adder 180 by an inverting circuit 172,
together with a logical "1" carry-in bit. The inversion of
the output signal of adder 128 along with the carry-in
5 bit provide a two's complementing of the output signal of
adder 128. This causes the output signal of adder 128
to be subtracted from the weighted center tap signal in
adder 180, causing adder 180 to exhibit a bandpass filter
response characteristic at its output. Bandpass filtered
10 chrominance information is thereby produced at its output.

The operation of the embodiments of FIGURES 2 and
3 may be appreciated by referring to the response character-
istic curves of FIGURES 5, 6 and 7. FIGURE 5 illustrates
the response characteristic 200 exhibited at the output
15 of adder 128, when the shift register 100 is clocked by
a 14.32 MHz signal. This response characteristic 200 is
seen to have substantially equal amplitude variations
about a midpoint value of 0.00.

When weighted signals from the center tapped
20 stage eleven are additively combined with signals
produced by adder 128 in adder 130, a response characteristic
as shown in FIGURE 6 results at the output of adder 130.
This is because the center tap eleven exhibits a flat
amplitude versus frequency response which has a constant
25 amplitude of one-half relative to the peak-to-peak
amplitude of the curve 200 of FIGURE 5. The one-half
amplitude value results from the value of the center tap
weighting coefficient of one-half. Adder 130 thus
effectively combines response curve 200 with a flat response
30 characteristic of substantially one-half its relative
amplitude, thereby raising the response curve 200 by
one-half with respect to the relative amplitude scale
shown at the ordinate of FIGURE 5. The result is response
curve 210 of FIGURE 6, in which the 0.00 value is now
35 located at the bottom of the response curve. Response curve
210 thus defines a lowpass filter response from zero Hz. to
a six dB point at about 1.8 MHz, and a highpass filter
above approximately 5.2 MHz, with a stopband interposed in
the intermediate frequency range. However, since the video

frequency range in the NTSC television system extends to only about 4.2 MHz, the highpass portion of the response contains essentially no signal content in the television receiver. The lowpass filter portion, then defines a passband for lowpass filtered vertical detail information signals at the output of adder 130.

When the output signals of adder 128 are two's complemented for combination with the center tap weighted signals in adder 180 (or subtractor 140), the response characteristic 200 of FIGURE 5 is essentially inverted about the median 0.00 value. The combination of the tapped signals from the center stage, weighted by one-half, effectively relocates the 0.00 scale value at the bottom of the inverted response characteristic, as shown by response characteristic 220 of FIGURE 7. Response characteristic 220 is seen to define a bandpass filter characteristic with a passband between approximately 1.8 MHz and 5.2 MHz. Since the chrominance passband terminates at approximately 4.1 MHz, adder 180 (or subtractor 140) will pass the chrominance signal of a television receiver in the passband of approximately 1.8 to 4.1 MHz.

The bandpass/lowpass filter network of the present invention may also be configured as an input tapped FIR filter, as shown in the arrangement of FIGURE 4. In this embodiment a twenty-stage shift register 302 is used in the FIR filter, with adders 320-328 inserted between four-stage segments of the shift register. Weighted input signals from the combed chrominance signal applied to the filter input 300 are applied to the input of the first stage of the shift register 302 and to the intervening adders. The shift register stages are clocked by a common clock signal.

The combed chrominance input signal is applied to the input of the first stage and to an input of an adder 330 by weighting function circuits 304 and 316 respectively, which weight the applied signals by $+(1/64)$. Adder 330 has a second input coupled to the output of the last shift register

1 stage twenty. The input signal is applied to an input of
an adder 320, which is coupled between shift register
stages four and five, by a weighting function circuit 306.
5 The input signal is also applied to an input of an adder 328,
which is coupled between shift register stages sixteen and
seventeen, by a weighting function circuit 314. Weighting
function circuits 306 and 314 weight the input signals by
a factor of $-(5/64)$. The input signal is weighted by a
10 factor of $+(5/16)$ by weighting function circuits 308 and
312, which are coupled to inputs of adders 322 and 326
respectively. Adder 322 is coupled between shift register
stages eight and nine, and adder 326 is coupled between
shift register stages twelve and thirteen.

15 The impulse response of the FIR filter of
FIGURE 4 is concentrated around the junction of shift
register stages ten and eleven, which is located
equidistantly between the first and last stages. Weighted
signal components are accumulated in the adders as they
20 pass through the shift register and adders, with the
response characteristic of FIGURE 5 being exhibited at
the output of adder 330. Signals at the output of adder 330
are applied to an input of an adder 340 for combination
with signals provided by a shift register 360. The shift
25 register 360 receives input signals which have been
weighted by one-half by weighting function circuit 310,
and delays these signals by the same amount of delay time
as exhibited by the FIR filter from its impulse response
center at the output of stage ten to the output of adder 330.
30 Signals at the output of shift register 360 thus correspond
to the center tap weighted signals of the embodiments of
FIGURES 2 and 3. Therefore, adder 340 will exhibit the
lowpass filter response characteristic of FIGURE 6 at its
output, at which the vertical detail information signals
35 are provided.

Signals developed at the output of adder 330
are two's complemented for subtractive combination with
signals provided by a shift register 360 in an adder 350.
The output of adder 330 is coupled to an input of adder 350
by an inverting circuit 352, with the adder 350 also

1 receiving a logical "1" carry-in bit. Adder 350 thus
exhibits the bandpass filter response characteristic of
FIGURE 7 at its output by reason of the subtractive
combination of signals supplied by shift register 360 and
5 adder 330.

The FIR filter embodiments of the present
invention have complementary forms, which may be obtained
by selective reversal of the signs of the weighting
coefficients, and/or reversal of the senses of the signal
10 combining elements which produce the output signals. For
example, if the signs of the weighting function coefficients
of circuits 104, 106, 108 and 114, 116, 118 of FIGURE 2
are all reversed, adder 130 will exhibit the bandpass
response characteristic and subtractor 140 will exhibit
15 the lowpass response characteristic. If, in addition, the
senses of adder 130 and subtractor 140 are changed so that
adder 130 becomes a subtractor and subtractor 140 becomes
an adder, the new adder 140 will exhibit a bandpass
response and the new subtractor 130 will exhibit a lowpass
20 response. However, signals passed by the new subtractor
130 will now exhibit a phase reversal with respect to the
input signals of the filter. As another example, if the
embodiment of FIGURE 2 is changed so that subtractor 140
subtracts the weighted center tap signal from the signals
25 produced by adder 128, instead of the opposite as shown
in the FIGURE, subtractor 140 will exhibit a bandpass
response with a phase reversal of the passed signals with
respect to the filter input signal. These alternate
filter forms, in which signals at one or even both of the
30 outputs exhibit a phase reversal, may be desirable when
one of the subsequent signal processing stages requires
phase-inverted input signals. Analysis has shown that
at least twelve such complementary filter forms may be
obtained for each of the illustrated embodiments.

35 It may be appreciated that the bandpass/lowpass
filter networks of the present invention have application in
television receivers in which the luminance and chrominance
information is not separated by comb filtering. Luminance
and chrominance signals can then be separated directly by

1 the bandpass/lowpass filter. In such a receiver, the
values of the weighting function coefficients or the clock
frequency can be adjusted to relocate the crossover
5 frequencies (transition bands) of the output response
characteristics at a higher frequency. In the NTSC
television system, this crossover frequency would be
approximately 3.2 MHz. The lowpass filter output in such
an arrangement would pass signals up to approximately
10 3.2 MHz, and the bandpass filter output would provide
signals of frequencies from 3.2 MHz to the upper limit
of the video frequency range. When the digital video
signal from the A/D converter is supplied to the input
of the filter, luminance information signals would be
15 produced at the output exhibiting the lowpass filter
response, and chrominance information signals would be
produced at the output exhibiting the bandpass filter
response.

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1 CLAIMS

1. A digital filter responsive to an input signal occupying first and second contiguous frequency ranges, for producing first and second output signals at outputs exhibiting complementary frequency characteristics comprising:

5 delaying means, responsive to said input signal, comprising a shift register having a plurality of signal taps, said shift register exhibiting a given time delay between an input and an output
10 said delaying means also producing said input signal delayed by at least an amount of time equal to half of said given time delay;

 signal coupling means, coupled to taps of said shift register for
15 weighting signals coupled therethrough; means, coupled to said signal coupling means excluding said delayed signal weighting means and operating in combination with said shift register, for producing at an output a signal which is a sum of tap-weighted signals;

20 first signal combining means having a first input coupled to receive said sum of tap-weighted signals and a second input coupled to receive said weighted delayed input signal for adding applied signals to produce said first output signal, said first output signal occupying the relatively
25 low frequency one of said contiguous frequency ranges; and

 second signal combining means having a first input coupled to receive said sum of tap-weighted signals and a second input coupled to receive said weighted delayed input signal for subtracting applied signals to
30 produce said second output signal said second output signal occupying the relatively high frequency one of said contiguous frequency range



1 2. A digital filter, responsive to an input signal
occupying first and second contiguous frequency ranges for producing first
and second output signals at outputs exhibiting complementary
frequency response characteristics comprising:

5 a shift register having an input coupled to
receive an input signal and producing at a plurality of
output taps signals delayed relatively less than and
relatively more than signals produced at an intermediate tap
located intermediate said plurality of taps;

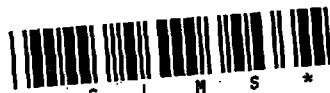
10 means coupled to said plurality of taps and
excluding said intermediate tap, having an output, for
weighting and combining signals developed at said plurality
of taps;

 means coupled to said intermediate tap for weighting
15 signals coupled therethrough;

 first signal combining means coupled to receive
weighted signals from said intermediate tap and from said
weighting and combining means, for adding applied signals,
and having an output exhibiting a first amplitude versus
20 frequency response characteristic occupying the relatively
low frequency one of said contiguous frequency ranges;
and

 second signal combining means coupled to receive
signals from said intermediate tap and from said weighting
25 and combining means, for subtracting applied signals, and
having an output exhibiting a second amplitude versus
frequency response characteristic occupying a relatively
high frequency one of said contiguous frequency ranges.

30 3. A filter according to claim 2, wherein said
plurality of output taps of said shift register is
symmetrically located with respect to said intermediate
output tap; and wherein said weighting and combining means
includes a plurality of weighting function circuits coupled
35 to ones of said plurality of output taps and exhibiting
symmetrical weighting function values about said intermediate
output tap, and an adder tree coupled to said weighting
function circuits and having an output at which a tap-
weighted signal is produced.



- 1 4. A digital filter, responsive to an input
signal occupying first and second contiguous frequency ranges for producing
first and second output signals at outputs exhibiting comple-
mentary response characteristics comprising:
- 5 a shift register including a plurality of serially
coupled stages and having a plurality of adders coupled
between ones of said stages, said shift register having an
output, and exhibiting a given delay;
- 10 means for applying weighted input signals to ones of
said adders;
- means for producing signals at an output which are
said input signals delayed by at least half the delay of
said shift register;
- 15 first signal combining means, coupled to said
output of said shift register and to said signal delaying
means, for adding signals applied thereto and exhibiting, at
an output, a first amplitude versus frequency response
characteristic occupying the relatively low frequency one
of said contiguous frequency ranges; and
- 20 second signal combining means, coupled to said
output of said shift register and to said signal delaying
means, for subtracting signals applied thereto and
exhibiting, at an output, a second amplitude versus
frequency response characteristic occupying the relatively high
25 frequency one of said contiguous frequency ranges.



1 5. A filter according to claim 4, wherein said
weighted signal applying means comprises a plurality of
weighting function circuits having symmetrical weighting
function values with respect to an intermediate point of
5 said shift register, and wherein said plurality of adders
are symmetrically located about said intermediate point of
said shift register.

6. A filter according to claim 5 wherein said
10 signal delaying means includes the series combination of
a weighting function circuit and a second shift register
having half the number of stages as said first-named shift
register.

15 7. A filter according to claim 3 or 5 wherein
said weighting function circuits comprise shift-and-add
circuits.

8. A filter according to claim 1, 2 or 4 wherein
20 said second signal combining means includes means for two's
complementing one of said applied signals, and an adder.

9. A television receiver comprising a digital
filter according to any preceding claim for separating
25 chrominance and vertical detail information.

10. A digital filter substantially as hereinbefore
described with reference to Figure 2, 3 or 4.

30 11. A television receiver substantially as here-
inbefore described with reference to Figure 1 and Figure
2, 3 or 4.

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