cycle time and decreases manufacturing throughput. Vertical interconnections formed exclusively by a laser drilling process can result in reduced control for vertical interconnections. Unprotected contacts can also lead to increases in yield loss for interconnections formed with subsequent surface mount technology (SMT). Furthermore, conductive materials used for forming vertical interconnects within PoP, such as copper (Cu), can incidentally be transferred to semiconductor die during package formation, thereby contaminating the semiconductor die within the package.

## Summary of the Invention

A need exists for vertical interconnects in a Fo-PoP without laser drilling through the package. Accordingly, in one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier with a die attach area, mounting a semiconductor die to the die attach area, mounting a modular interconnect unit over the carrier in a peripheral region around the semiconductor die, depositing an encapsulant over the carrier, semiconductor die, and modular interconnect unit, removing a portion of the encapsulant to expose the semiconductor die and modular interconnect unit, removing the carrier, and forming an interconnect structure over the semiconductor die and modular interconnect unit.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier, mounting a semiconductor die to the carrier, mounting a modular interconnect unit over the carrier in a peripheral region around the semiconductor die, depositing

units having vertical interconnect structures;

FIGs. 7a-7i illustrate various conductive vertical interconnect structures for PWB modular units;

FIGs. 8a-8c illustrate a process of forming a PWB modular unit with a vertical interconnect structures containing bumps;

FIG. 9 illustrates a Fo-PoP with semiconductor die interconnected by PWB modular units having vertical interconnect structures containing bumps; and

FIG. 10 illustrates another Fo-PoP with semiconductor die interconnected by PWB modular units having vertical interconnect structures.

etch-resistant. In most negative resists, the polymers are polyisoprenes. Removing the soluble portions (i.e., the portions not exposed to light) with chemical solvents or developers leaves a hole in the resist layer that corresponds to the opaque pattern on the reticle. A mask whose pattern exists in the opaque regions is called a clear-field mask.

In positive-acting photoresists, photoresist is exposed to light and is changed from relatively nonsoluble condition to much more soluble condition in a process known as photosolubilization. In photosolubilization, the relatively insoluble resist is exposed to the proper light energy and is converted to a more soluble state. The photosolubilized part of the resist can be removed by a solvent in the development process. The basic positive photoresist polymer is the phenol-formaldehyde polymer, also called the phenol-formaldehyde novolak resin. Removing the soluble portions (i.e., the portions exposed to light) with chemical solvents or developers leaves a hole in the resist layer that corresponds to the transparent pattern on the reticle. A mask whose pattern exists in the transparent regions is called a dark-field mask.

After removal of the top portion of the semiconductor wafer not covered by the photoresist, the remainder of the photoresist is removed, leaving behind a patterned layer. Alternatively, some types of materials are patterned by directly depositing the material into the areas or voids formed by a previous deposition/etch process using techniques such as electroless and electrolytic plating.

Depositing a thin film of material over an existing pattern can exaggerate the underlying pattern and create a non-uniformly flat surface. A uniformly flat surface is required to produce smaller and more densely packed active and passive

In FIG. 4e, a conductive layer 156 is formed over conductive layer 152 and filler material 154 using a metal deposition process such as printing, PVD, CVD, sputtering, electrolytic plating, and electroless plating. Conductive layer 156 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material. In one embodiment, conductive layer 156 includes a first Cu layer formed by electroless plating, followed by a second Cu layer formed by electrolytic plating.

In FIG. 4f, a portion of conductive layers 142, 144, 146, 148, 152, and 156 is removed by a wet etching process through a patterned photoresist layer to expose laminate core 140 and leave conductive vertical interconnect structures 158 through laminate core 140. An insulating or passivation layer 160 is formed over laminate core 140 and conductive vertical interconnect structures 158 using vacuum lamination, spin coating, spray coating, screen printing, or other printing process. The insulating layer 160 contains one or more layers of polymer dielectric material with or without insulating filler of $SiO_2$, $Si_3N_4$, SiON, $Ta_2O_5$, $Al_2O_3$, or other material having similar insulating and structural properties. A portion of insulating layer 160 is removed by an etching process or LDA to expose conductive layer 156 and facilitate the formation of subsequent conductive layers.

An optional conductive layer 162 can be formed over the exposed conductive layer 156 using a metal deposition process such as electrolytic plating and electroless plating. Conductive layer 162 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, W, or other suitable electrically conductive material. In one embodiment, conductive layer 162 is a Cu protective layer.

124 and PWB units 164-166 mounted to carrier 170 as a reconstituted wafer 174. Semiconductor die 124 extend above PWB units 164-166 by distance D1 greater than 1 μm. The offset between PWB units 164-166 and semiconductor die 124 reduces contamination during a subsequent backgrinding step.

In FIG. 5c, an encapsulant or molding compound 176 is deposited over semiconductor die 124, PWB units 164-166, and carrier 170 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 176 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 176 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 5d, carrier 170 and interface layer 172 are removed by chemical etching, mechanical peeling, chemical mechanical polishing (CMP,) mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose insulating layer 134, PWB units 164-166, and encapsulant 176.

In FIG. 5e, a build-up interconnect structure 180 is formed over semiconductor die 124, PWB units 164-166, and encapsulant 176. An insulating or passivation layer 182 is formed over semiconductor die 124, PWB units 164-166, and encapsulant 176 using PVD, CVD, lamination, printing, spin coating, or spray coating. The insulating layer 182 contains one or more layers of low temperature (less than 250°C) curing polymer dielectric with or without insulating fillers, like $SiO_2$, $Si_3N_4$, SiON, $Ta_2O_5$, $Al_2O_3$, rubber particles, or other material having similar insulating and structural properties. A portion of insulating layer 182 can be removed by an etching

electrical contact to conductive layer 188. An under bump metallization (UBM) can be formed under bumps 192. Bumps 192 can also be compression bonded to conductive layer 188. Bumps 192 represent one type of interconnect structure that can be formed over conductive layer 188. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect.

In FIG. 5f, a portion of encapsulant 176 and semiconductor die 124 is removed by a grinding operation with grinder 194 to planarize the surface and reduce a thickness of the encapsulant. Encapsulant 176 remains over PWB units 164-166 with a thickness D2 of at least 1 μm. A chemical etch, CMP, or plasma dry etch can also be used to remove back grinding damage and residue stress on semiconductor die 124 and encapsulant 176 to enhance the package strength.

In FIG. 5g, a backside balance layer 196 is applied over encapsulant 176, PWB units 164-166, and semiconductor die 124. Backside balance layer 196 balances the coefficient of thermal expansion (CTE), e.g. 30-150ppm/K, of conductive layers 184 and 188 and reduces warpage in the package. In one embodiment, backside balance layer 196 has a thickness of 10-100 μm.

In FIG. 5h, a portion of backside balance layer 196 and encapsulant 176 removed to expose vertical interconnect structures 158. Reconstituted wafer 174 is singulated through PWB modular unit 164 with saw blade or laser cutting tool 202 into separate Fo-PoP 204.

vertical interconnection with respect to vertical interconnections formed exclusively by a laser drilling process.

In another embodiment, FIG. 6a shows a cross-sectional view of a portion of a carrier or temporary substrate 220 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 224 is formed over carrier 220 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer.

In FIG. 6b, semiconductor die 124 from FIG. 3c are mounted to interface layer 224 and carrier 220 using a pick and place operation with active surface 130 oriented toward the carrier. Semiconductor die 124 are pressed into interface layer 224 such that insulating layer 134 is disposed into the interface layer. When semiconductor die 124 is mounted to interface layer 224, a surface 225 of insulating layer 134 is separated by a distance D1 from carrier 220.

In FIG. 6c, PWB modular units 164-166 from FIG. 4h are mounted to interface layer 224 and carrier 220 using a pick and place operation. PWB units 164-166 are pressed into interface layer 224 such that contacting surface 226 is disposed into the interface layer. When PWB units 164-166 are mounted to interface layer 224, surface 226 is separated by a distance D2 from carrier 220. D2 is greater than D1 such that surface 226 of PWB units 164-166 is vertically offset with respect to surface 225 of insulating layer 134.

FIG. 6d shows semiconductor die 124 and PWB modular units 164-166 mounted to carrier 220 as a reconstituted wafer 227. A surface 228 of PWB units 164-166, opposite surface 226, is vertically offset with respect to back surface 128 of

semiconductor die 124 by a distance of D3, e.g. at least 1 μm. By separating surface 228 of PWB units 166 and back surface 128 of semiconductor die 124 a subsequent backgrinding step is facilitated by preventing material from vertical interconnect structures 158, such as Cu, from contaminating a material of semiconductor die 124, such as Si.

FIG. 6e shows a plan view of a portion of reconstituted wafer 227 having PWB modular units 164-166 mounted over interface layer 224. PWB units 164-166 contain multiple rows of vertical interconnect structures 158 that provide through vertical interconnection between opposing sides of the PWB units. PWB units 164-166 are disposed around semiconductor die 124 in an interlocking pattern. PWB units 164-166 are disposed around semiconductor die 124 in such a way that different sides of the semiconductor die are aligned with, and correspond to, a number of different sides of the PWB units in a repeating pattern across reconstituted wafer 227. A plurality of saw streets 230 are aligned with respect to the semiconductor die and extend across PWB units 164-166 such that when reconstituted wafer 227 is singulated along the saw streets, each semiconductor die 124 has a plurality of vertical interconnect structures 158 from singulated PWB units 164-166 that are disposed around or in a peripheral region around the semiconductor die. While PWB units 164-166 are illustrated with interlocking square and rectangular footprints, the PWB units disposed around semiconductor die 124 can include PWB units having footprints with a cross-shape (+), an angled or "L-shape," a circular or oval shape, a hexagonal shape, an octagonal shape, a star shape, or any other geometric shape.

FIG. 6f shows a plan view of a portion of a reconstituted wafer 240 having cross-shaped (+) PWB modular

vertical interconnect structures 264 from singulated PWB units 262 and 263 that are disposed around or in a peripheral region around the semiconductor die. Vertical interconnect structures 264 are disposed in one or more rows offset from a perimeter of the semiconductor die after singulation through saw streets 265.

FIG. 6i shows a plan view of a portion of a reconstituted wafer 266 having a continuous PWB unit 267 mounted over interface layer 224. PWB unit 267 is formed in a process similar to PWB units 164-166 as shown in FIGs. 4a-4h. Semiconductor die 124 are disposed within openings of PWB unit 267 with 50 μm clearance. PWB unit 267 contain multiple rows of vertical interconnect structures 268 that are similar to vertical interconnect structures 158 , and provide through vertical interconnection between opposing sides of the PWB units.

A plurality of saw streets 269 are aligned with respect to semiconductor die 124

and extend across PWB unit 267 such that when reconstituted wafer 266 is singulated along the saw streets, each semiconductor die 124 has a plurality of vertical interconnect structures 268 from singulated PWB unit 267 that are disposed around or in a peripheral region around the semiconductor die. Vertical interconnect structures 268 can be disposed in the peripheral region around semiconductor 124 as one or more rows offset from a perimeter of the semiconductor die after singulation through saw streets 269.

Continuing from FIG. 6d, FIG. 6j shows that after semiconductor die 124 and PWB modular units 164-166 are mounted to interface layer 224, reconstituted wafer 227 is partially singulated through saw street 230 using a saw blade or laser cutting tool 270 to form channels or openings 272. Channel 272 extends through PWB units 164-166, and additionally may extend through interface layer 224 and partially but not completely through carrier 220. Channel 272 forms a separation among vertical interconnect structures 158 and the semiconductor die 124 to which the conductive vias will be subsequently joined in a Fo-PoP.

In FIG. 6k, an encapsulant or molding compound 282 is deposited over semiconductor die 124, PWB units 164-166, and carrier 220 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 282 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 282 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

structure 324 is formed over the PWB units.

PWB modular units 164-166 provide a cost effective alternative to using standard laser drilling processes for vertical interconnection in Fo-PoP for a number of reasons. First, PWB units 164-166 can be made with low cost manufacturing technology such as substrate manufacturing technology. Second, standard laser drilling includes high equipment cost and requires drilling through an entire package thickness, which increases cycle time and decrease manufacturing throughput. Furthermore, the use of PWB units 164-166 for vertical interconnection provides an advantage of improved control for vertical interconnection with respect to vertical interconnections formed exclusively by a laser drilling process.

FIG. 7a shows an embodiment of vertical interconnect structure 340 with laminate core 342, conductive layers 344 and 346, and filler material 348. Filler material 348 can be conductive material or insulating material. Conductive layer 344 overlaps laminate core 342 by 0-200 μm. A Cu protective layer 350 is formed over conductive layer 346. An insulating layer 352 is formed over one surface of laminate core 342. A portion of insulating layer 352 is removed to expose Cu protective layer 350.

FIG. 7b shows an embodiment of vertical interconnect structure 360 with laminate core 362, conductive layers 364 and 366, and filler material 368. Filler material 368 can be conductive material or insulating material. Conductive layer 364 overlaps laminate core 362 by 0-200 μm. A Cu protective layer 370 is formed over conductive layer 366.

FIG. 7c shows an embodiment of vertical interconnect structure 380 with laminate

core 382, conductive layers 384 and 386, and filler material 388. Filler material 388 can be conductive material or insulating material. Conductive layer 384 overlaps laminate core 382 by 0-200 μm. A Cu protective layer 390 is formed over conductive layer 346. An insulating layer 392 is formed over one surface of laminate core 382. An insulating layer 394 is formed over an opposite surface of laminate core 382. A portion of insulating layer 394 is removed to expose Cu protective layer 386.

FIG. 7d shows an embodiment of vertical interconnect structure 400 with laminate core 402, conductive layers 404 and 406, and filler material 408. Filler material 408 can be conductive material or insulating material. Conductive layer 404 overlaps laminate core 402 by 0-200 μm.

FIG. 7e shows an embodiment of vertical interconnect structure 410 with laminate core 412, conductive layer 414, and filler material 416. Filler material 416 can be conductive material or insulating material. Conductive layer 414 overlaps laminate core 412 by 0-200 μm. An insulating layer 418 is formed over one surface of laminate core 412. A portion of insulating layer 418 is removed to expose conductive layer 414. A conductive layer 420 is formed over the expose conductive layer 414. A Cu protective layer 422 is formed over conductive layer 420. An insulating layer 424 is formed over an opposite surface of laminate core 412. A conductive layer 426 is formed over the expose conductive layer 414.

FIG. 7f shows an embodiment of vertical interconnect structure 430 with laminate core 432, conductive layer 434, and filler material 436. Filler

material 436 can be conductive material or insulating material. Conductive layer 434 overlaps laminate core 432 by 0-200 μm. An insulating layer 438 is formed over one surface of laminate core 432. A portion of insulating layer 438 is removed to expose conductive layer 434. A conductive layer 440 is formed over the expose conductive layer 434. A Cu protective layer 442 is formed over conductive layer 420. An insulating layer 444 is formed over an opposite surface of laminate core 432. A conductive layer 446 is formed over the expose conductive layer 434. A Cu protective layer 446 is formed over conductive layer 446.

FIG. 7g shows an embodiment of vertical interconnect structure 450 with laminate core 452, conductive layers 454 and 456, and filler material 458. Filler material 458 can be conductive material or insulating material. Conductive layer 454 overlaps laminate core 452 by 0-200 μm. A Cu protective layer 460 is formed over conductive layer 456. An insulating layer 462 is formed over one surface of laminate core 452. A portion of insulating layer 462 is removed to expose Cu protective layer 460. An insulating layer 464 is formed over an opposite surface of laminate core 452. A portion of insulating layer 464 is removed to expose Cu protective layer 460.

FIG. 7h shows an embodiment of vertical interconnect structure 470 with laminate core 472, conductive layers 474 and 476, and filler material 478. Filler material 478 can be conductive material or insulating material. Conductive layer 474 overlaps laminate core 472 by 0-200 μm. A Cu protective layer 480 is formed over conductive layer 476. An insulating layer 482 is formed over one surface of laminate core 472. An insulating layer 484 is

formed over an opposite surface of laminate core 472. A portion of insulating layer 484 is removed to expose Cu protective layer 480.

FIG. 7i shows an embodiment of vertical interconnect structure 490 with laminate core 492, conductive layers 494 and 496, and filler material 498. Filler material 498 can be conductive material or insulating material. Conductive layer 494 overlaps laminate core 492 by 0-200 μm. A Cu protective layer 500 is formed over conductive layer 496. An insulating layer 502 is formed over an opposite surface of laminate core 492. A portion of insulating layer 502 is removed to expose Cu protective layer 480. A Cu protective layer 504 is formed over the exposed conductive layer 496.

In FIG. 8a, a plurality of bumps 510 is formed over Cu foil 512, or other foil or carrier with thin patterned Cu or other wetting material layer. The foil or supporting layer can be evenly bonded to temporary carrier with thermal releasing tape which can stand reflow temperature. In FIG. 8b, an encapsulant 514 is formed over bumps 510 and Cu foil 512. In FIG. 8c, Cu foil 512 is removed and bumps 510 embedded in encapsulant 514 is singulated with saw blade or laser cutting tool 516 into PWB vertical interconnect units 518.

FIG. 9 shows a Fo-PoP 520 including semiconductor die 522, which is similar to semiconductor die 124 from FIG. 3c. Semiconductor die 522 has a back surface 524 and active surface 526 opposite back surface 524 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. An electrically conductive

layer 528 is formed over active surface 526 and operates as contact pads that are electrically connected to the circuits on active surface 526. An insulating or passivation layer 530 is conformally applied over active surface 526.

FIG. 9 also shows PWB modular units 518 from FIGs. 8a-8c laterally offset from, and disposed around or in a peripheral region around semiconductor die 522. Back surface 524 of semiconductor die 522 is offset from PWB modular units 518 by at least 1 μm, similar to FIG. 5b. Encapsulant 532 is deposited around PWB units 518. A build-up interconnect structure 534, similar to build-up interconnect structure 180 in FIG. 5e, is formed over encapsulant 532, PWB units 518, and semiconductor die 522. An insulating or passivation layer 536 is formed over encapsulant 532, PWB units 518, and semiconductor die 522. A portion of encapsulant 514 and insulating layer 536 is removed to expose bumps 510. Bumps 510 are offset from back surface 524 of semiconductor die 522 by at least 1 μm.

FIG. 10 shows an embodiment of Fo-PoP 540, similar to FIG. 5h, with encapsulant 542 disposed around PWB units 164-166.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.