

AMPLIFIER AND TRANSCEIVER INCLUDING THE AMPLIFIER

TECHNICAL FIELD

[0001] Various embodiments relate generally to an amplifier and a transceiver
5 including the amplifier.

BACKGROUND

[0002] In March 2009, the Federal Communications Commission (FCC) introduced the Medical Device Radiocommunications Service (MedRadio) band in the range of 401-
10 406 MHz which is a wireless communication regulation dedicated for biomedical telemetry. Formerly known as the 402-405 MHz Medical Implant Communication Service (MICS) band allocated in 1999, MedRadio is the superset of MICS in which additional adjacent bands at 401-402 MHz and 405-406 MHz are newly designated with twenty 100 kHz bandwidth channels to provide a total of five megahertz of contiguous
15 spectrum and accommodate both implantable and wearable sensor devices for medical use.

[0003] Due to the need for reliable, continuous, and cost-effective health monitoring in hospitals and homes in recent years, both implantable and wearable sensors in Wireless Body Area Networks (WBAN) must meet ultra-low-power consumption for prolonged
20 battery life. Since the wireless part of the sensor device usually consumes the most power, it is important to reduce both the current and the supply voltage of the transceiver to minimize the power consumption without compromising the performance.

[0004] Among several wireless bands for wearable sensor applications such as the industrial, scientific, and medical (ISM) frequencies at 433 MHz, 868-928 MHz, and 2.4 GHz respectively, some of these bands are not recognized globally while higher frequencies have the disadvantage of increased power consumption and free-space path loss. As higher frequencies are utilized for many other non-medical applications, it is prone to interference issues which are critical in biomedical applications where highly reliable communication is of key importance.

[0005] A low noise amplifier (LNA) usually dominates the total noise performance and sensitivity of a receiver used in biomedical applications. However, conventional LNAs typically have a limitation in performance improvement without increasing power, complexity or area.

[0006] Figure 1a shows a conventional source degeneration cascode LNA (SDCLNA) 102. The SDCLNA 102 has a simple topology and can achieve a good noise performance with sufficient gain even at low bias current due to the passive amplification from the input matching circuitry. However, in order to constrain the current consumption of the SDCLNA 102 to less than 150 μ A, the transistor M_{n1} is biased close to threshold and its size is limited which leads to a small transconductance g_m and a small gate-to-source capacitance C_{gs} . A small g_m and C_{gs} will require large values of depletion capacitance C_d , gate inductance L_g , and source inductance L_s in order to match the impedance to 50 Ω at 400 MHz. Thus, at a low frequency of operation (e.g. <1 GHz) and low power (<~mW), large sizes of passive matching components (e.g. source inductor) are required for 50 Ω matching. A small g_m also leads to a limitation in the gain and noise performance. Thus, there is a limitation of performance improvement (noise and

linearity) without power increase. It is difficult to further improve the noise figure (NF) of the SDCLNA 102 without increasing the power consumption.

[0007] Figure 1b shows a conventional current-reuse LNA 104. The current-reuse LNA 104 has a current reuse topology and can provide an improved noise performance.

5 However, the current-reuse LNA 104 requires additional DC feedback circuitry and additional passive components for performance improvement.

SUMMARY

[0008] According to one embodiment, an amplifier is provided. The amplifier
10 includes an input terminal; a first transistor of a first conductivity and a second transistor of a second conductivity, each transistor comprising a source terminal, a gate terminal and a drain terminal respectively, the source terminal of the first transistor being coupled to the source terminal of the second transistor, and the gate terminal of the first transistor and the gate terminal of the second transistor being coupled to the input terminal; and an
15 output terminal coupled to the drain terminal of the first transistor and the drain terminal of the second transistor is provided.

[0009] In one embodiment, the amplifier may further include a first depletion capacitor coupled between the gate terminal and the source terminal of the first transistor.

[0010] In one embodiment, the first depletion capacitor may include a positive
20 terminal and a negative terminal. The positive terminal of the first depletion capacitor may be coupled to the gate terminal of the first transistor and the negative terminal of the first depletion capacitor may be coupled to the source terminal of the first transistor.

[0011] In one embodiment, the amplifier may further include a second depletion capacitor coupled between the gate terminal and the source terminal of the second transistor.

5 [0012] In one embodiment, the second depletion capacitor may include a positive terminal and a negative terminal. The positive terminal of the second depletion capacitor may be coupled to the gate terminal of the second transistor and the negative terminal of the second depletion capacitor may be coupled to the source terminal of the second transistor.

10 [0013] In one embodiment, the amplifier may further include a first resistor coupled between the drain terminal of the first transistor and a first voltage reference point.

[0014] In one embodiment, the first resistor may include a first terminal and a second terminal. The first terminal of the first resistor may be coupled to the drain terminal of the first transistor and the second terminal of the first resistor may be coupled to the first voltage reference point.

15 [0015] In one embodiment, the amplifier may further include a second resistor coupled between the drain terminal of the second transistor and a second voltage reference point.

20 [0016] In one embodiment, the second resistor may include a first terminal and a second terminal. The first terminal of the second resistor may be coupled to the drain terminal of the second transistor and the second terminal of the second resistor may be coupled to the second voltage reference point.

[0017] In one embodiment, the amplifier may further include a first output capacitor coupled between the drain terminal of the first transistor and the output terminal.

[0018] In one embodiment, the first output capacitor may include a positive terminal and a negative terminal. The positive terminal of the first output capacitor may be coupled to the drain terminal of the first transistor and the first terminal of the first resistor and the negative terminal of the first output capacitor may be coupled to the output terminal.

[0019] In one embodiment, the amplifier may further include a second output capacitor coupled between the drain terminal of the second transistor and the output terminal.

[0020] In one embodiment, the second output capacitor may include a positive terminal and a negative terminal. The positive terminal of the second output capacitor may be coupled to the drain terminal of the second transistor and the first terminal of the second resistor and the negative terminal of the second output capacitor may be coupled to the output terminal.

[0021] In one embodiment, the amplifier may further include a gate inductor having a first terminal and a second terminal, a first gate capacitor having a positive terminal and a negative terminal, and a second gate capacitor having a positive terminal and a negative terminal. The first terminal of the gate inductor may be coupled to the input terminal, and the second terminal of the gate inductor may be coupled to the positive terminal of the first gate capacitor and the positive terminal of the second gate capacitor. The negative terminal of the first gate capacitor may be coupled to the gate terminal of the first transistor and the positive terminal of the first depletion capacitor. The negative terminal of the second gate capacitor may be coupled to the gate terminal of the second transistor and the positive terminal of the second depletion capacitor.

[0022] In one embodiment, the amplifier may further include a source inductor having a first terminal and a second terminal, and a source capacitor having a positive terminal and a negative terminal. The first terminal of the source inductor may be coupled to the source terminal of the first transistor, the negative terminal of the first depletion capacitor, the source terminal of the second transistor and the negative terminal of the second depletion capacitor. The second terminal of the source inductor may be coupled to the positive terminal of the source capacitor. The negative terminal of the source capacitor may be coupled to the second voltage reference point.

[0023] In one embodiment, the amplifier may further include a first bias voltage input terminal adapted to provide a first bias voltage to the gate terminal of the first transistor.

[0024] In one embodiment, the first bias voltage input terminal may be provided between the negative terminal of the first gate capacitor and the positive terminal of the first depletion capacitor.

[0025] In one embodiment, the amplifier may further include a second bias voltage input terminal adapted to provide a second bias voltage to the gate terminal of the second transistor.

[0026] In one embodiment, the second bias voltage input terminal may be provided between the negative terminal of the second gate capacitor and the positive terminal of the second depletion capacitor.

[0027] In one embodiment, the first transistor may include an n-channel metal-oxide-semiconductor field-effect transistor.

[0028] In one embodiment, the second transistor may include a p-channel metal-oxide-semiconductor field-effect transistor.

[0029] In one embodiment, the second voltage reference point may be ground.

[0030] According to another embodiment, a transceiver including an amplifier as described above is provided.

[0031] According to yet another embodiment, an amplifier is provided. The amplifier
5 includes an input terminal and an output terminal, wherein the input terminal and the output terminal are single-ended with equal phases for a signal; and a core configured to operate as a differential mode.

[0032] In one embodiment, the core may include a first transistor of a first conductivity and a second transistor of a second conductivity, each transistor comprising
10 a source terminal, a gate terminal and a drain terminal respectively, the source terminal of the first transistor being coupled to the source terminal of the second transistor, and the gate terminal of the first transistor and the gate terminal of the second transistor being coupled to the input terminal.

[0033] In one embodiment, the first transistor may include an n-channel metal-oxide-
15 semiconductor field-effect transistor.

[0034] In one embodiment, the second transistor may include a p-channel metal-oxide-semiconductor field-effect transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

20 [0035] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the

following description, various embodiments of the invention are described with reference to the following drawings, in which:

[0036] Figure 1a shows a schematic diagram of a conventional source degeneration cascode low noise amplifier (SDCLNA).

5 [0037] Figure 1b shows a schematic diagram of a conventional current-reuse low noise amplifier.

[0038] Figure 2 shows a schematic diagram of an amplifier according to one embodiment.

[0039] Figure 3 shows a schematic diagram of an amplifier according to one
10 embodiment.

[0040] Figure 4 shows schematic diagrams of a first circuit arrangement and a second circuit arrangement according to one embodiment.

[0041] Figure 5 shows a graph of measured drain current i_{DS} , transconductance g_m , and first derivative of transconductance g_m' of a 120- μm /0.18- μm n-channel metal-oxide-semiconductor field-effect transistor and a 240- μm /0.18- μm p-channel metal-oxide-semiconductor field-effect transistor.
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[0042] Figure 6 shows a schematic diagram of an alternating current equivalent circuit of an amplifier according to one embodiment.

[0043] Figure 7a shows a schematic diagram of a high impedance passive
20 amplification circuit according to one embodiment.

[0044] Figure 7b shows a schematic diagram of an equivalent circuit of a high impedance passive amplification circuit according to one embodiment.

[0045] Figure 7c shows a schematic diagram of an equivalent circuit of a high impedance passive amplification circuit according to one embodiment.

[0046] Figure 8 shows a graph of s-parameter plotted against frequency according to one embodiment.

5 [0047] Figure 9 shows a graph of noise figure (NF) plotted against frequency according to one embodiment.

[0048] Figure 10a shows a simulated third order input intercept point (IIP3) of a conventional source degeneration cascode low noise amplifier (SDCLNA).

10 [0049] Figure 10b shows a simulated third order input intercept point (IIP3) of an amplifier according to one embodiment.

[0050] Figure 11 shows a table listing simulation results of a conventional source degeneration cascode low noise amplifier (SDCLNA) and simulation results of an amplifier according to one embodiment.

15 [0051] Figure 12 shows a graph illustrating experimental results of an amplifier according to one embodiment.

[0052] Figure 13 shows a graph illustrating third order input intercept point (IIP3) linearity measurements of an amplifier according to one embodiment.

20 [0053] Figure 14 shows a table listing simulation results of four conventional amplifiers, preliminary measurements of an amplifier with 50 Ω impedance matching according to one embodiment, and simulation results of an amplifier with high impedance matching (non-50 Ω matching) according to one embodiment.

[0054] Figure 15 shows a graph illustrating simulation results of an amplifier with high impedance passive network (non-50 Ω matching) according to one embodiment.

[0055] Figure 16 shows a block diagram of a receiver RF front-end according to one embodiment.

[0056] Figure 17 shows a schematic diagram of a folded active mixer according to one embodiment.

5 [0057] Figure 18 shows a chip microphotograph of a receiver RF front-end according to one embodiment.

[0058] Figure 19 shows a graph of measured conversion gain and input return loss (S11) of a receiver front-end plotted against RF input frequency at an intermediate frequency (IF) of 500 kHz according to one embodiment.

10 [0059] Figure 20 shows a graph of noise figure (NF) measurement plotted against output frequency of a receiver front-end according to one embodiment.

[0060] Figure 21 shows a graph of third order input intercept point (IIP3) linearity measurement where two-tones at 402 and 402.1 MHz are applied to an input of a receiver front-end according to one embodiment.

15 [0061] Figure 22 shows a table showing measured results of four conventional receivers and measured results of a receiver RF front-end according to one embodiment.

DETAILED DESCRIPTION

[0062] Embodiments of an amplifier and a transceiver including the amplifier will be
20 described in detail below with reference to the accompanying figures. It will be appreciated that the embodiments described below can be modified in various aspects without changing the essence of the invention.

[0063] Figure 2 shows a schematic diagram of one embodiment of an amplifier 200. The amplifier 200 includes an input terminal 202 and an output terminal 204. The input terminal 202 and the output terminal 204 are single-ended with equal phases for a signal. The amplifier 200 also includes a core 206.

5 [0064] The core 206 includes a first transistor 208 of a first conductivity and a second transistor 210 of a second conductivity. In one embodiment, the first transistor 208 may be an n-channel metal-oxide-semiconductor field-effect transistor (NMOS), and the second transistor 210 may be a p-channel metal-oxide-semiconductor field-effect transistor (PMOS). The first transistor 208 has a source terminal 212, a gate terminal 214
10 and a drain terminal 216. The second transistor 210 has a source terminal 218, a gate terminal 220 and a drain terminal 222.

[0065] In one embodiment, the source terminal 212 of the first transistor 208 is coupled to the source terminal 218 of the second transistor 210. The gate terminal 214 of the first transistor 208 and the gate terminal 220 of the second transistor 210 are coupled
15 to the input terminal 202. The drain terminal 216 of the first transistor 208 and the drain terminal 222 of the second transistor 210 may be coupled to various electrical components which are not shown for ease of illustration. Details of the coupling of the drain terminal 216 of the first transistor 208 and the drain terminal 222 of the second transistor 210 are shown in Figure 3 and are described in detail with respect to Figure 3.

20 [0066] The core 206 is configured to operate as a differential mode. The core 206 may operate as a differential mode due to the complementary characteristic of the first transistor 208 and the second transistor 210. Since the first transistor 208 is NMOS and the second transistor 210 is PMOS, the core 206 can operate between a high (e.g.

positive) voltage and a low (e.g. negative) voltage. When a high (e.g. positive) voltage is applied at the input terminal 202, the first transistor 208 is on (i.e. operating) and the second transistor 210 is off. When a low (e.g. negative voltage) is applied at the input terminal 202, the first transistor 208 is off and the second transistor 210 is on (i.e. operating).

[0067] Figure 3 shows a schematic diagram of another embodiment of an amplifier 300. The amplifier 300 includes an input terminal 302, a first transistor 304 of a first conductivity and a second transistor 306 of a second conductivity. In one embodiment, the first transistor 304 may be an n-channel metal-oxide-semiconductor field-effect transistor (NMOS), and the second transistor 306 may be a p-channel metal-oxide-semiconductor field-effect transistor (PMOS).

[0068] The first transistor 304 includes a source terminal 308, a gate terminal 310 and a drain terminal 312. The second transistor 306 includes a source terminal 314, a gate terminal 316 and a drain terminal 318. In one embodiment, the source terminal 308 of the first transistor 304 is coupled to the source terminal 314 of the second transistor 306. The gate terminal 310 of the first transistor 304 and the gate terminal 316 of the second transistor 306 are coupled to the input terminal 302.

[0069] The amplifier 300 includes an output terminal 320 coupled to the drain terminal 312 of the first transistor 304 and the drain terminal 318 of the second transistor 306. The amplifier 300 also includes a first depletion capacitor 322 coupled between the gate terminal 310 and the source terminal 308 of the first transistor 304. The first depletion capacitor 322 has a positive terminal 324 and a negative terminal 326. The positive terminal 324 of the first depletion capacitor 322 is coupled to the gate terminal

310 of the first transistor 304 and the negative terminal 326 of the first depletion capacitor 322 is coupled to the source terminal 308 of the first transistor 304.

[0070] The amplifier 300 includes a second depletion capacitor 328 coupled between the gate terminal 316 and the source terminal 314 of the second transistor 306. The second depletion capacitor 328 has a positive terminal 330 and a negative terminal 332. The positive terminal 330 of the second depletion capacitor 328 is coupled to the gate terminal 316 of the second transistor 306 and the negative terminal 332 of the second depletion capacitor 328 is coupled to the source terminal 314 of the second transistor 306.

[0071] The amplifier 300 includes a first resistor 334 coupled between the drain terminal 312 of the first transistor 304 and a first voltage reference point 336. The first resistor 334 includes a first terminal 338 and a second terminal 340. The first terminal 338 of the first resistor 334 is coupled to the drain terminal 312 of the first transistor 304 and the second terminal 340 of the first resistor 334 is coupled to the first voltage reference point 336.

[0072] The amplifier 300 includes a second resistor 342 coupled between the drain terminal 318 of the second transistor 306 and a second voltage reference point 344. The second resistor has a first terminal 346 and a second terminal 348. The first terminal 346 of the second resistor 342 is coupled to the drain terminal 318 of the second transistor 306 and the second terminal 348 of the second resistor 342 is coupled to the second voltage reference point 344. In one embodiment, the second voltage reference point 344 may be ground.

[0073] The amplifier 300 includes a first output capacitor 350 coupled between the drain terminal 312 of the first transistor 308 and the output terminal 320. The first output

capacitor 350 has a positive terminal 352 and a negative terminal 354. The positive terminal 352 of the first output capacitor 350 is coupled to the drain terminal 312 of the first transistor 304 and the first terminal 338 of the first resistor 334. The negative terminal 354 of the first output capacitor 350 is coupled to the output terminal 320.

5 [0074] The amplifier 300 includes a second output capacitor 356 coupled between the drain terminal 318 of the second transistor 306 and the output terminal 320. The second output capacitor 356 has a positive terminal 358 and a negative terminal 360. The positive terminal 358 of the second output capacitor 356 is coupled to the drain terminal 318 of the second transistor 306 and the first terminal 346 of the second resistor 342. The
10 negative terminal 360 of the second output capacitor 356 is coupled to the output terminal 320.

[0075] In other words, the negative terminal 354 of the first output capacitor 350 is coupled to the negative terminal 360 of the second output capacitor 356. The output terminal 320 is coupled between the negative terminal 354 of the first output capacitor
15 350 and the negative terminal 360 of the second output capacitor 356.

[0076] The amplifier 300 includes a gate inductor 362 having a first terminal 364 and a second terminal 366, a first gate capacitor 368 having a positive terminal 370 and a negative terminal 372, and a second gate capacitor 374 having a positive terminal 376 and a negative terminal 378. The first terminal 364 of the gate inductor 362 is coupled to
20 the input terminal 302, and the second terminal 366 of the gate inductor 362 is coupled to the positive terminal 370 of the first gate capacitor 368 and the positive terminal 376 of the second gate capacitor 374. The negative terminal 372 of the first gate capacitor 368 is coupled to the gate terminal 310 of the first transistor 304 and the positive terminal 324

of the first depletion capacitor 322. The negative terminal 378 of the second gate capacitor 374 is coupled to the gate terminal 316 of the second transistor 306 and the positive terminal 330 of the second depletion capacitor 328.

[0077] The amplifier 300 also includes a source inductor 380 having a first terminal 382 and a second terminal 384, and a source capacitor 386 having a positive terminal 388 and a negative terminal 390. The first terminal 382 of the source inductor 380 is coupled to the source terminal 308 of the first transistor 304, the negative terminal 326 of the first depletion capacitor 322, the source terminal 314 of the second transistor 306 and the negative terminal 332 of the second depletion capacitor 328. The second terminal 384 of the source inductor 380 is coupled to the positive terminal 388 of the source capacitor 386. The negative terminal 390 of the source capacitor 386 is coupled to the second voltage reference point 344.

[0078] The amplifier 300 includes a first bias voltage input terminal 392 adapted to provide a first bias voltage to the gate terminal 310 of the first transistor 304. The first bias voltage input terminal 392 is provided between the negative terminal 372 of the first gate capacitor 368 and the positive terminal 324 of the first depletion capacitor 322. The amplifier 300 also includes a second bias voltage input terminal 394 adapted to provide a second bias voltage to the gate terminal 316 of the second transistor 306. The second bias voltage input terminal 394 is provided between the negative terminal 378 of the second gate capacitor 374 and the positive terminal 330 of the second depletion capacitor 328.

[0079] In one embodiment, the amplifier 300 may include an n-channel metal-oxide-semiconductor field-effect transistor (NMOS) and a p-channel metal-oxide-semiconductor field-effect transistor (PMOS). The NMOS and the PMOS may be

coupled such that the respective source terminals are coupled together. Thus, the amplifier 300 may have a common source topology. The respective gate terminals of the NMOS and the PMOS may be coupled together. An input terminal may be coupled between the gate terminals of the NMOS and the PMOS. The respective drain terminals of the NMOS and the PMOS may be coupled together. An output terminal may be coupled between the drain terminals of the NMOS and the PMOS. In other words, the amplifier 300 may provide a single input and a single output. The arrangement of the NMOS and the PMOS may provide a complementary metal-oxide-semiconductor field-effect transistor (CMOS). With this arrangement, the NMOS and the PMOS may be on (i.e. operating) depending on the input. When the input is high, the NMOS is on and the PMOS is off. When the input is low, the NMOS is off and the PMOS is on.

[0080] In one embodiment, the amplifier 300 may be formed by combining a first circuit arrangement 400 and a second circuit arrangement 450 as shown in Figure 4. The first circuit arrangement 400 includes an input terminal 401 and an output terminal 402. The first circuit arrangement 400 includes a transistor 403 of a first conductivity having a source terminal 404, a gate terminal 405 and a drain terminal 406, a depletion capacitor 407 having a positive terminal 408 and a negative terminal 409, a resistor 410 having a first terminal 411 and a second terminal 412, an output capacitor 413 having a positive terminal 414 and a negative terminal 415, a gate inductor 416 having a first terminal 417 and a second terminal 418, a gate capacitor 419 having a positive terminal 420 and a negative terminal 421, and a source inductor 422 having a first terminal 423 and a second terminal 424. In one embodiment, the transistor 403 may be an n-channel metal-oxide-

semiconductor field-effect transistor (NMOS). The first circuit arrangement 400 also includes a bias voltage input terminal 425.

[0081] The source terminal 404 of the transistor 403 is coupled to the negative terminal 408 of the depletion capacitor 407 and the first terminal 423 of the source inductor 422. The gate terminal 405 of the transistor 403 is coupled to the positive terminal 409 of the depletion capacitor 407 and the negative terminal 421 of the gate capacitor 419. The drain terminal 406 of the transistor 403 is coupled to the first terminal 411 of the resistor 410 and the positive terminal 414 of the output capacitor 413.

[0082] The positive terminal 420 of the gate capacitor 419 is coupled to the second terminal 418 of the gate inductor 416. The first terminal 417 of the gate inductor 416 is coupled to the input terminal 401. The negative terminal 415 of the output capacitor 413 is coupled to the output terminal 402. The second terminal 412 of the resistor 410 is coupled to a first voltage reference point 426. The second terminal 424 of the source inductor 422 is coupled to a second voltage reference point 427. In one embodiment, the second voltage reference point 427 may be ground. The bias voltage input terminal 425 is coupled between the negative terminal 421 of the gate capacitor 419 and the positive terminal 409 of the depletion capacitor 407. The bias voltage input terminal 425 may be adapted to provide a bias voltage to the gate terminal 405 of the transistor 403.

[0083] The second circuit arrangement 450 includes an input terminal 451 and an output terminal 452. The second circuit arrangement 450 includes a transistor 453 of a second conductivity having a source terminal 454, a gate terminal 455 and a drain terminal 456, a depletion capacitor 457 having a positive terminal 458 and a negative terminal 459, a resistor 460 having a first terminal 461 and a second terminal 462, an

output capacitor 463 having a positive terminal 464 and a negative terminal 462, a gate inductor 466 having a first terminal 467 and a second terminal 468, a gate capacitor 469 having a positive terminal 470 and a negative terminal 471, and a source inductor 472 having a first terminal 473 and a second terminal 474. In one embodiment, the transistor 5 453 may be a p-channel metal-oxide-semiconductor field-effect transistor (PMOS). The second circuit arrangement 450 also includes a bias voltage input terminal 475.

[0084] The source terminal 454 of the transistor 453 is coupled to the negative terminal 459 of the depletion capacitor 457 and the second terminal 474 of the source inductor 472. The gate terminal 455 of the transistor 453 is coupled to the positive terminal 458 of the depletion capacitor 457 and the negative terminal 471 of the gate capacitor 469. The drain terminal 456 of the transistor 453 is coupled to the first terminal 461 of the resistor 460 and the positive terminal 464 of the output capacitor 463. 10

[0085] The positive terminal 470 of the gate capacitor 469 is coupled to the second terminal 468 of the gate inductor 466. The first terminal 467 of the gate inductor 466 is coupled to the input terminal 451. The negative terminal 462 of the output capacitor 463 15 is coupled to the output terminal 452. The first terminal 473 of the source inductor 472 is coupled to a third voltage reference point 476. The second terminal 462 of the resistor 460 is coupled to a fourth voltage reference point 477. In one embodiment, the fourth voltage reference point 477 may be ground. The bias voltage input terminal 475 is coupled between the negative terminal 471 of the gate capacitor 469 and the positive terminal 458 of the depletion capacitor 457. The bias voltage input terminal 475 may be 20 adapted to provide a bias voltage to the gate terminal 455 of the transistor 453.

[0086] The first circuit arrangement 400 and the second circuit arrangement 450 may be combined to form the amplifier 300 by stacking the transistor 403 of the first circuit arrangement 400 on top of the transistor 453 of the second circuit arrangement 450.

[0087] In one embodiment, the amplifier 300 may be a complementary current-reuse amplifier. The amplifier 300 may have a complementary current-reuse common-source (CS) topology where a NMOS CS amplifier (e.g. first transistor 304) is stacked on top of a PMOS CS amplifier (e.g. second transistor 306) to reuse the direct current (DC) among the two symmetrically stacked amplifiers. In short, the DC current can flow through both the NMOS CS amplifier (e.g. first transistor 304) and the PMOS CS amplifier (e.g. second transistor 306), i.e. through the drain terminal 312 of the first transistor 304 and the drain terminal 318 of the second transistor 306. The advantage of having this configuration in comparison to a conventional current-reuse topology is that no DC feedback circuitry is required to define the operating point of high impedance output node. No additional circuit or complexity is required. Less number of passive components is required for input matching. The common-source (CS) topology can provide improved noise and linearity performance.

[0088] Since only a small amount of DC current flows through the drain terminals 312, 318 of the transistors 304, 306, a small voltage drop occurs in both load resistors R_L (e.g. first and second resistors 334, 342) and 1-V supply voltage can still be used without headroom issues. In other words, a low voltage and ultra-low power design can be used for the amplifier 300. No additional power is required for the common-source (CS) topology of the amplifier 300. Both the first transistor M_{n1} 304 and the second transistor M_{p1} 306 are biased so that the gate-to-source voltage V_{GS} is close to the threshold voltage

V_{th} . The transistors 304, 306 are sized so that the voltage at node A is biased at $V_{DD}/2$ (supply voltage/2) to provide symmetric characteristics between the two stacked amplifiers. Node A is alternating current (ac) ground at 400 MHz due to the large bypass capacitor C_s (e.g. source capacitor 386). The large bypass capacitor C_s (e.g. source capacitor 386) is included for ac ground and stability. The source degeneration on-chip spiral inductor L_s (e.g. source inductor 380) is used for input impedance matching along with the depletion capacitors C_d 322, 328 and the gate inductor L_g 362. Since both the transconductance g_m and gate-to-source capacitance C_{gs} are increased in comparison to the SDCLNA 102 of Figure 1 at the same power consumption, the size of both the depletion capacitors C_d 322, 328 and the source inductor L_s 380 can be reduced, resulting in a smaller die area. The ac-coupled gate terminals 310, 316 and drain terminals 312, 318 of the first transistor M_{n1} 304 and the second transistor M_{p1} 306 are connected together, respectively, which results in both the input and output of the resulting amplifier 300 being single-ended with equal phases for the signal. The amplifier 300 operates as a differential mode due to the complementary characteristic of NMOS (e.g. the first transistor 304) and PMOS (e.g. the second transistor 306). This may result in a single-ended input-output differential amplifier 300.

[0089] Since the amplifier 300 effectively operates as a differential amplifier, the even-order distortion can be eliminated. Figure 5 shows a graph 500 of measured drain current i_{DS} , transconductance g_m , and first derivative of transconductance g_m' of a 120- $\mu\text{m}/0.18\text{-}\mu\text{m}$ NMOS and a 240- $\mu\text{m}/0.18\text{-}\mu\text{m}$ PMOS FET (see reference [1] I. Nam, B. Kim, and K. Lee, "CMOS RF amplifier and mixer circuits utilizing complementary characteristics of parallel combined NMOS and PMOS devices," *IEEE Trans. Microw.*

Theory and Tech., vol.53, no.5, pp. 1662-1671, May 2005). Plot 502 shows the measured total drain current i_{DS} plotted against a gate-to-source voltage V_{gs} . Plot 504 shows the transconductance g_m plotted against the gate-to-source voltage V_{gs} . Plot 506 shows the first derivative of transconductance g_m' plotted against the gate-to-source voltage V_{gs} .

- 5 Plot 506 shows that g_m' of NMOS and g_m' of PMOS have opposite signs.

[0090] A small signal drain current i_{ds} of a common source metal-oxide semiconductor field effect transistor (e.g. the first transistor 304 and the second transistor 306) can be expressed:

$$i_{ds} = I_{DS} + g_m v_{gs} + \frac{1}{2!} g_m' v_{gs}^2 + \frac{1}{2!} g_m'' v_{gs}^3 + \dots$$

- 10 wherein i_{ds} is small signal drain current of the transistor, I_{DS} is direct current (DC) drain current of the transistor, g_m is the transconductance, g_m' is the first derivative of the transconductance g_m , and v_{gs} is small signal gate-to-source voltage.

- [0091] From the above equation, it can be understood by a skilled person that g_m' causes second-order nonlinearity of the drain current. Since g_m' of NMOS (e.g. the first transistor 304) and g_m' of PMOS (e.g. the second transistor 306) have opposite signs, combining them can suppress the second-order nonlinearity of the drain current. A slight improvement in third-order nonlinearity can be obtained due to cancelling effect of g_m' . In other words, an improvement in the second order input intercept point IIP2 performance can lead to a slight enhancement in the third order input intercept point IIP3.

- 20 [0092] Figure 6 shows a schematic diagram of an AC (alternating current) equivalent circuit 600 of the amplifier 300. V_{sig_in} represents an input voltage of the circuit 600, i_{sig_n} represents a current passing through the first transistor 304, i_{sig_p} represents a current

passing through the second transistor 306, and V_{out} represents an output voltage of the circuit 600.

[0093] An external high inductance gate inductor L_g 362 may be employed for 50 Ω impedance matching and passive amplification. The input matching circuit amplifies the input voltage and noise from the antenna with the effective inductance of the input matching circuit. The input matching circuit may include the gate inductor L_g 362, the depletion capacitor C_{dn} 322, the depletion capacitor C_{dp} 328, and the source inductor L_s 380.

[0094] If the inductance is large enough, the output noise of the amplifier 300 will be dominated by the amplified input noise. The signal-to-noise ratio is not much degraded due to the input referred noise of the amplifier 300, and the resulting noise figure (NF) can be further improved.

[0095] Figure 7a shows a schematic diagram of high impedance passive amplification circuit 800. The circuit 800 has an antenna 802 and an amplifier 804. The antenna 802 has an inductor 806 and a resistor 808 connected in series. The antenna 802 also has a capacitor 810 connected in parallel with a series connection 812 of the inductor 806 and the resistor 808. The amplifier 804 may be a low noise amplifier. In one embodiment, the amplifier 804 may correspond to the amplifier 200 or the amplifier 300 as described above.

[0096] Figure 7b shows a schematic diagram of an equivalent circuit 814 of the circuit 800 of Figure 7a. The equivalent circuit 814 includes the inductor 806, the resistor 808 and a voltage source 816 connected in series. The equivalent circuit 814 also includes the capacitor 810 connected in parallel with a series connection 818 of the

inductor 806, the resistor 808 and the voltage source 818. The equivalent circuit 814 includes a further capacitor 820 connected in parallel with the capacitor 810, and a further resistor 821 connected in parallel with the further capacitor 820. The equivalent circuit 814 is divided into a first portion 822 and a second portion 824 by a dotted line 5 826. The first portion 822 of the equivalent circuit 814 includes the inductor 806, the resistor 808, the voltage source 818 and the capacitor 810. The second portion 824 of the equivalent circuit 814 includes further capacitor 820 and the further resistor 821. A source impedance Z_S can be calculated based on the first portion 822 of the equivalent circuit 814. A load impedance Z_L can be calculated based on the second portion 824 of 10 the equivalent circuit 814. In other words, the source impedance Z_S shown in Figure 7b may be calculated based on the impedance of the antenna 802 shown in Figure 7a. The load impedance Z_L shown in Figure 7a may be calculated based on the impedance of the amplifier 804 shown in Figure 7b.

[0097] Figure 7c shows a schematic diagram of an equivalent circuit 828 of the 15 circuit 800 for noise calculation. The equivalent circuit 828 includes the inductor 806, the resistor 808 and a voltage source 816 connected in series. The equivalent circuit 828 includes the capacitor 810 connected in parallel with a series connection 818 of the inductor 806, the resistor 808 and the voltage source 818, forming a parallel arrangement 830. The equivalent circuit 828 also includes the amplifier 804. One end 832 of the 20 parallel arrangement 830 is coupled to an input terminal 834 of the amplifier 804. The other end 836 of the parallel arrangement 830 is coupled to ground 838.

[0098] The voltage gain of the amplifier 804 can be calculated using the following equation:

$$A_v = Q_{in} \cdot g_m \cdot R_{Load} \cdot \frac{Z_L}{Z_S + Z_L}$$

where A_v is voltage gain of the amplifier 804, Q_{in} is an input charge (e.g. charge of capacitor 810), g_m is transconductance, R_{Load} is load resistance (e.g. resistance of resistor 808), Z_L is load impedance, and Z_S is source impedance.

- 5 The noise figure (NF) can be calculated using the following equation:

$$NF = 10 \log \left(\frac{V_n^2 + V_{LNA_inputrefer}^2}{V_n^2} \right) = 10 \log \left(\frac{A_v^2 Q_{in}^2 V_n^2 + V_{LNA_outputrefer}^2}{A_v^2 Q_{in}^2 V_n^2} \right) \quad (1)$$

where NF is noise figure, V_n is voltage of the voltage source 816, $V_{LNA_inputrefer}$ is a reference input voltage of the amplifier 804, A_v is voltage gain, Q_{in} is a quality factor of the input matching circuit, and $V_{LNA_outputrefer}$ is a reference input voltage of the amplifier 804.

Referring to equation (1), if $A_v^2 Q_{in}^2 V_n^2 \gg V_{LNA}^2$, the output noise is dominated by the input noise and the noise figure can be effectively reduced significantly.

[0099] The maximum passive amplification can be applied to the amplifier 300 for non-50Ω impedance matching applications. Additional gain, improved NF and further reduction in power can be achieved by using the maximum passive amplification.

[00100] The amplifier 300 and the conventional SDCLNA 100 are simulated at about 1.0 V, about 27°C and with 50Ω impedance matching. Figure 8 shows a graph of s-parameter plotted against frequency. Plot 902 shows insertion loss (S21) of the conventional SDCLNA 100 plotted against frequency. Plot 904 shows input return loss (S11) of the conventional SDCLNA 100 plotted against frequency. Plot 906 shows insertion loss (S21) of the amplifier 300 plotted against frequency. Plot 908 shows input return loss (S11) of the amplifier 300 plotted against frequency. It can be observed from

graph 900 that the s-parameters of the conventional SDCLNA 100 and the amplifier 300 are similar.

[00101] Figure 9 shows a graph 1000 of noise figure (NF) plotted against frequency.

Plot 1002 shows the NF of the conventional SDCLNA 100 plotted against frequency.

5 Plot 1004 shows the minimum NF of the conventional SDCLNA 100 plotted against frequency. Plot 1006 shows the NF of the amplifier 300 plotted against frequency. Plot 1008 shows the minimum NF of the amplifier 300 plotted against frequency. The NF of the conventional SDCLNA 100 is about 2.6 dB. The NF of the amplifier 300 is about 1.8 dB. In comparison to the conventional SDCLNA 100, the NF of the amplifier 300 is
10 improved at the same power consumption. The NF of the amplifier 300 may be improved due to the increased transconductance of the current reuse structure of the amplifier 300.

[00102] Figure 10a shows the simulated third order input intercept point IIP3 of the conventional SDCLNA 100. The IIP3 of the conventional SDCLNA 100 is about -

10.7dBm. Figure 10b shows the simulated third order input intercept point IIP3

15 of the amplifier 300. The IIP3 of the amplifier 300 is about -6.5dBm. It can be observed that in comparison to the conventional SDCLNA 100, the IIP3 of the amplifier 300 is improved.

[00103] Figure 11 shows a table 1200 listing the simulation results of the conventional SDCLNA 100 and the amplifier 300. Column 1202 shows the targeted simulation results.

20 Column 1204 shows the simulation results of the conventional SDCLNA 100. Column 1206 shows the simulation results of the amplifier 300. The amplifier 300 shows better performance than the conventional SDCLNA 100.

[00104] Figure 12 shows a graph 1300 illustrating experimental results of the amplifier 300 at 50 Ω impedance matching and at a frequency range of 401 MHz to 406 MHz. Plot 1302 shows the insertion loss (S21) of the amplifier 300 plotted against frequency. Plot 1304 shows the input return loss (S11) of the amplifier 300 plotted against frequency. 5 Plot 1306 shows the noise figure (NF) of the amplifier 300 plotted against frequency. The NF of the amplifier 300 with 50 Ω matching is about 2.9 dB.

[00105] Figure 13 shows a graph 1400 illustrating third order input intercept point (IIP3) linearity measurements of the amplifier 300. Plot 1402 shows output power plotted against input power for a fundamental signal. Plot 1404 shows output power plotted 10 against input power for a third-order product of the fundamental signal. A fitted line 1406 for plot 1402 is drawn and a fitted line 1408 for plot 1404 is drawn. It can be observed from an intersection point 1410 of line 1406 and line 1408 that a -8.1 dBm of IIP3 is measured for the amplifier 300.

[00106] Figure 14 shows a table 1500 listing simulation results of four conventional 15 amplifiers (see references [2] "A 1V wireless transceiver for an ultra-low-power SoC for biotelemetry applications," JSSC2008, [3] "A 1V wireless transceiver for an ultra-low-power SoC for biotelemetry applications," JSSC2008, [4] "A subthreshold low-noise amplifier optimized for ultra-low-power applications in the ISM band," TMTT2008, and [5] "A novel ultra-low power (ULP) low noise amplifier using differential inductor 20 feedback" ESSCIRC2006), preliminary measurements of the amplifier 300 with 50 Ω impedance matching, and simulation results of the amplifier 300 with high impedance matching (non-50 Ω matching). Columns 1502 to 1508 show the simulation results of the four conventional amplifiers respectively. Column 1510 shows the preliminary

measurements of the amplifier 300 with 50Ω impedance matching. Column 1512 shows the simulation results of the amplifier 300 with high impedance matching (non-50Ω matching).

[00107] With 50Ω impedance matching, the amplifier 300 has a gain of 20.2 dB, a
 5 noise figure of 2.9 dB, an IIP3 of -8.1 dBm, a power consumption of 150 μW at 1-V and a figure of merit (F.O.M.) of 20. With high impedance matching, the amplifier 300 has a gain of 22 dB, a noise figure of 1.5 dB, an IIP3 of -13 dBm, a power consumption of 100 μW at 1-V and a figure of merit (F.O.M.) of 22.6. In comparison with the four conventional amplifiers, the amplifier 300 exhibits an improved performance with 50Ω
 10 impedance matching and with high impedance matching.

[00108] Figure 15 shows a graph 1600 illustrating the simulation results of the amplifier 300 with high impedance passive network (non-50Ω matching). Plot 1602 shows the insertion loss (S21) of the amplifier 300 plotted against frequency. Plot 1604 shows the input return loss (S11) of the amplifier 300 plotted against frequency. Plot
 15 1606 shows the noise figure (NF) of the amplifier 300 plotted against frequency. The NF of the amplifier 300 with non-50Ω matching is about 1.6 dB which is improved as compared to the NF of the amplifier 300 with 50Ω matching (e.g. 1.8 dB (see Figure 9) and 2.9 dB (see Figure 14)).

[00109] Simulation of the noise figure (NF) of the amplifier 300 at high impedance
 20 (non-50Ω matching) can be carried out using various methods. One possible method is the noise voltage method. Referring to the above-mentioned equation (1), $V_n^2 + V_{LNA_inputrefer}^2$ and $A_v^2 Q_{in}^2 V_n^2 + V_{LNA_outputrefer}^2$ can be simulated. The NF of the amplifier 300 obtained from the noise voltage method is 1.617 dB. Another possible method is the

S-parameter method where serial network is transformed to parallel network and conventional S-parameter simulation is used. The NF of the amplifier 300 obtained from the S-parameter method is 1.566 dB.

[00110] The amplifier 300 has a current reuse topology and requires no additional
5 power or complexity required. Improvement of noise and linearity performance can be achieved without increase in power consumption. Power consumption can be reduced by more than 50%. Application of maximum passive amplification to the amplifier 300 to further reduce the power consumption for applications where 50 Ω input matching may not be required. Nevertheless, high impedance matching can still result in further
10 reduction in power consumption of the amplifier 300. Smaller passive components can be used in the amplifier 300 for higher integration.

[00111] The amplifier 300 can be employed for receiver radio frequency (RF) front-ends as a low-noise amplifier in different applications (e.g. ultra-low-power implantable and wearable wireless sensors for biomedical applications). For example, the amplifier
15 300 can be applied to a full transceiver for MedRadio regulation compliant implant and wearable sensor applications where sufficient gain and noise performances are required and ultra-low-power consumption for prolonged battery life is provided. The amplifier 300 can be used in a low-voltage sub-mW transceiver for biomedical applications where the amplifier 300 is a key building block in the receiver part.

20 [00112] Figure 16 shows a block diagram of a receiver RF front-end 1800. The receiver RF front-end 1800 includes an amplifier 1802 (e.g. low noise amplifier (LNA)). The amplifier 1802 may correspond to the amplifier 300 described above. The receiver RF front-end 1800 also includes a transconductor 1804, an in-phase/quadrature (I/Q)

folded active mixer 1806, a first intermediate frequency (IF) buffer 1808a and a second IF buffer 1808b, and a two-stage passive polyphase filter (PPF) 1810 with a first buffer 1812a and a second buffer 1812b. The receiver RF front-end 1800 has an antenna 1814.

[00113] The antenna 1814 is coupled to an input terminal 1816 of the amplifier 1802.

- 5 An output terminal 1818 of the amplifier 1802 is coupled to an input terminal 1820 of the transconductor 1804. An output terminal 1822 of the transconductor 1804 is coupled to a first input terminal 1824 and a second input terminal 1826 of the I/Q folded mixer 1806. A first output terminal 1828 and a second output terminal 1830 of the I/Q folded mixer 1806 are coupled to a first input terminal 1832 and a second input terminal 1834 of the
- 10 first IF buffer 1808a respectively. A third output terminal 1836 and a fourth output terminal 1838 of the I/Q folded mixer 1806 are coupled to a first input terminal 1840 and a second input terminal 1842 of the second IF buffer 1808b respectively. The first IF buffer 1808a has a first output terminal 1844 and a second output terminal 1846 for transmitting in-phase signals. The second IF buffer 1808b has a first output terminal 1848
- 15 and a second output terminal 1850 for transmitting quadrature signals. The PPF 1810 has a first input terminal 1852 and a second input terminal 1854 for receiving I/Q local oscillator (LO) signal from an external LO source (not shown). A first output terminal 1856 and a second output terminal 1858 of the PPF 1810 are coupled to a first input terminal 1860 and a second input terminal 1862 of the first buffer 1812a respectively. A
- 20 third output terminal 1864 and a fourth output terminal 1866 of the PPF 1810 are coupled to a first input terminal 1868 and a second input terminal 1870 of the second buffer 1812b respectively. A first output terminal 1872 and a second output terminal 1874 of the first buffer 1812a are coupled to a third input terminal 1876 and a fourth input terminal

1878 of the I/Q folded mixer 1806 respectively. A first output terminal 1880 and a second output terminal 1882 of the second buffer 1812b are coupled to a fifth input terminal 1884 and a sixth input terminal 1886 of the I/Q folded mixer 1806 respectively.

[00114] The two-stage passive polyphase filter 1810 with a first buffer 1812a and a second buffer 1812b are used to drive the mixer 1806 for I/Q LO signal generation from the external LO source (not shown). The two poles $1/R_1C_1$ and $1/R_2C_2$ are placed at 395 and 410 MHz, respectively, to broaden the frequency response. Considering low power consumption, the LO buffer (e.g. including first buffer 1812a and second buffer 1812b) may be an ac-coupled inverter type differential amplifier where a large differential swing can be obtained for a given operating current due to its push-pull operation.

[00115] In addition, a constant-gm bias circuitry may be included to supply accurate reference current to all the blocks (e.g. amplifier 1802, transconductor 1804, I/Q folded active mixer 1806, first IF buffer 1808a, second IF buffer 1808b, PPF 1810 with first buffer 1812a and second buffer 1812b) of the receiver RF front-end 1800 regardless of process, voltage, and temperature (PVT) variations. Single-ended paths are employed up to the mixer 1806 to minimize the current consumption and to avoid the use of a lossy balun at the receiver input. To minimize power in each of the blocks, low-power design techniques such as current-reuse and weak inversion biasing are utilized with a 1-V supply voltage through the receiver chain (e.g. receiver RF front-end 1800).

[00116] The antenna 1814 of the receiver RF front-end 1800 has a RF input band of 401-406 MHz. However, the narrow 100 kHz channel bandwidth of the 401-402 MHz and 405-406 MHz wing bands in MedRadio may severely be corrupted by the flicker noise and DC offset at baseband. Therefore, the RF input band of 401-406 MHz is

downconverted to a low-IF of 500 kHz. The 500 kHz IF is selected as a compromise in order to avoid the 1/f noise and at the same time minimize the required power consumption of the IF blocks (e.g. first IF buffer 1808a and second IF buffer 1808b).

[00117] The mixer 1806 is used to alleviate the headroom issue and have separate
5 biasing for the transconductor 1804 and the switching part of the mixer 1806 for better optimization. Figure 17 shows a schematic diagram of the folded active mixer 1806. The mixer 1806 has seven p-channel MOSFET (PMOS) 1902a-g, one n-channel MOSFET (NMOS) 1904, ten resistors 1906a-j, eleven capacitors 1908a-k and one current source 1910. A source terminal 1912 of the first PMOS 1902a, a source terminal 1913 of the
10 second PMOS 1902b and a source terminal 1914 of the seventh PMOS 1902g are coupled to a first voltage reference point 1915. A gate terminal 1916 of the first PMOS 1902a is coupled to a negative terminal 1917 of the first capacitor 1908a. A positive terminal 1918 of the first capacitor 1908a is coupled to a first terminal 1919 of the first resistor 1906a and a gate terminal 1920 of the NMOS 1904. A drain terminal 1921 of the
15 first PMOS 1902a is coupled to a second terminal 1922 of the first resistor 1906a, a drain terminal 1923 of the NMOS 1904, and a positive terminal 1924 of the second capacitor 1908b. A source terminal 1925 of the NMOS 1904 is coupled to ground 1901. The mixer 1806 has a first input terminal 1926 coupled to the positive terminal 1918 of the first capacitor 1908a, the first terminal 1919 of the first resistor 1906a and the gate terminal
20 1920 of the NMOS 1904. The mixer 1806 also has a bias voltage input terminal 1927 coupled between the gate terminal 1916 of the first PMOS 1902a and the negative terminal 1917 of the first capacitor 1908a.

[00118] The gate terminal 1928 of the second PMOS 1902b is coupled to a first terminal 1929 of the second resistor 1906b. A second terminal 1930 of the second resistor 1906b is coupled to a gate terminal 1931 of the seventh PMOS 1902g, a positive terminal 1932 of the third capacitor 1908c, a first terminal 1933 of the current source 1910 and a drain terminal 1934 of the seventh PMOS 1902g. The negative terminal 1935 of the third capacitor 1908c and the second terminal 1936 of the current source 1910 are respectively coupled to ground 1901. The drain terminal 1937 of the second PMOS 1902b is coupled to a negative terminal 1938 of the second capacitor 1908b, a source terminal 1940 of the third PMOS 1902c, a source terminal 1941 of the fourth PMOS 1902d, a source terminal 1942 of the fifth PMOS 1902e, and a source terminal 1943 of the sixth PMOS 1902f.

[00119] A gate terminal 1944 of the third PMOS 1902c is coupled to a negative terminal 1945 of the fourth capacitor 1908d and a first terminal 1946 of the third resistor 1906c. A gate terminal 1947 of the fourth PMOS 1902d is coupled to a negative terminal 1948 of the fifth capacitor 1908e and a first terminal 1949 of the fourth resistor 1906d. A second terminal 1950 of the third resistor 1906c is coupled to a second terminal 1951 of the fourth resistor 1906d. A drain terminal 1952 of the third PMOS 1902c is coupled to a positive terminal 1953 of the sixth capacitor 1908f and a first terminal 1954 of the fifth resistor 1906e. A negative terminal 1955 of the sixth capacitor 1908f is coupled to a second terminal 1956 of the fifth resistor 1906e. The negative terminal 1955 of the sixth capacitor 1908f and second terminal 1956 of the fifth resistor 1906e are coupled to ground 1901. A drain terminal 1957 of the fourth PMOS 1902d is coupled to a positive terminal 1958 of the seventh capacitor 1908g and a first terminal 1959 of the sixth resistor 1906f. A negative terminal 1960 of the seventh capacitor 1908g is coupled to a

second terminal 1961 of the sixth resistor 1906f. The negative terminal 1960 of the seventh capacitor 1908g and the second terminal 1961 of the sixth resistor 1906f are coupled to ground 1901.

[00120] The mixer 1806 includes a second input terminal 1962 coupled to a positive terminal 1963 of the fourth capacitor 1908d, and a third input terminal 1964 coupled to a positive terminal 1965 of the fifth capacitor 1908e. The mixer 1806 includes a first output terminal 1966 coupled between the drain terminal 1952 of the third PMOS 1902c and a coupling point 1967. The mixer 1806 includes a second output terminal 1968 coupled between the drain terminal 1957 of the fourth PMOS 1902d and a coupling point 1969. A bias voltage V_b is applied between the second terminal 1950 of the third resistor 1906c and the second terminal 1951 of the fourth resistor 1906d.

[00121] A gate terminal 1970 of the fifth PMOS 1902e is coupled to a negative terminal 1971 of the eighth capacitor 1908h and a first terminal 1972 of the seventh resistor 1906g. A gate terminal 1973 of the sixth PMOS 1902f is coupled to a negative terminal 1974 of the ninth capacitor 1908i and a first terminal 1975 of the eighth resistor 1906h. A second terminal 1976 of the seventh resistor 1906g is coupled to a second terminal 1977 of the eighth resistor 1906h. A drain terminal 1978 of the fifth PMOS 1902e is coupled to a positive terminal 1979 of the tenth capacitor 1908j and a first terminal 1980 of the ninth resistor 1906i. A negative terminal 1981 of the tenth capacitor 1908j is coupled to a second terminal 1982 of the ninth resistor 1906i. The negative terminal 1981 of the tenth capacitor 1908j and the second terminal 1982 of the ninth resistor 1906i are coupled to ground 1901. A drain terminal 1983 of the sixth PMOS 1902f is coupled to a positive terminal 1984 of the eleventh capacitor 1908k and a first

terminal 1985 of the tenth resistor 1906j. A negative terminal 1986 of the eleventh capacitor 1908k is coupled to a second terminal 1987 of the tenth resistor 1906j. The negative terminal 1986 of the eleventh capacitor 1908k and the second terminal 1987 of the tenth resistor 1906j are coupled to ground 1901.

5 [00122] The mixer 1806 includes a fourth input terminal 1988 coupled to a positive terminal 1989 of the eighth capacitor 1908h, and a fifth input terminal 1990 coupled to a positive terminal 1991 of the ninth capacitor 1908i. The mixer 1806 includes a third output terminal 1992 coupled between the drain terminal 1978 of the fifth PMOS 1902e and a coupling point 1993. The mixer 1806 includes a fourth output terminal 1994
10 coupled between the drain terminal 1983 of the sixth PMOS 1902f and a coupling point 1995. A bias voltage V_b is applied between the second terminal 1976 of the seventh resistor 1906g and the second terminal 1977 of the eighth resistor 1906h.

[00123] Referring back to Figure 16, the transconductor 1804 is an ac-coupled current reuse inverter type where the biasing for the transistor M_{p1} (e.g. first PMOS 1902a) and
15 transistor M_{n1} (e.g. NMOS 1904) are separated in order to support low supply voltage and reduce its sensitivity to PVT variations. A single tail current source M_{p2} (e.g. second PMOS 1902b) is used in the I/Q mixer 1806 in order to minimize mismatch between the two mixer paths. The mixer 1806 is a single-balanced active mixer with parallel RC load for low-pass filtering in the baseband.

20 [00124] The receiver RF front-end 1800 can be fabricated in one-poly six-metal (1P6M) 0.18- μ m CMOS process. The chip microphotograph 2000 of the receiver RF front-end 1800 is shown in Figure 18. The total chip area of the core 2002 (e.g. including the amplifier 1802, the I/Q mixer 1806, the first IF buffer 1808a, the second IF buffer 1808b,

the PPF 1810 with the first buffer 1812a and the second buffer 1812b) is 0.7 mm². All pads include electrostatic discharge (ESD) circuits using diode pairs.

[00125] Figure 19 shows a graph 2100 of measured conversion gain and input return loss (S11) of the receiver front-end plotted against RF input frequency at an intermediate frequency (IF) of 500 kHz. The external LO signal is provided by a signal generator. Plot 2102 shows measured conversion gain plotted RF input frequency at an IF of 500 kHz. Plot 2104 shows input return loss (S11) plotted against RF input frequency at an IF of 500 kHz. It can be observed from plot 2102 that there is a conversion gain of 28.7 dB.

[00126] Figure 20 shows a graph 2200 of noise figure (NF) measurement plotted against output frequency of the receiver front-end. It can be observed from the graph 2200 that less than 5.5 dB of double-sideband (DSB) NF is obtained at an IF of 500 kHz to 2 MHz and at 28.7 dB of conversion gain.

[00127] Figure 21 shows a graph 2300 of third order input intercept point (IIP3) linearity measurement where two-tones at 402 and 402.1 MHz are applied to the input of the receiver. Plot 2302 shows output power plotted against input power for a fundamental signal. Plot 2304 shows output power plotted against input power for a third-order product of the fundamental signal. A fitted line 2306 for plot 2302 is drawn and a fitted line 2308 for plot 2304 is drawn. It can be observed from an intersection point 2310 of line 2306 and line 2308 that a -25 dBm of IIP3 is measured for the RF receiver front-end.

[00128] Figure 22 shows a table 2400 showing the measured results of four conventional receivers (see references [6] R. van Langevelde, M. van Elzakker, D. van Goor, H. Termeer, J. Moss, and A.J. Davie, "An ultra-low-power 868/915 MHz RF transceiver for wireless sensor network applications," in *Proc. IEEE RF Integ. Circuits*

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[00129] In one embodiment, the receiver RF front-end 1800 may be a low-voltage ultra-low-power 401-406 MHz MedRadio receiver RF front-end targeted for wearable sensor applications. The receiver RF front-end 1800 may be an ultra-low-power 401-406 MHz Medical Device Radiocommunication Service (MedRadio) receiver RF front-end for biomedical telemetry applications implemented using 0.18- μ m CMOS technology with a 1-V supply voltage. The receiver RF front-end 1800 employs the amplifier 300 (e.g. complementary current-reuse low-noise amplifier (CCRLNA)) which shows

enhanced noise and linearity performance in comparison to the well-known source degeneration cascode LNA (SDCLNA) 100 at equal power consumption and design conditions. The receiver RF front-end 1500 including the amplifier 1802 (e.g. amplifier/CCRLNA 300), transconductor 1804, I/Q folded mixer 1806, and LO buffers 5 1812a, 1812b can achieve a conversion gain of 28.7 dB, NF of 5.5 dB, and IIP3 of -25 dBm while consuming less than 500 μ W (e.g. 490 μ W) from a 1-V supply voltage and occupy 0.7mm² of core die area. The receiver RF front-end 1800 exhibits enhanced noise and linearity performance.

[00130] While embodiments of the invention have been particularly shown and 10 described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore 15 intended to be embraced.

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CLAIMS

What is claimed is:

- 5 1. An amplifier, comprising:
 an input terminal;
 a first transistor of a first conductivity and a second transistor of a second
 conductivity, each transistor comprising a source terminal, a gate terminal and a drain
 terminal respectively, the source terminal of the first transistor being coupled to the
10 source terminal of the second transistor, and the gate terminal of the first transistor and
 the gate terminal of the second transistor being coupled to the input terminal; and
 an output terminal coupled to the drain terminal of the first transistor and the drain
 terminal of the second transistor.
- 15 2. The amplifier of claim 1,
 further comprising a first depletion capacitor coupled between the gate terminal
 and the source terminal of the first transistor.
3. The amplifier of claim 2,
20 wherein the first depletion capacitor comprises a positive terminal and a negative
 terminal, wherein the positive terminal of the first depletion capacitor is coupled to the
 gate terminal of the first transistor and the negative terminal of the first depletion
 capacitor is coupled to the source terminal of the first transistor.

4. The amplifier of any one of claims 1 to 3,
further comprising a second depletion capacitor coupled between the gate terminal and the source terminal of the second transistor.

5

5. The amplifier of claim 4,
wherein the second depletion capacitor comprises a positive terminal and a negative terminal, wherein the positive terminal of the second depletion capacitor is coupled to the gate terminal of the second transistor and the negative terminal of the
10 second depletion capacitor is coupled to the source terminal of the second transistor.

6. The amplifier of any one of claims 1 to 5,
further comprising a first resistor coupled between the drain terminal of the first transistor and a first voltage reference point.

15

7. The amplifier of claim 6,
wherein the first resistor comprises a first terminal and a second terminal, wherein the first terminal of the first resistor is coupled to the drain terminal of the first transistor and the second terminal of the first resistor is coupled to the first voltage reference point.

20

8. The amplifier of any one of claims 1 to 7,
further comprising a second resistor coupled between the drain terminal of the second transistor and a second voltage reference point.

9. The amplifier of claim 8,
wherein the second resistor comprises a first terminal and a second terminal,
wherein the first terminal of the second resistor is coupled to the drain terminal of the
5 second transistor and the second terminal of the second resistor is coupled to the second
voltage reference point.
10. The amplifier of any one of claims 1 to 9,
further comprising a first output capacitor coupled between the drain terminal of
10 the first transistor and the output terminal.
11. The amplifier of claim 10,
wherein the first output capacitor comprises a positive terminal and a negative
terminal, wherein the positive terminal of the first output capacitor is coupled to the drain
15 terminal of the first transistor and the first terminal of the first resistor and the negative
terminal of the first output capacitor is coupled to the output terminal.
12. The amplifier of any one of claims 1 to 11,
further comprising a second output capacitor coupled between the drain terminal
20 of the second transistor and the output terminal.
13. The amplifier of claim 12,

wherein the second output capacitor comprises a positive terminal and a negative terminal, wherein the positive terminal of the second output capacitor is coupled to the drain terminal of the second transistor and the first terminal of the second resistor and the negative terminal of the second output capacitor is coupled to the output terminal.

5

14. The amplifier of any one of claims 5 to 13, further comprising:

a gate inductor comprising a first terminal and a second terminal;

a first gate capacitor comprising a positive terminal and a negative terminal;

a second gate capacitor comprising a positive terminal and a negative terminal;

10 wherein the first terminal of the gate inductor is coupled to the input terminal, and the second terminal of the gate inductor is coupled to the positive terminal of the first gate capacitor and the positive terminal of the second gate capacitor;

wherein the negative terminal of the first gate capacitor is coupled to the gate terminal of the first transistor and the positive terminal of the first depletion capacitor;

15 wherein the negative terminal of the second gate capacitor is coupled to the gate terminal of the second transistor and the positive terminal of the second depletion capacitor.

15. The amplifier of any one of claims 5 to 14, further comprising:

20 a source inductor comprising a first terminal and a second terminal;

a source capacitor comprising a positive terminal and a negative terminal;

wherein the first terminal of the source inductor is coupled to the source terminal of the first transistor, the negative terminal of the first depletion capacitor, the source

terminal of the second transistor and the negative terminal of the second depletion capacitor;

wherein the second terminal of the source inductor is coupled to the positive terminal of the source capacitor;

5 wherein the negative terminal of the source capacitor is coupled to the second voltage reference point.

16. The amplifier of any one of claims 1 to 15,

 further comprising a first bias voltage input terminal adapted to provide a first
10 bias voltage to the gate terminal of the first transistor.

17. The amplifier of claim 16,

 wherein the first bias voltage input terminal is provided between the negative
terminal of the first gate capacitor and the positive terminal of the first depletion
15 capacitor.

18. The amplifier of any one of claims 1 to 17,

 further comprising a second bias voltage input terminal adapted to provide a
second bias voltage to the gate terminal of the second transistor.

20

19. The amplifier of claim 18,

wherein the second bias voltage input terminal is provided between the negative terminal of the second gate capacitor and the positive terminal of the second depletion capacitor.

5 20. The amplifier of any one of claims 1 to 19,

wherein the first transistor comprises a n-channel metal-oxide-semiconductor field-effect transistor.

21. The amplifier of any one of claims 1 to 20,

10 wherein the second transistor comprises a p-channel metal-oxide-semiconductor field-effect transistor.

22. The amplifier of any one of claims 8 to 21,

wherein the second voltage reference point is ground.

15

23. A transceiver comprising an amplifier of any one of claims 1 to 22.

24. An amplifier, comprising:

an input terminal and an output terminal, wherein the input terminal and the

20 output terminal are single-ended with equal phases for a signal; and

a core configured to operate as a differential mode.