ABSTRACT

Provided herein is a memory device that may include a string, a voltage generation circuit, a page buffer, and a channel initializing circuit. The string may include select transistors and memory cells coupled in series between a bit line and a source line. The page buffer may be configured to precharge or discharge the bit line. The voltage generation circuit may be configured to apply a turn-on voltage or a turn-off voltage to select lines coupled to the select transistors, apply at least one operating voltage to word lines coupled to the memory cells, or discharge the select lines or the word lines. The channel initializing circuit may be configured to control the voltage generation circuit and the page buffer so as to initialize a channel of the string when an operation performed on the memory cells is completed or is suspended before being completed.

FIG. 7B