WHAT IS CLAIMED IS:

1. A clock converting circuit comprising:

a first switch connected between a first input node for receiving a second input clock and a first node and configured to operate in response to a first logic state of a first input clock, the second input clock delayed with respect to the first input clock as much as 90 degrees;

a second switch connected between a second input node for receiving the first input clock and a second node and configured to operate in response to a second logic state of the second input clock; and

a third switch connected between the second node and a ground node and configured to operate in response to a first logic state of the second input clock opposite to the second logic state of the second input clock,

wherein the clock converting circuit is configured to output a first output clock and a first inverted output clock opposite to the first output clock based on the first and second input clocks.

2. The clock converting circuit of claim 1, further comprising:

a fourth switch connected between the first node and a power node and configured to operate in response to a second logic state of the first input clock opposite to the first logic state of the first input clock.

3. The clock converting circuit of claim 1, further comprising:

a fourth switch connected between a third input node for receiving a third input clock delayed with respect to the first input clock as much as 180 degrees and a third node

and configured to operate in response to the first logic state of the second input clock;

a fifth switch connected between the first input node and a fourth node and configured to operate in response to a second logic state of the third input clock;

a sixth switch connected between the fourth node and the ground node and configured to operate in response to a first logic state of the third input clock opposite to the second logic state of the third input clock;

a seventh switch connected between a fourth input node for receiving a fourth input clock delayed with respect to the first input clock as much as 270 degrees and a fifth node and configured to operate in response to the first logic state of the third input clock;

an eighth switch connected between the third input node and a sixth node and configured to operate in response to a second logic state of the fourth input clock;

a ninth switch connected between the sixth node and the ground node and configured to operate in response to a first logic state of the fourth input clock opposite to the second logic state of the fourth input clock;

a tenth switch connected between the second input node and a seventh node and configured to operate in response to the first logic state of the fourth input clock;

an eleventh switch connected between the fourth input node and an eighth node and configured to operate in response to a second logic state of the first input clock opposite to the first logic state of the first input clock; and

a twelfth switch connected between the eighth node and the ground node and configured to operate in response to the first logic state of the first input clock.

4. The clock converting circuit of claim 3, further comprising:

a thirteenth switch connected between the first node and a power node and configured to operate in response to the second logic state of the first input clock;

a fourteenth switch connected between the third node and the power node and configured to operate in response to the second logic state of the second input clock;

a fifteenth switch connected between the fifth node and the power node and configured to operate in response to the second logic state of the third input clock; and

a sixteenth switch connected between the seventh node and the power node and configured to operate in response to the second logic state of the fourth input clock.

5. The clock converting circuit of claim 1, wherein the first switch includes a first transmission gate configured to operate in response to the first input clock and a third input clock,

wherein the second switch includes a second transmission gate configured to operate in response to the second input clock and a fourth input clock,

wherein the third input clock is delayed with respect to the first input clock as much as 180 degrees, and

wherein the fourth input clock is delayed with respect to the first input clock as much as 270 degrees.

6. The clock converting circuit of claim 5, wherein the first transmission gate includes:

a first NMOS transistor connected between the first input node and the first node and configured to operate in response to the first input clock; and

a first PMOS transistor connected between the first input node and the first node and configured to operate in response to the third input clock, and

wherein the second transmission gate includes:

a second NMOS transistor connected between the second input node and the second

node and configured to operate in response to the fourth input clock; and

a second PMOS transistor connected between the second input node and the second node and configured to operate in response to the second input clock.

7. The clock converting circuit of claim 6, further comprising:

a fourth switch connected between the first node and a power node and configured to operate in response to a second logic state of the first input clock opposite to the first logic state of the first input clock,

wherein the third switch includes:

a third NMOS transistor connected between the second node and the ground node and configured to operate in response to the second input clock, and

wherein the fourth switch includes:

a third PMOS transistor connected between the first node and the power node and configured to operate in response to the first input clock.

8. The clock converting circuit of any one of claims 1 to 7, further comprising:

a first inverter configured to invert a voltage of the first node and to output the first output clock; and

a second inverter configured to invert a voltage of the second node and to output the first inverted output clock opposite to the first output clock.

9. The clock converting circuit of any one of claims 1 to 7, further comprising:

a first latch inverter configured to invert a voltage of the first node and to output an inverted voltage of the first node to the second node; and

a second latch inverter configured to invert a voltage of the second node and to

output an inverted voltage of the second node to the first node.

10. The clock converting circuit of any one of claims 1 to 7, further comprising:

N first buffers connected in series between the first node and a first output node of generating the first inverted output clock; and

M second buffers connected in series between the second node and a second output node of generating the first output clock opposite to the first inverted output clock, and

wherein the “N” and the “M” are natural numbers.

11. The clock converting circuit of claim 10, wherein the “N” is equal to the “M”.

12. The clock converting circuit of claim 10 or claim 11, wherein a first time interval taken for the N first buffers to transfer a voltage of the first node to the first output node is equal to a second time interval taken for the M second buffers to transfer a voltage of the second node to the second output node.

13. A clock converting circuit comprising:

first to fourth clock circuits configured to generate an output four-phase clock including first to fourth output clocks, based on an input four-phase clock including first to fourth input clocks,

wherein the first clock circuit includes:

a first switch connected between a first input node for receiving the second input clock and a first node and configured to operate in response to a first logic state of the first input clock;

a second switch connected between a second input node for receiving the first input

clock and a second node and configured to operate in response to a second logic state of the second input clock; and

a third switch connected between the second node and a ground node and configured to operate in response to a first logic state of the second input clock opposite to the second logic state of the second input clock, and

wherein the first clock circuit is configured to generate the first output clock and a first inverted output clock opposite to the first output clock based on the first and second input clocks.

14. The clock converting circuit of claim 13,

wherein the second clock circuit is configured to generate the second output clock and a second inverted output clock opposite to the second output clock based on the second and third input clocks,

wherein the third clock circuit is configured to generate the third output clock and a third inverted output clock opposite to the third output clock based on the third and fourth input clocks, and

wherein the fourth clock circuit is configured to generate the fourth output clock and a fourth inverted output clock opposite to the fourth output clock based on the fourth and first input clocks.

15. The clock converting circuit of claim 13 or claim 14, wherein the second input clock is delayed with respect to the first input clock as much as 90 degrees,

wherein the third input clock is delayed with respect to the first input clock as much as 180 degrees, and

wherein the fourth input clock is delayed with respect to the first input clock as

much as 270 degrees.

16. A clock converting circuit comprising:

a first switch connected between a first input node for receiving a first input clock and a first node and configured to operate in response to a first logic state of a second input clock delayed with respect to the first input clock as much as 90 degrees;

a second switch connected between a second input node for receiving the second input clock and a second node and configured to operate in response to a second logic state of the first input clock; and

a third switch connected between the first node and a power node and configured to operate in response to a second logic state of the second input clock opposite to the first logic state of the second input clock,

wherein the clock converting circuit is configured to output a first output clock and a first inverted output clock opposite to the first output clock based on the first and second input clocks.

17. The clock converting circuit of claim 16, further comprising:

a fourth switch connected between the second node and a ground node and configured to operate in response to a first logic state of the first input clock opposite to the second logic state of the first input clock.

18. The clock converting circuit of claim 16, further comprising:

a fourth switch connected between the second input node and a third node and configured to operate in response to a first logic state of a third input clock delayed with respect to the first input clock as much as 180 degrees;

a fifth switch connected between a third input node for receiving the third input clock and a fourth node and configured to operate in response to the second logic state of the second input clock;

a sixth switch connected between the third node and the power node and configured to operate in response to a second logic state of the third input clock opposite to the first logic state of the third input clock;

a seventh switch connected between the third input node and a fifth node and configured to operate in response to a first logic state of a fourth input clock delayed with respect to the first input clock as much as 270 degrees;

an eighth switch connected between a fourth input node for receiving the fourth input clock and a sixth node and configured to operate in response to the second logic state of the third input clock;

a ninth switch connected between the fifth node and the power node and configured to operate in response to a second logic state of the fourth input clock opposite to the first logic state of the fourth input clock;

a tenth switch connected between the fourth input node and a seventh node and configured to operate in response to a first logic state of the first input clock opposite to the second logic state of the first input clock;

an eleventh switch connected between the first input node and an eighth node and configured to operate in response to the second logic state of the fourth input clock; and

a twelfth switch connected between the seventh node and the power node and configured to operate in response to the second logic state of the first input clock.

19. The clock converting circuit of claim 18, further comprising:

a thirteenth switch connected between the second node and a ground node and

configured to operate in response to the first logic state of the first input clock;

a fourteenth switch connected between the fourth node and the ground node and configured to operate in response to the first logic state of the second input clock;

a fifteenth switch connected between the sixth node and the ground node and configured to operate in response to the first logic state of the third input clock; and

a sixteenth switch connected between the eighth node and the ground node and configured to operate in response to the first logic state of the fourth input clock.

20. The clock converting circuit of claim 16, wherein the first switch includes a first transmission gate configured to operate in response to the second input clock and a fourth input clock,

wherein the second switch includes a second transmission gate configured to operate in response to the first input clock and a third input clock,

wherein the third input clock is delayed with respect to the first input clock as much as 180 degrees, and

wherein the fourth input clock is delayed with respect to the first input clock as much as 270 degrees.