ABSTRACT

A MOSFET device structure formed on a silicon on insulator layer, and a process sequence employed to fabricate said MOSFET device structure, has been developed. The process features insulator filled, shallow trench isolation (STI) regions formed in specific locations of the MOSFET device structure for purposes of reducing the risk of parasitic transistor formation underlying a gate structure junction. After formation of either a "T" shaped, or an "H" shaped gate structure, body contact regions of a first conductivity type are formed adjacent to both an STI region and to a component of the gate structure. Formation of a source/drain region of a second conductivity type located on the opposite side of the same STI region, and the same gate structure component, is next performed. Unwanted parasitic transistor formation, which can occur underlying the gate structure via the body contact region and the source/drain region, is prevented by the presence of the separating STI region.

Figure 5